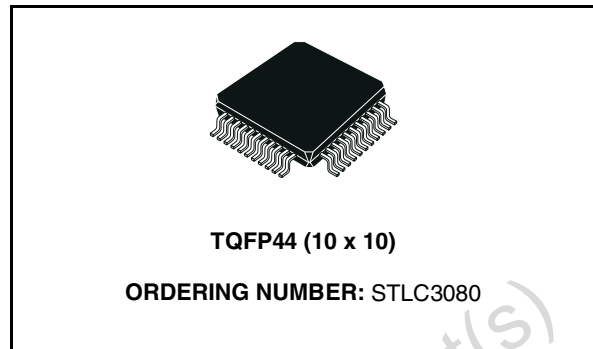


SUBSCRIBER LINE INTERFACE CIRCUIT

- MONOCHIP SLIC SUITABLE FOR PUBLIC APPLICATIONS
- IMPLEMENTES ALL KEY FEATURES OF THE BORSHT FUNCTION
- DUAL CONTROL MODE CONFIGURATION: SLAVE MODE OR AUTOMATIC ACTIVATION MODE.
- SOFT BATTERY REVERSAL WITH PROGRAMMABLE TRANSITION TIME
- ON HOOK TRANSMISSION
- LOOP START/GROUND START FEATURE WITH PROGR. THRESHOLD
- LOW POWER DISSIPATION IN ALL OPERATING MODES
- AUTOMATIC DUAL BATTERY OPERATION
- INTEGRATED RING TRIP DETECTION WITH AUTOMATIC AND SYNCHRONISED RING DISCONNECTION
- METERING PULSE INJECTION
- SURFACE MOUNT PACKAGE
- THREE RELAY DRIVERS FOR RING AND TESTING

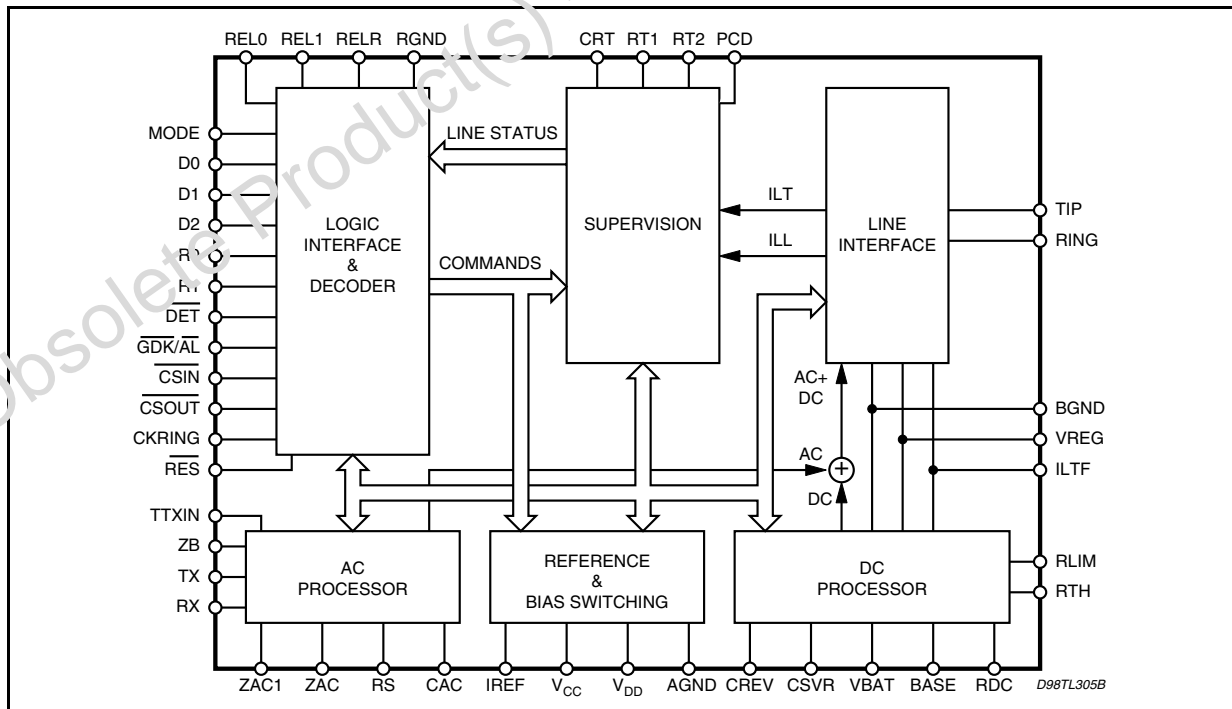


- -40 TO +85°C OPERATING RANGE

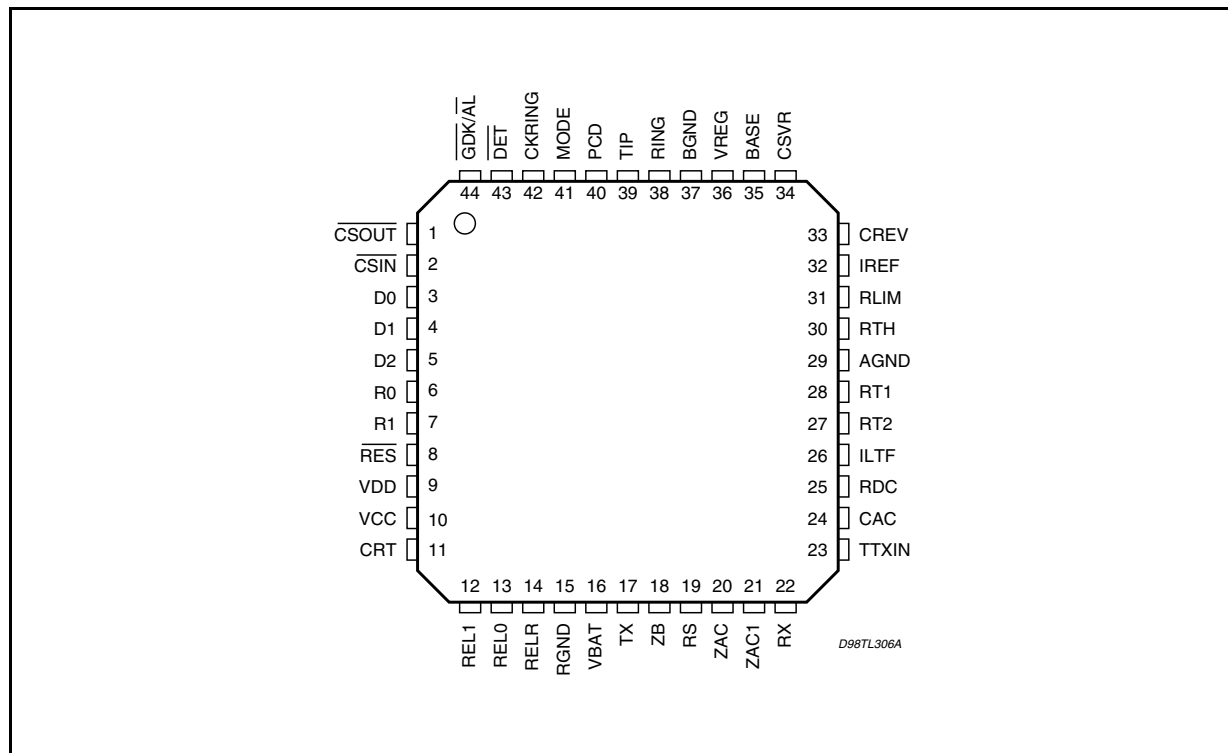
DESCRIPTION

The STLC3080 is a SLIC device suitable for a wide range of applications: public (CO), transmission (DLC) and private (PABX). The SLIC provides the standard battery feeding with full programmability of the DC characteristic. In particular two external resistors allow to set the limiting current value (up to 50mA) and the value of the resistive feeding when not in constant current region.

BLOCK DIAGRAM



PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{BAT}	Battery voltage	-80 + V_{CC} to +0.4	V
		-80 + V_{REL} to +0.4	V
V_{CC}	Positive supply voltage	-0.4 to +7	V
V_{DD}	Control Interface Supply Voltage	-0.4 to +7	V
I_{REL}	Current into relay drivers	80	mA
A/R/BGND	AGND respect BGND respect RGND	-2 to +2	V

OPERATING RANGE

Symbol	Parameter	Value	Unit
T_{opT}	Operating temperature range	-40 to +85	°C
V_{CC}	Positive supply voltage	4.75 to 5.25	V
V_{DD}	Control Interface Supply Voltage	3 to 5.25	V
V_{BAT}	Battery voltage	-73 to -15	V
		if $V_{REL} > V_{CC}$ -78 + V_{REL} to -15	V
A/R/BGND	AGND respect BGND respect RGND	-0.3 to +0.3	V
PD (70)	Max. power dissipation @ $T_{amb} = 70^{\circ}C$	1.1	W
PD(85)	Max. power dissipation @ $T_{amb} = 85^{\circ}C$	0.9	W

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal resistance Junction to Ambient Typ.	60	°C/W

PIN DESCRIPTION

Pins	Name	Description
1	$\overline{\text{CSOUT}}$	Chip-Select for output control bits $\overline{\text{DET}}$ and $\overline{\text{GDK}}$. Active Low. (*)
2	$\overline{\text{CSIN}}$	Chip-Select for input control bits latches D0 D1 D2 R0 R1. Active Low. (*)
3	D0	Control Interface input bit 0. (*)
4	D1	Control Interface input bit 1. (*)
5	D2	Control Interface input bit 2. (*)
6	R0	Relay driver 0 command. Active High. (*)
7	R1	Relay driver 1 command. Active High. (*)
8	$\overline{\text{RES}}$	Reset Input; active low.
9	V _{DD}	Control interface Power Supply. V _{DD} = 3.3V or V _{DD} = V _{CC} .
10	V _{CC}	Positive Power Supply (+5V).
11	CRT	Ring-Trip time constant capacitor.
12	REL1	Relay 1 driver output.
13	REL0	Relay 0 driver output.
14	RELR	Ringer Relay driver output.
15	RGND	Relay drivers ground.
16	V _{BAT}	Negative Battery Supply.
17	TX	4 wires output stage (Transmitting Port).
18	ZB	Cancelling input of Balance Network for 2 to 4 wires conversion.
19	RS	Protection resistors image. The image resistor is connected between this node and ZAC.
20	ZAC	AC impedance synthesis.
21	ZAC1	RX buffer output/ AC impedance is connected between this node and ZAC.
22	RX	4 wires input stage (Receiving Port). A 100K external resistor must be connected to AGND to bias the input stage.
23	TTXIN	Metering Signal Input (AC) and Line Voltage Drop Programming (DC). If not used must be connected to AGND.
24	CAC	AC feedback input/ AC-DC split capacitor is connected between this node and ILTF.
25	RDC	DC current feedback input. The RDC resistor is connected between this node and ILTF.
26	ILTF	Transversal Line Current Image.
27	RT2	Input pin to sense ringing current, for Ring-Trip detection.
28	RT1	Input pin to sense ringing current, for Ring-Trip detection.
29	AGND	Analog ground.
30	RTH	Off-Hook threshold programming pin.
31	RLIM	Limiting current programming pin.
32	IREF	Voltage reference output to generate internal reference current.
33	CREV	Reverse polarity transition time programming.
34	CSVF	Battery supply filter capacitor.
35	BASE	Driver of the external transistor. Connected to the base.
36	VREG	Regulated voltage. Provides the negative supply to the power line drivers. It is connected to the emitter of the external transistor.
37	BGND	Battery ground.
38	RING	B wire termination output. IB is the current sunk into this pin.
39	TIP	A wire termination output. IA is the current sourced from this pin.
40	PCD	Power Cross Detection Input
41	MODE	Interface Control Mode selection.
42	CKRING	Clock at ringing frequency for relay synch and time reference for Automatic activation
43	$\overline{\text{DET}}$	Off-hook and Ring-Trip detection bit. Tri-State Output/Active Low.
44	$\overline{\text{GDK/AL}}$	Ground-Key/Alarm detection bit. Tri-State Output. Active Low.

* Input pins provided with 15 μ A sink to AGND pull-down.

CONTROL INTERFACE
Slave mode (MODE=Low).

INPUTS					OPERATING MODE	OUTPUTS	
R0	R1	D0	D1	D2		$\overline{\text{DET}}$ (Active Low)	$\overline{\text{GDK/AL}}$ (Active Low)
X	X	0	0	0	Power down	disable	disable
X	X	0	0	1	Stand-by	off/hk	gnd-key
X	X	0	1	0	Active N.P.	off/hk	gnd-key
X	X	0	1	1	Active R.P.	off/hk	gnd-key
X	X	1	0	0	Ringing (with SLIC Active N.P.)	ring/trip	disable
X	X	1	0	1	Ringing (with SLIC Active R.P.)	ring/trip	disable
X	X	1	1	0	Ground start	off/hk	gnd-key
X	X	1	1	1	High Impedance Feeding	off/hk	disable
0/1	X	X	X	X	Rel 0 (on = 1, off = 0)	def by D0-D2	def by D0-D2
X	0/1	X	X	X	Rel 1 (on = 1, off = 0)	def by D0-D2	def by D0-D2

A parallel interface allow to control the operation of STLC3080 through a control bus:

- D0 D1 D2 latched input bits defining the Slic operation mode
- R0 R1 latched input bits (active High) drive the test relays.
- $\overline{\text{DET}}$ and $\overline{\text{GDK/AL}}$, tri-state outputs, signal the status of the loop: On/Off-Hook and Ground-Key. Pin GDK/AL goes low also when the device thermal protection is activated or a line fault (Tip to Ring, Tip and/or Ring to Ground or VBAT) is detected (flowing current $\geq 7.5\text{mA}$).
- $\overline{\text{CSIN}}$: chip select for input bits, active Low, strobes the data present on the control bus into the internal latch.
- $\overline{\text{CSOUT}}$: chip select for output bits ; active Low, when high $\overline{\text{DET}}$ and $\overline{\text{GDK/AL}}$ goes tri-state.

D0 D1 D2 R0 R1 $\overline{\text{CSIN}}$ and $\overline{\text{CSOUT}}$ inputs are provided with a $15\mu\text{A}$ pull-down current to prevent uncontrolled conditions in case the control bus goes floating.

According to the above table, 8 operating modes can be set:

- 1) Power-Down.
- 2) Stand-By.
- 3) Active N.P.
- 4) Active R.P.
- 5) Ringing (with SLIC Active N.P.).
- 6) Ringing (with SLIC Active R.P.).
- 7) Ground start.
- 8) High Impedance Feeding.

Power-Down

It's an idle state characterised by a very low power consumption; any functionality is disabled; only relays Rel0 and Rel1 can be driven by proper setting of bits R0 and R1.

It can be set during out of service periods just to

reduce the power consumption.

It is worth noticing that two other conditions can set the Slic in idle state but with some differences as reported in the table:

Idle State	Rel0/1 Drive	$\overline{\text{DET}}$	$\overline{\text{GDK/AL}}$
Power Down	Enable	Disable	Disable
Reset	Disable	Disable	Disable
Thermal Alarm	Enable	Low	Low

Stand-By.

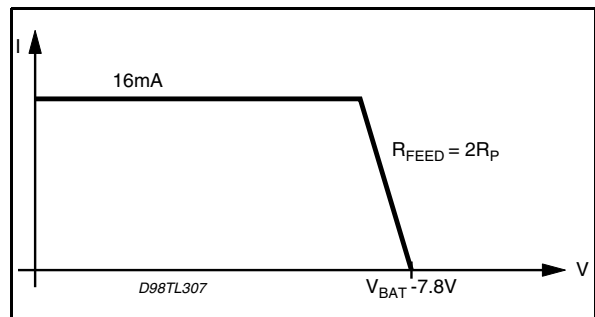
Mode selected in On-Hook condition when high immunity to common mode currents is needed for the $\overline{\text{DET}}$ bit.

To reduce the current consumption, AC feedback loop is disabled and only $\overline{\text{DET}}$ and $\overline{\text{GDK/AL}}$ detectors are active.

DC current is limited at 16mA (not programmable); feeding characteristic shown in fig. a.

The voltage drop in on-hook condition is 7.8V.

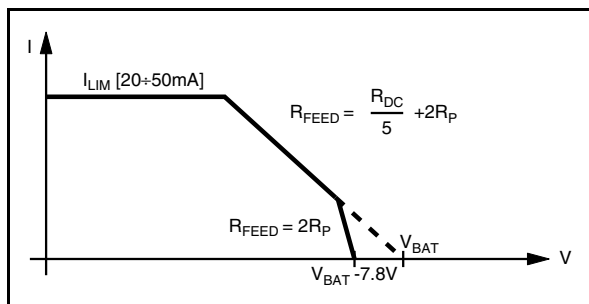
Figure a: STLC3080 DC Characteristic in Stand-By Mode.



Active

Mode selected to allow voice signal transmission. When in ACTIVE mode the voltage drop in on-hook condition is 7.8V in order to allow proper on-hook transmission (Fig. b).

Figure b. STLC3080 DC Characteristic in Active Mode.



Resistive Region is programmable by means of external resistor R_{DC} , limiting current can be selected by R_{LIM} resistor.

Concerning AC characteristic the STLC3080 allows to set 2W termination impedance by means of one external scaled impedance that may be complex. Two to four wire conversion is provided by an external network. Such network can be avoided in case of application with COMBOII, in this case the two to four wire conversion is implemented inside the COMBOII by means of the programmable Hybal filter.

When in ACTIVE mode it is also possible to perform battery reversal in soft mode (with programmable transition time) without affecting the AC signal transmission.

Ringling

When Ringling mode is selected the STLC3080 activates the ring relay injecting the ringling signal on the line. As the ring trip is detected the logic indicator \overline{DET} is set low and the ringling is automatically disconnected without waiting for the card controller command (auto ring trip).

\overline{DET} remains latched Low until the operative mode is modified.

If required, the ringling relay drive signal RELR can be synchronised to a clock applied to CKRING input.

This clock is derived from the ringling signal with proper time delay, according to the activation/deactivation time of the relay.

RELR is activated on the low level of CKRING clock. The duty cycle of CKRING can be modified in order to activate the RELR when required: CKRING low must last 1µs minimum.

If the synchronisation is not required, CKRING input must be steadily kept Low.

All the STLC3080 relay drivers are open drain with the source connected to the RGND pin. Each relay drivers integrates a protection structure that allows to avoid external kick - back diodes, using both 5V or 12V relays.

The ring trip circuit and its behaviour is described in Appendix D.



Ground Start.

This mode is selected when the SLIC is adopted in a system using the Ground Start feature. In this mode the TIP termination is set in High Impedance (100kΩ) while the RING one is active and fixed at $V_{bat} + 4.8V$. In the case of connection of RING termination to GND the sunked current is limited to 30mA. When RING is connected to GND both Off-Hook and Ground-Key detectors become active. Power dissipation in this mode with a -48V battery voltage is 100mW

High Impedance Feeding.

As Stand-By, this mode is set in On-Hook condition, with further reduced power consumption.

Higher power efficiency turns back a lower immunity of the Off-Hook detector to line common mode currents.

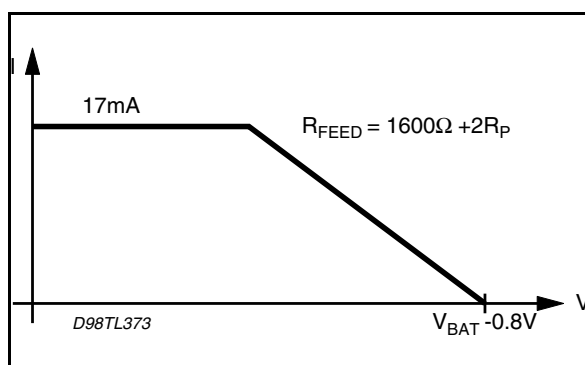
The DC feeding shows a constant current characteristic ($I_{lim} = 17mA$) followed by a resistive range with an equivalent series resistance $R_{FEED} = 1600\Omega + 2R_p$.

Thermal protection circuit is still active, preventing the junction temperature, in case of fault condition, to exceed 150°C

In High Impedance Feeding most of the circuit is switched off, only the circuit, dedicated to Off-Hook detection, is powered. This allows to reduce the total power consumption in On-hook to 30mW (typical).

The Off-Hook detection threshold is not programmable but defined at a fixed $I_{DET_{HI}} = 8mA(max.)$

Figure c. STLC3080 DC Characteristic in High Impedance Feeding



CONTROL INTERFACE

Automatic activation mode (MODE=High).

Inputs						Operating Mode (Mode = High)	Outputs	
R0	R1	D0	D1	D2	RES		DET	GDK/AL
X	X	0	0	0	1	Power Down	disable	disable
X	X	0	0	1	1	Ringing	Ring-Trip	disable
X	X	0	1	0	1	On-Hook Transmission Reverse Polarity	Off-Hook Fault	Fault
X	X	0	1	1	1	On-Hook Transmission Direct Polarity	Off_Hook Fault	Fault
X	X	1	0	0	1	Active Direct Polarity (default)	Off_Hook Fault	Fault
X	X	1	0	1	1	Active Direct Polarity (default)	Off_Hook Fault	Fault
X	X	1	1	0	1	Active Reverse Polarity	Off_Hook Fault	Fault
X	X	1	1	1	1	Active Direct Polarity (default)	Off_Hook Fault	Fault
0/1	X	X	X	X	1	R0 = 0/1: Rel0 = off/on	(1)	(1)
X	0/1	X	X	X	1	R1 = 0/1: Rel1 = off/on	(1)	(1)
X	X	X	X	X	0	Power Down; Rel0/1 = off	disable	disable

DET: On/Off Hook Signalling ; together with GDK/AL it is set Low also in case of Thermal Alarm or Ground-Key.

GDK/AL : Thermal Alarm or Ground-Key Signalling

(1) : DET and GDK/AL signalling function is related to D0,D1,D2 and it doesn't depend on R0 and R1 setting.

As in Slave mode the control is performed through a parallel bus, with independent chip selects, CSIN and CSOUT, for inputs and outputs.

In Automatic Activation, once Active mode is selected the device automatically selects the proper operating mode (Active, Stand By or H.I. feeding) depending on the loop status in order to optimise the power consumption.

In order to guarantee the proper behaviour of the internal state machine the "CKRING" signal must be always applied, this signal in fact is used to generate the "WTIME" delay (see Appendix) necessary to properly perform automatic state change.

Power-Down

It's an idle state characterised by a very low power consumption; any functionality is disabled; only relays Rel0 and Rel1 can be driven by proper setting of bits R0 and R1.

It can be set during out of service periods just to reduce the power consumption.

It is worth noticing that two other conditions can set the Slic in idle state but with some differences as reported in the table:

Idle State	Rel0/1 Drive	DET	GDK/AL
Power Down	Enable	Disable	Disable
Reset	Disable	Disable	Disable
Thermal Alarm	Enable	Low	Low

Ringing

When Ringing mode is selected the STLC3080 activates the ringing relay injecting the ringing signal on the line.

As a Ring-Trip is detected the logic indicator DET is set Low and the ringing relay is automatically switched-off without waiting for the card controller command (auto ring-trip).

DET remains latched Low until the operative mode is modified.

Ringing relay drive signal RELR must be synchronised to a clock applied to CKRING input. This clock is derived from the ringing signal with proper time delay, according to the activation / deactivation time of the relay.

RELR is activated on the low level of CKRING clock. The duty cycle of CKRING can be modified in order to activate the RELR when required: CKRING low must last 1µs minimum.

All the relay drivers are open-drain with the source connected to RGND pin.

Each relay driver integrates a protection structure to avoid external kick-back diodes using both 5V or 12V relays.

The ring trip circuit and its behaviour is described in Appendix D.

On-Hook Transmission.

Sets the Slic for conversation even though the line is in On-Hook; it is required for On/Hook transmission purposes; Active mode cannot support a conversation when the line is in On-Hook as it automatically turns in High Impedance Feeding.

Active.

The relevant feature of this setting is that when Active Mode (D0D1D2=1XX) is set by the external control, internally, the device is able to select between three operative states according to the status of the line:

- High Impedance Feeding :

entered after a Power-On Reset or 1XX word, this status is set during steady On/Hook condition; most of the circuitry is idle and only a low power Off-Hook detection circuit is kept alive.

Direct Polarity only is assumed, independently of the selected one.

To minimise the power consumption the Off-Hook detection circuit has low common mode current rejection.

- Stand by

Notice that in Stand-By state the Off-Hook detector is sensitive only to the transversal component of the line current with high immunity to common mode disturbances; this performance implies an increasing in power consumption: for that reason Stand-By is not used as a quiescent state.

- Active state gets operative for conversation after an Off-Hook validity check performed in Stand-By state, set after any Off-Hook detected in High Impedance Feeding.

If the Off-Hook condition is confirmed in Stand By, Active mode is set; if not (in case of spurious detection), false activation is prevented, and High Impedance Feeding is resumed.

In order to have the device falling back in HI-feeding mode after the line is back in on-hook condition. It is necessary to select as input state the active direct polarity mode (default).

During Active state On/Off-Hook status will affect in real time DET signalling bit.

In order to allow Pulse-Mode Dialling, once Active state is set, it cannot be changed by fast On-Hook, but it is turned back to High Impedance Feeding only if an On-Hook condition lasts longer than $128 \times \text{CKRING}$ period.

Automatic activation (and deactivation) is based on an internal state-machine which is clocked by a free running internal oscillator.

A detailed description is reported in the Appendix A.

DUAL BATTERY CONFIGURATION

STLC3080 is also meant for low power consumption systems using Dual Battery solution. It is sufficient to connect the collector of the external transistor, through a diode, to the reduced battery (see Fig. 2 for single battery solution and Fig. 3 for dual battery solution). The activation of the batteries is automatic, only depending on the DC load at the RING and TIP terminals; no controllers action is required.

PROTECTION CIRCUIT

- Suggested protection circuit is based on programmable Trisils (like LCP1511/2) as shown in Fig.2 and Fig. 3, and the surge current is limited by the resistors RPT2 and RPR2, which are PTC types, protecting the device against

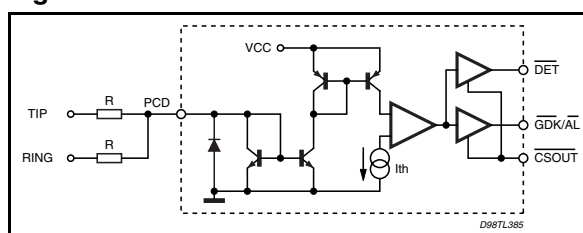
both lightning and power-cross.

- Additionally, STLC3080 is provided with the PCD input to directly monitor overvoltages applied to the line wires.

When the current injected into PCD exceeds a threshold of $320\mu\text{A}$ ($\pm 30\%$), DET and GDK/AL are set Low signalling a fault condition. No change on the SLIC mode is performed.

Voltage threshold is defined by proper value of the series resistors (see Fig.1)

Figure 1.



This circuit gives the possibility to protect the device against power crosses through a relay instead of PTCs; once the fault condition is detected the controller drives this relay disconnecting the Slc from the line terminals.

METERING PULSE INJECTION

STLC3080 provides external pins and components for Metering Pulse injection. TTXIN pin is the input for the 12kHz or 16kHz Metering Pulse injection. This pin also provides a DC constant current source that is injected into the external RDA resistor (typ. $10\text{k}\Omega$ to obtain 2.2Vrms on 200Ω) connected between TTXIN pin and AGND. The voltage drop across TIP and RING line amplifiers and, consequentially the AC swing available.

When Metering Pulse injection is not used and voltage drop is not required, TTXIN must be shorted to AGND and RTTX, RDA and CTTX external components must be removed. The TTX cancellation is obtained through an external RTTX and CTTX network connected between TTXIN and CAC pins.

Fault detection

The device provides current sense on TIP and RING wires that allow to detect longitudinal DC current (I_{LL}). When this I_{LL} current becomes higher than a threshold (see detectors table inside electrical characteristics) a fault indication is provided on DET and GDK pin (both outputs become low). The fault indication is active till the fault cause persists. With this circuit the following fault condition can be detected.

TIP to VB1
 TIP to GND
 RING to VB1
 RING to GND
 RING to TIP to VB1

When a fault is detected the line current is limited in order to avoid any damage on the device itself and also on the external transistor.

MISCELLANEOUS

- Thermal overload: the integrated thermal protection is activated when Tj reaches 150°C typ.: the SLIC is forced in Power-down mode, DET and AL are set Low. The RELR relay driver is turned off while it is still possible to control REL0 and REL1 through R0 and R1 inputs.
- One low cost external transistor allows to reduce the power dissipated in the SLIC itself allowing the use of extreme small size package (TQFP44). The external transistor size/package can be selected depending on the max. power requested by the particular application.
- The SLIC supports loop start lines and gives the possibility to set loop current indicator threshold by means of one external resistor.

EXTERNAL COMPONENTS LIST

To set the SLIC into operation the following parameters have to be defined:

- The DC feeding resistance "Rfeed" defined as the resistance of the traditional feeding system (most common Rfeed values are: 400, 800, 1000 ohm).
- The AC SLIC impedance at line terminals "Zs" to which the return loss measurements is referred. It can be real (typ. 600 ohm) or complex.
- The equivalent AC impedance of the line "Zl" used for evaluation of the trans-hybrid loss performance (2/4wire conversion). It can be a complex impedance.
- The value of the two protection resistors Rp in series with the line termination.
- The reverse polarity transition time defined as "ΔV_{TR}/ΔT".
- The constant current limit value "I_{lim}".
- Rth: sets the OFF/Hook DETection threshold

Once, the above parameters are defined, it is possible to calculate all the external components using the following table.

EXTERNAL COMPONENTS

Name	Function	Formula	Typical Value
CVCC	Positive Supply Filter		100nF ±20%
CVB	Battery Supply Filter		100nF ±20% 100V
R _{REF} (*)	Internal current reference programming resistor	$I_{REF} = \frac{1.16}{R_{REF}}$	30.1kΩ ± 1%
C _{SVR}	Battery ripple rejection capacitance	$C_{SVR} = \frac{1}{2\pi \cdot fp \cdot 1.3M\Omega}$	100nF ±10% 100V @ fp = 1.22Hz
C _{RT}	Ring Trip capacitance	see Appendix D	470nF ±20% 6V @ 25Hz
R _{DC}	DC synthesized resistance programming resistor	$R_{DC} = 5[R_{feed} - 2Rp]$ $R_{DC} \geq 1k\Omega$	1.5kΩ ±1%
C _{AC}	AC/DC splitter capacitance	$C_{AC} = \frac{1}{2\pi \cdot f_{sp} \cdot R_{DC}}$	10μF ±20% 15V @ f _{sp} = 10Hz
R _S	Protection resistor image	$R_S = 25 \cdot 2Rp$	2.5kΩ ±1%
Z _{AC}	2 wire AC impedance	$Z_{AC} = 25[Z_s - 2Rp]$	12.5kΩ ±1%
Z _A	SLIC impedance balancing network	$Z_A = 25 \cdot Z_s$	15kΩ ±1%
Z _B	Line impedance balancing network	$Z_B = 25 \cdot Z_l$	15kΩ ±1%
C _{COMP}	AC feedback compensation capacitance	$C_{COMP} = \frac{2}{2\pi \cdot fo[100 \cdot Rp]}$	220pF ±20% @ fo = 250kHz
RR	Feeding resistance for Ring Injection	≥400Ω	600Ω 2W
RS1	Sensing resistor for Ring Trip	1000 · RR	600kΩ ±1%
RS2	Sensing resistor for Ring Trip	1000 · RR	600kΩ ±1%
RT	Feeding resistance for Ring Injection	≥0Ω	0Ω
Q _{EXT}	External transistor	(1)	BD140, MJD32
RPT1	Line series resistor	≥20Ω	
RPR1	Line series resistor	≥20Ω	20Ω 1/4W ±1%

EXTERNAL COMPONENTS (continued)

Name	Function	Formula	Typical Value
R _{LIM} (*)	Current limiting setting resistor	$R_{LIM} = 10^3 \cdot \frac{1.16}{I_{LIM}}$ 23.2kΩ ÷ 58kΩ	51.1kΩ ±1%
R _{TH} (**)	OFF/HOOK \overline{DETE} detection threshold setting resistor.	$R_{TH} = 200 \cdot \frac{1.16}{I_{TH}}$ 21.1kΩ ÷ 77.3kΩ	26.1kΩ ±1%
C _{REV}	Polarity reversal transition time programming	$C_{REV} = \frac{K}{\frac{\Delta V_{TR}}{\Delta T}}$; $K = \frac{1}{3750}$	47nF for 5.67V/ms
RDA	Output Voltage Drop Adjustment	$RDA = \frac{\Delta Drop \cdot 20k\Omega}{9.6 - \Delta Drop}$	10kΩ ($\Delta Drop = 3.2V$) (2)
R1, R2	Power Cross Detection		240kΩ (3)
R _{TTX}	Teletax Cancellation Resistor	$R_{TTX} = 12.5 \cdot [Re(Z_{LTTX}) + 2R_P]$	3.75kΩ
C _{TTX}	Teletax Cancellation Capacitor	$C_{TTX} = \frac{1}{(12.5 \cdot I_m(Z_{LTTX}) \cdot 2\pi \cdot f_{TTX})}$	
RPT2	Protection resistor	≥ 8Ω	20Ω 1/4W ±1%
RPR2	Protection resistor	≥ 8Ω	20Ω 1/4W ±1%
D1	Overvoltage protection		1N4448
D2	Dual Battery Operation		1N4448
CH	Trans-Hybrid Loss Frequency Compensation	CH = CCOMP	220pF ±30%

Notes:

- (1) Transistor characteristics: $h_{FE} \geq 25$, $I_C \geq 100mA$, $V_{CEO} \geq 60V$, $f_T \geq 20MHz$ in all operating range (I_C from 1 to 100mA). PDISS depends on application, see Appendix.
For SMD application possible alternatives are MJD350 in D-PACK or BCP53 in SOT223
- (2) Typical value needed for 2.2Vrms metering pulse level, if no metering RDA = 0Ω.
- (3) These resistors are needed to activate the power cross detection circuit, they should withstand the typical lighting voltage. If the power cross detection is not needed R1, R2 can be avoided.
- (*) R_{REF} and R_{LIM} should be connected close to the corresponding pins of STLC3080.
Avoid any digital line or high voltage swing line to pass close to R_{REF} and R_{LIM} pins. Eventually screen these pins with a GND track.
- (**) Inside the formula the coefficient 1.16 must be changed to 1.20 if the selected value of I_{th} is lower than 5mA.

STLC3080

Figure 2. Typical application diagram.

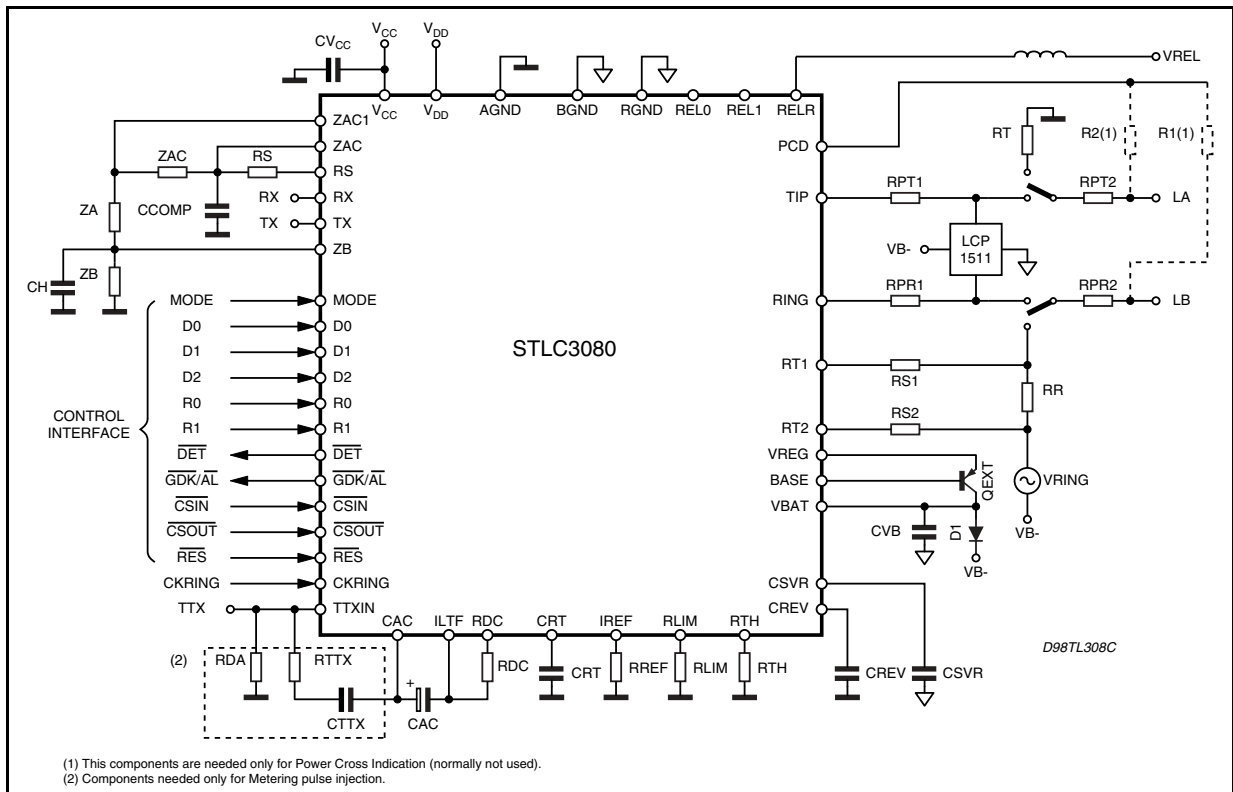
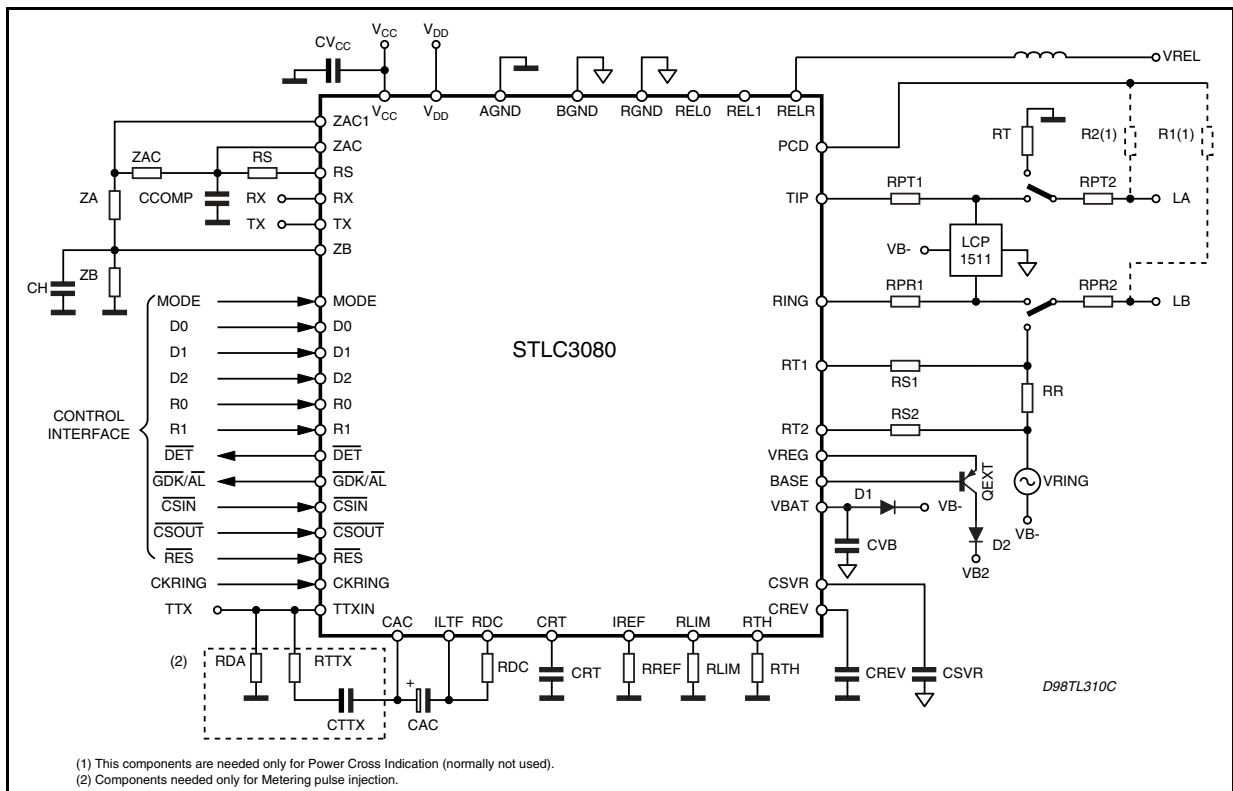


Figure 3. Typical dual battery application diagram.



ELECTRICAL CHARACTERISTICS (Test Condition, unless otherwise specified: $V_{CC} = 5V$, $V_{DD} = 3.3V$, $V_B = -48V$, $AGND = BGND = RGND$, $T_{amb} = 25^{\circ}C$).

Note: the limits below listed are guaranteed with the specified test condition and in the 0 to 70°C temperature range. Performances over -40 to +85°C range are guaranteed by product characterisation.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
AC CHARACTERISTICS							
Zil	Long. Impedance	each wire			40	Ω	
I _{ii}	Long. Current Capability AC	H.I. feeding per wire (ON-HOOK)		5		mApk	
		STANDBY or ACTIVE per wire (ON-HOOK)		13		mApk	
		ACTIVE per wire (OFF-HOOK). I _T = Transversal Current		80 -I _T		mApk	
L/T	Long. to transv.	NP with nominal R _P at 300Hz	60			dB	C5
		NP with nominal R _P at 1020Hz	60			dB	
		NP with nominal R _P at 3400Hz	55			dB	
T/L	Transv. to long	NP with nominal R _P at 300Hz	37			dB	
		NP with nominal R _P at 1020Hz	40			dB	
		NP with nominal R _P at 3400Hz	40			dB	
2wRL	2W return loss.	300 to 3400Hz	22			dB	C6
THL	trans-hybrid loss.	1020Hz; 20Log VRX/VTXI	30			dB	C2
Ovl	2W overload level	ACTIVE MODE at line terminals on ref. impeded.	3.2			dBm	
TXoff	TX output offset		-200		200	mV	
G24	Transmit gain abs.	0dBm 1020Hz	-12.38		-12.02	dB	C4
G42	Receive gain abs.	0dBm 1020Hz	5.74		6.1	dB	C1
G24fq	tx gain variation vs. frequency	rel. 1020Hz, 0dBm 300 to 3400Hz	-0.1		0.1	dB	
G42fq	rx gain variation vs. frequency	rel. 1020Hz, 0dBm 300 to 3400Hz	-0.1		0.1	dB	
G24lv	Tx gain variation vs. level	f = 10120Hz, input level from 3dBm to -40dBm	-0.1		0.1	dB	
G42lv	Rx gain variation vs. level		-0.1		0.1	dB	
V2wp	idle channel noise at line terminals	psophometric, Active On Hook		-82	-78	dBmp	C8
V4wp	idle channel noise at TX port	psophometric, Active On Hook		-90	-84	dBmp	C7
Thd	total harm. dist. 2w-4w, 4w-2w	0dBm, 1KHz I _I = 20 to 45mA			-50	dB	
G _{TTX}	Transfer Gain	V _{TTX} = 100mV _{RMS} @ 16kHz $G_{TTX} = 20\text{Log} \left(\frac{V_L}{V_{TTX}} \right)$ with R _L = 200 Ω		14.5		dB	
THD (TTX)	TTX Harmonic Distortion	2.2V _{RMS} = on 200 Ω			3	%	
DC CHARACTERISTICS (TTX pin connected to ground)							
V _{lohi}	Line voltage	I _I = 0, H.I. feeding	47	47.4	47.8	V	
V _{lo}	Line voltage	I _I = 0, SBY/ACTIVE/ON-HOOK	38.9	39.9	40.9	V	
I _{lims}	Short circ. curr.	R _{loop} = 0, SBY	14	16	18	mA	
I _{limb}	Short circ. curr.	R _{loop} = 0, H.I. feeding	11	17	20	mA	
I _{lima}	Lim. current accuracy	Rel to progr. val. 20 to 50mA ACTIVE NP, RP	-10		10	%	
V _{REF}	Bang up reference		1.08	1.16	1.24	V	
R _{feed}	Feed res. accuracy	ACTIVE NP, RP	-10		10	%	
R _{feed} H.I.	Feeding resistance	H.I. feeding	1100		2100	Ω	

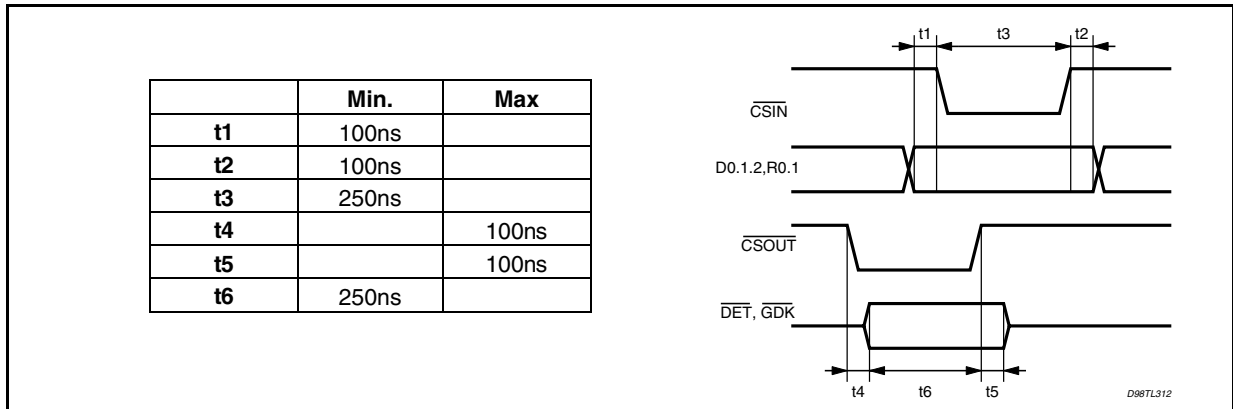
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I _{lact}	Feed current ACTIVE	ACTIVE NP, RP Rloop = 1900Ω RDC = 1.5kΩ	18	20		mA	
I _{lsby}	Feed current STBY	STY, Rloop = 2.2KΩ RDC = 1.5kΩ	13			mA	
I _{TIP}	Tip leakage current	Ground Start			1	μA	
I _{GS}	Ring Lead Current	Ground Start Ring to GND		33		mA	
I _{DA}	Reference current sourced by TTX IN pin for Voltage Drop programming	V _{TTX} = 0V	-70	-60	-45	μA	
DETECTORS							
I _{det}	Off-hook current threshold ST-BY, ACTIVE	Rel. to progr. val. 7 to 11mA	-10		+10	%	
		Rel. to progr. val. 3 to 6mA	-20		+20	%	
I _{det} H.I.	Off-Hook current threshold	H.I. feeding	5		8	mA	
Hys	Off/On hook hyst.	ST-BY, ACTIVE		15% I _{det}		mA	
Td	Dialling distortion	ACTIVE	-1		+1	ms	
I _{LL}	Ground Key Current threshold I _{LL} = I _B - I _A	TIP to RING to GND or RING to GND		7.5		mA	
I _{gst}	Ground Start detection threshold	I _{gst} = 2 · I _{det} GROUND START	-10		+10	%	
DIGITAL INTERFACE							
INPUTS: D0, D1, D2, R0, R1, <u>CSIN</u> , <u>CSOUT</u>							
V _{ih}	Input high voltage	V _{DD} = 3.3V	2			V	
V _{il}	Input low voltage	V _{DD} = 3.3V			0.8	V	
I _{ih}	Input high current				30	μA	
I _{il}	Input low current				10	μA	
OUTPUTS: DET, GDK /AL							
V _{ol}	Output low voltage	I _{ol} = 0.75mA; <u>CSOUT</u> = LOW			0.5	V	
V _{oh}	Output high voltage	I _{oh} = 0.1mA; <u>CSOUT</u> = LOW	2.4			V	
I _{oz}	Tri-State Output Current	<u>CSOUT</u> = High	-10		+10	μA	
OUTPUTS: RELR, REL0, REL1							
I _{rd}	Current capability		40			mA	
V _r	Output voltage	I _{rd} = 40mA			0.6	V	
		I _{rd} = 70mA			1.1	V	
I _{lk}	Off leakage current				3	μA	
POWER SUPPLY REJECTION							
PSRRC	V _{CC} to 2W port	V _{ripple} = 0.1V _{rms} 50 to 4000Hz	27			dB	C9
PSRRB	V _{bat} to 2W port	V _{ripple} = 0.1V _{rms} 50 to 4000Hz	30			dB	C9
POWER CONSUMPTION							
I _{cc}	V _{CC} supply current	H. I. Feeding On-Hook From 0 to 70°C From -40 to 85°C			1.0 1.5	mA mA	
		SBY On-Hook From 0 to 70°C From -40 to 85°C			3.5 4	mA mA	
		Active On-Hook From 0 to 70°C From -40 to 85°C			5.0 5.5	mA mA	
		Power Down From 0 to 70°C From -40 to 85°C			1.0 1.5	mA mA	

ELECTRICAL CHARACTERISTICS (continued)

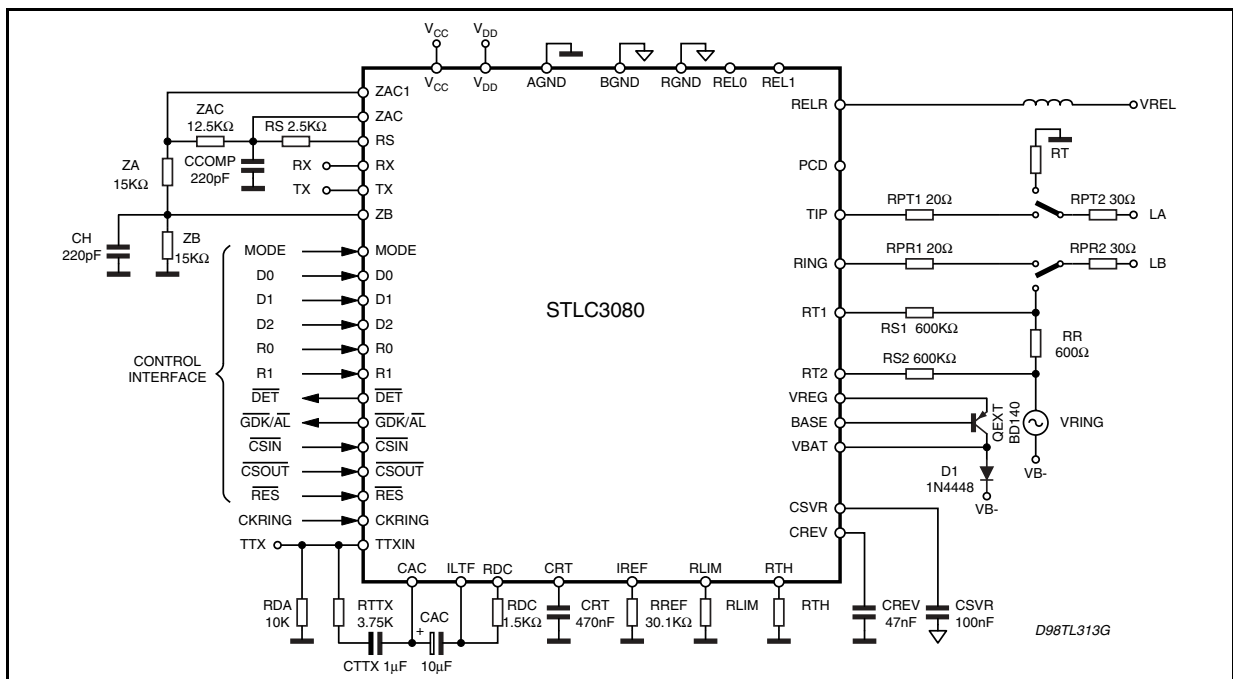
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I _{BAT}	V _{BAT} supply current	H. I. Feeding On-Hook From 0 to 70°C From -40 to 85°C			0.5 1.0	mA mA	
		SBY On-Hook From 0 to 70°C From -40 to 85°C			2.5 3.5	mA mA	
		Active On-Hook From 0 to 70°C From -40 to 85°C			4.5 5.0	mA mA	
		Power Down From 0 to 70°C From -40 to 85°C			0.5 1.0	mA mA	
I _{DD}	V _{DD} Supply Current	Any operating mode		100	320	μA	

LOGIC INTERFACE INPUT TIMING



Note: All measurements are performed with 100pF on outputs pin and with TTL compatible voltage levels.

Figure 4. Test Circuit.



APPENDIX A

The flow-chart in Fig.A1 describes the sequence of state machine supervising the STLC3080 operation when the control is set for Active mode, D0 D1 D2= 1 X X.

The state machine is a synchronous sequential circuit internally clocked by a free running oscillator ; the ringing frequency applied at the CKRING input is used to generate the long time delay $WTIME=128 \times CKRING$ necessary for proper operation as further described.

External control is supposed to be set for Active mode :

D0 D1 D2= 1 X X.

OH-HI : line status flag , set High when Off-Hook condition is detected in High Impedance Feeding; it differs from OHK because it's sensitive to the longitudinal current.

OHK: line status flag , set High when Off-Hook condition is detected in Stand-By or in Active mode; it differs from OH-HI for its immunity to longitudinal current .

DLY: time-out flag, it is set High to resume, with a given delay, the High Impedance Feeding when an On-Hook condition (OHK=Low) is detected in Stand-By or Active state.

1) Note that in this section the word "mode" has been used to indicate the operating status set with D0, D1 and D2 pin: the word "state" has been used to indicate an internal status of the finite state machine.

Flow-chart Description

H) A Reset condition, generated at Power On or setting RES pin Low, forces a Power-Down condition.

A) High Impedance Feeding is entered after the Active mode word is set and its maintained un-

til an Off-Hook condition is detected (OH-HI=High) ; in this case Stand-By state entered.

B) Stand-By state is set to perform a validity check of the Off-Hook status of the line before entering Active state. If it is confirmed (OH=High), immediately Active state is entered.

If not , Stand-By state remains set for a time period WTIME generated through a counter that times out after $128 \times CKRING$; DLY=High signals the state machine the time out to resume the High Impedance Feeding.

An OHK = High detected during WTIME will immediately enter Active state.

C) Active state is set for conversation and \overline{DET} =Low signals to the controller the Off-Hook condition of the line.

The status remains set as long as OHK=High (Off-Hook).

D) When OHK=Low is detected (On Hook), \overline{DET} is immediately set High whereas Active state is maintained for the period WTIME; when it expires DLY is set High and High Impedance Feeding is resumed.

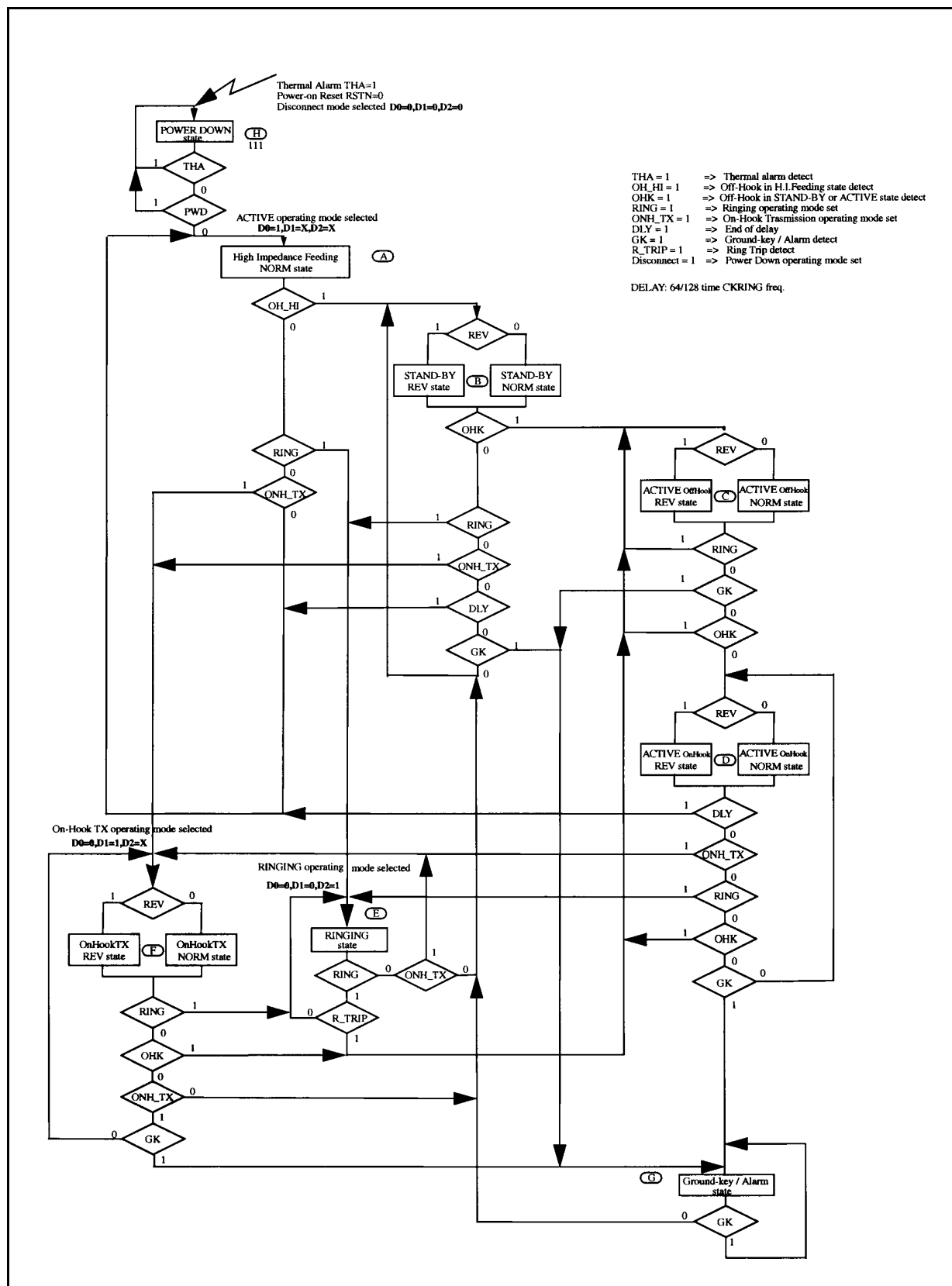
If, during WTIME, OHK=High is detected Off Hook, the state is returned to C) , i.e. Active with \overline{DET} =Low.

E) Ringing mode is set when D0 = D1 = 0 and D2 = 1. After ring trip detection the SLIC is automatically set in Active state (reverse or normal polarity according to D2 value set before ringing mode). Ring trip detection is indicated by DET pin: when it happens the SW must remove the ringing mode word (001) and set the Active mode word (100).

F) On-Hook Tx mode is selected when D0 = 0, D1 = 1 and D2 = X.

After Off Hook detection the SLIC is automatically set in Active state.

Figure A1.



APPENDIX B

STLC3080: allowed Rfeed values vs. Ilim

The STLC3080 device has been designed in order to fit in a small SMD package (TQFP44). This target has been achieved by using a dedicated circuit for power management based on one external transistor (Qext).

The particular power management circuit adopted allows to define the percentage of power dissipated on the SLIC itself and on the Qext. The sharing percentage is defined by the Rfeed value, in particular the higher is Rfeed, the higher is the percentage dissipated on the SLIC.

Rfeed represents the DC feeding impedance at TIP/RING terminals (including 2xRp) when the SLIC is in the resistive feed region of the DC characteristics.

Since the max. power dissipation inside the SLIC is limited it is important to know which value of Rfeed can be implemented without exceeding the max power allowed in the SLIC.

In order to define the allowed Rfeed values several other parameters should be considered, in particular:

Pdslic:

Max allowed power dissipation on SLIC, two values are considered:

- 1.1W for 70°C T_{amb} application;
- 0.9W for 85°C T_{amb} application;

Pdqext:

Max allowed power dissipation on Qext, three values are considered:

- 1.0W

- 1.5W
- 2.0W

These values depend on the package and the assembly of the Qext.

Ilim:

Programmed constant current value, continuous variations are considered from 20mA to 50mA.

Vbat:

Battery voltage, three values are considered:

- 48V
- 54V
- 62V

The following diagrams show the allowed Rfeed values depending on the above parameters. three diagrams are shown each one for a particular battery (Vbat = -48V, -54V, -60V).

In each diagrams you can find an upper and a lower limits for the Rfeed value:

The upper limit is defined by one of the two b1, b2 curves.

- b1 is the limit when max. power on SLIC is equal to 0.9W (T_{amb} = 85°C)
- b2 is the limit when max. power on SLIC is equal to 1.1W (T_{amb} = 70°C)

The lower limit is defined by one of the three a1, a2, a3 curves.

- a1 is the limit when max. power allowed on Qext is equal to 1.0W
- a2 is the limit when max. power allowed on Qext is equal to 1.5W
- a3 is the limit when max. power allowed on Qext is equal to 2.0W

Figure B1. Rfeed allowed values vs. Ilim (Vbat = -48V).

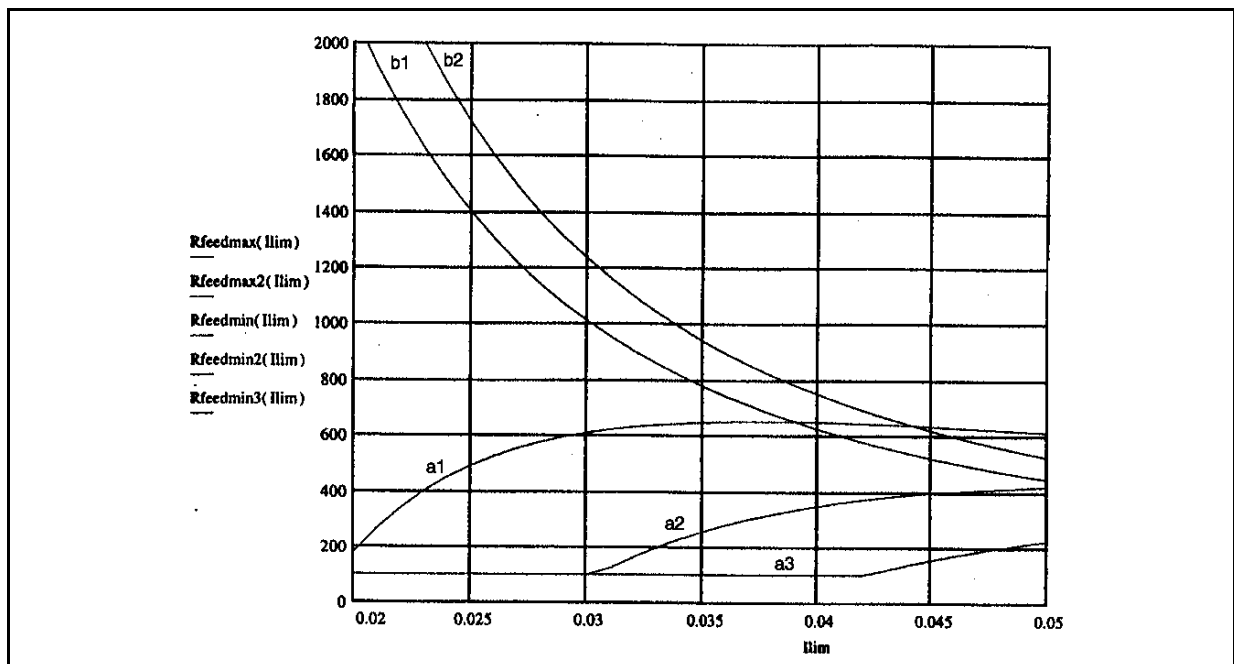


Figure B2. Rfeed allowed values vs. Ilim (Vbat = -54V).

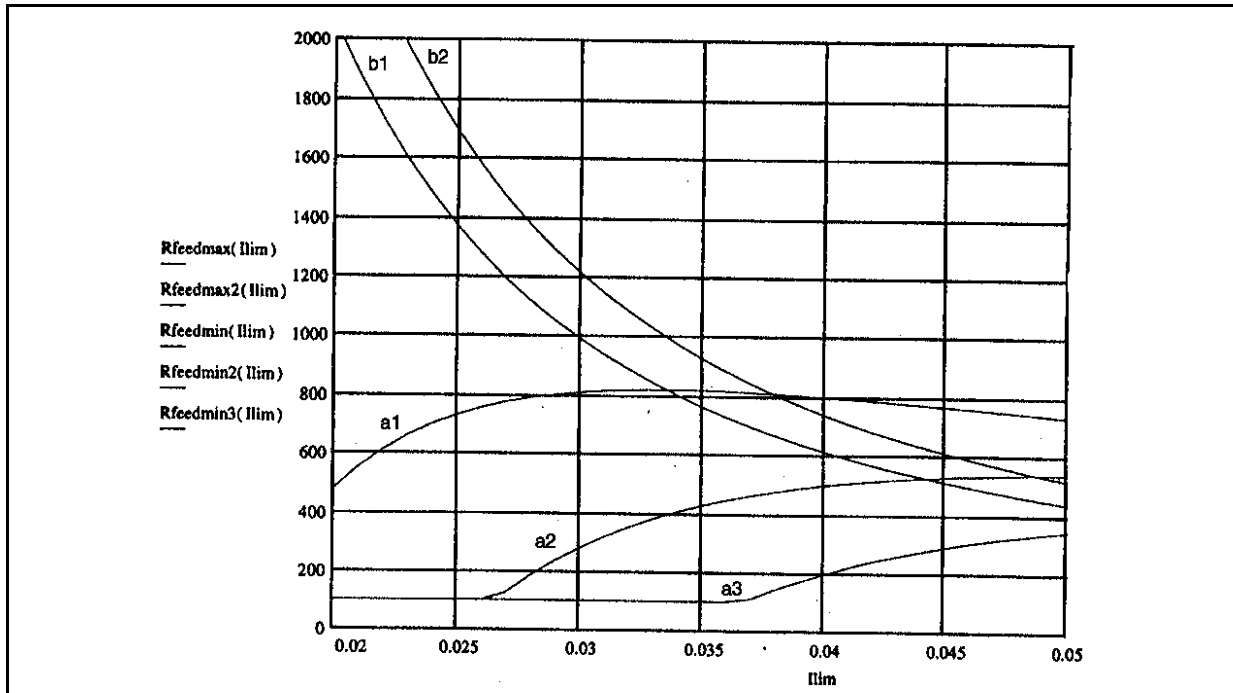
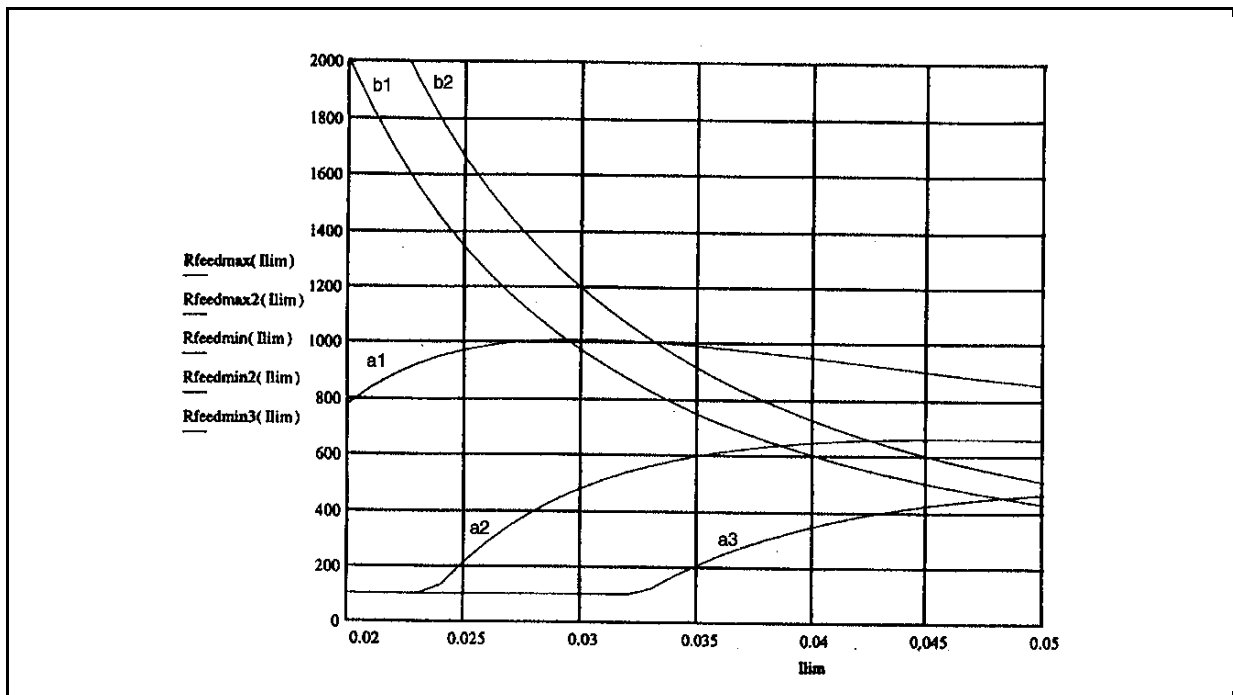


Figure B3. Rfeed allowed values vs. Ilim (Vbat = -60V).



EXAMPLE:

Considering the following parameters:
 Vbat = -48V, max Tamb = 70°C, Ilim = 25mA,
 Qext able to dissipate 1W, the possible values of
 Rfeed can be found in fig. 1 and are limited by the

b2 curve (upper limit) and the a1 curve (lower
 limit).

In particular considering the Ilim = 25mA the
 Rfeed allowed range will be:

$$500\Omega < R_{\text{feed}} < 1700\Omega$$



APPENDIX C

STLC3080 Test Circuits referring to the application diagram shown in figure 4 and using as external components the typ. values specified in the

"External Components", find below the proper configuration for each measurement.

Figure C1. Receive Gain.

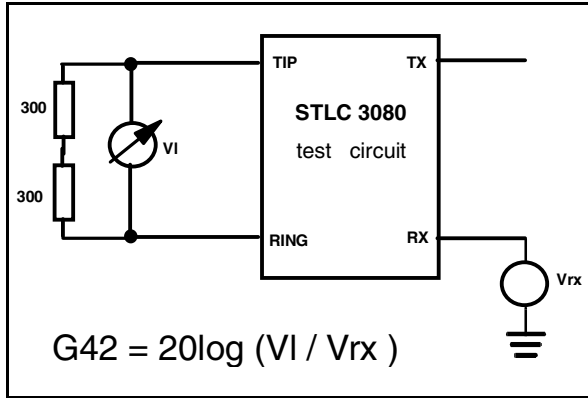


Figure C2. THL Trans Hybrid Loss.

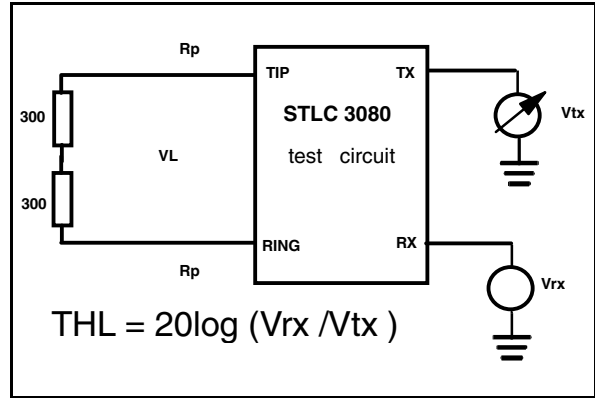


Figure C3. T/L Transversal to Longitudinal Conversion

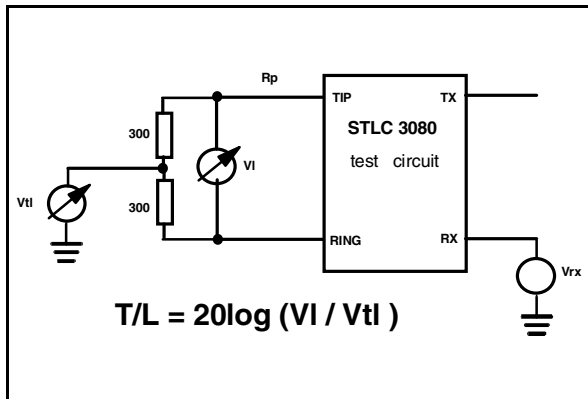


Figure C4. Transmit Gain.

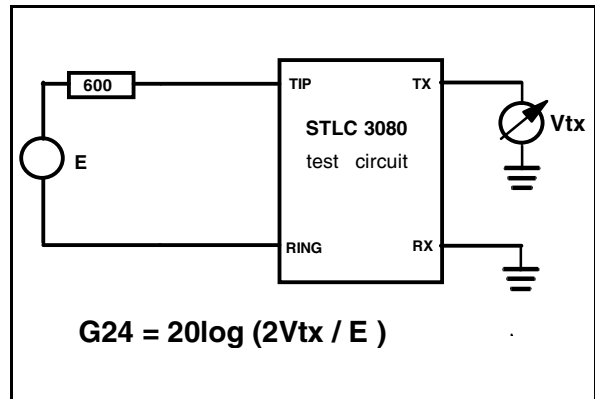


Figure C5. L/T Longitudinal to transversal Conversion.

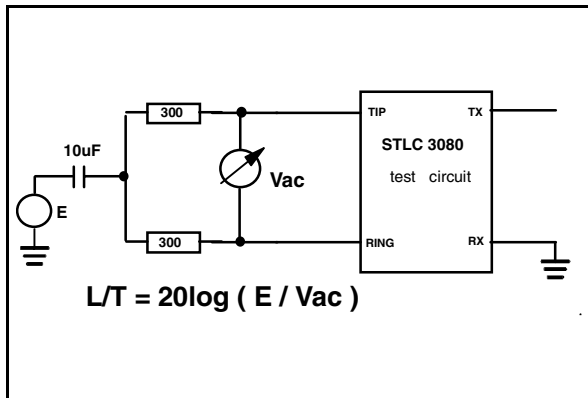


Figure C6. 2W Return Loss.

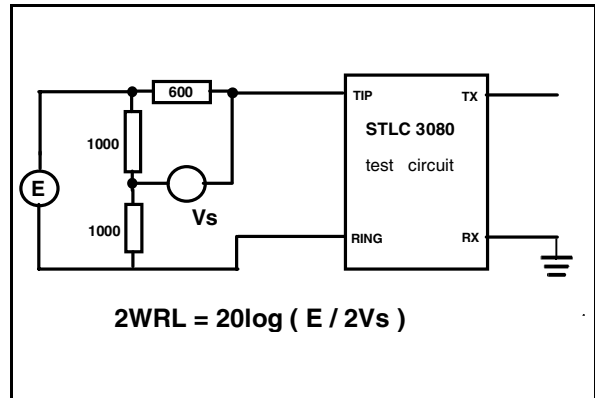


Figure C7. Idle channel psophometric noise at TX port.

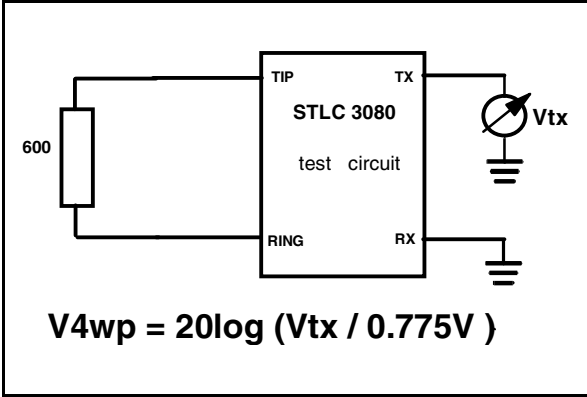


Figure C8. Idle channel psophometric noise at line terminals.

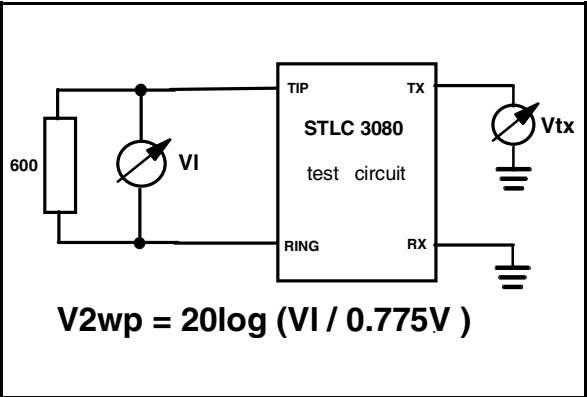
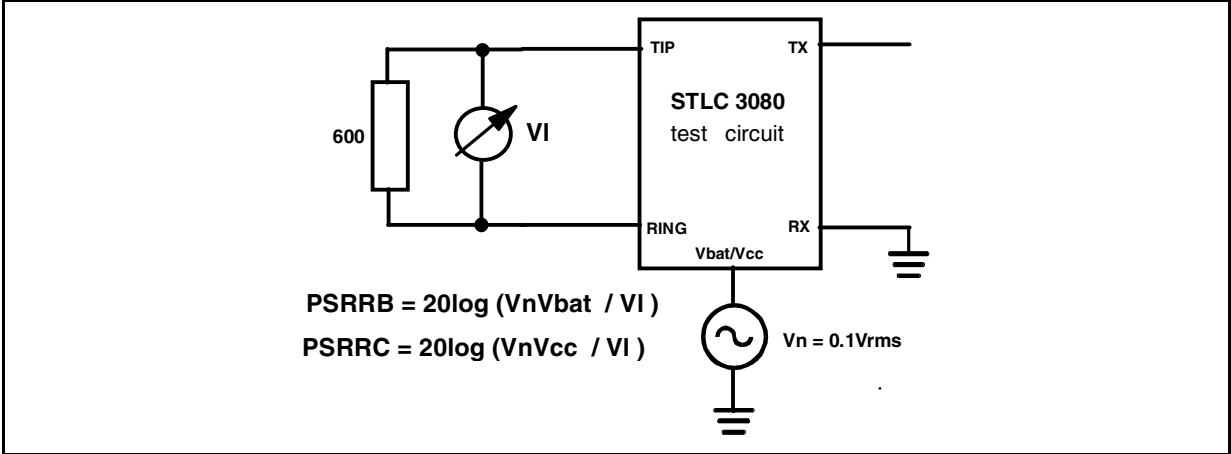


Figure C9. PSRRB = Power Supply Rejection Vcc to 2W Port
PSRRB = Power Supply Rejection VBAT to 2W Port



APPENDIX D RINGING MODE AND RING TRIP DETECTION

In ringing mode the STLC3080 provides:

- Relay driver capability (relay is synchronized with low level of CKRING)
- Ring-Trip detection

The monitor of the line state is performed by sensing the line current converted into a voltage drop across the RR resistor connected in series to the line. This voltage is read via RS1 and RST2 input pins of a differential stage that identifies, during the ringing phase, the ON/OFF HOOK state of the line (see Fig. D1).

The Ring-Trip condition is detected by sensing the DC component of the line current, rejecting the AC component. With $RR = 600\Omega$ the Ring-Trip threshold is: $I_{line} > 7.5mA$

When the Ring-Trip is detected, the STLC3080:

- deactivates the ringing relay RELR (if CKRING is low);
- indicates the ring-trip detection by setting DET=low;
- forces the Active state.

The information at RELR and DET pins is latched and it doesn't change opening the current loop. To reset the latched informations the Active or On-Hook Transmission mode have to be entered (in general changing the device mode the latched information is removed).

Although the ring-trip detection sets DET to signal the line status, there is a substantial difference respect to the on/off-hook detection. In Ringing mode on-hook condition, an AC current is present on the line. The ring-trip detector rejects the AC

component by integrating the line current: the detection threshold can be reached only if the line current has a DC component higher than the threshold. As a consequence the response is not immediate (as it is for off-hook in Active state): it takes an amount of time that is dependent on the DC current value (i.e. on the line length). The AC rejection and the delay depend on the CRT capacitor value (see Fig.D1).

When the voltage on the capacitor exceeds 3V, the Ring-Trip is detected (see fig.D3). CRT should be selected in order to avoid that during one half sinewave cycle, in on-hook, its voltage VCRT exceeds 3V (ring-trip threshold). The minimum value of CRT can be carried out with the following formula:

$$C_{crt} > 6\mu F / Fring$$

With $Fring = 20Hz$, you obtain a $C_{crt} = 390nF$.

When the CRT capacitor is selected, it must be considered that it is also used for the rejection of the common mode current. In this case the minimum value of the CRT capacitor can be carried out with the following formula:

$$C_{crt} > (I_p / f_l) \cdot 560\mu F$$

Where I_p is the peak of the longitudinal current and f_l is the frequency of this current. With $I_p = 25mA$ @ $f_l = 50Hz$ you obtain $330nF$.

For this reasons the suggested value for typical central office application is $470nF$.

Figure D1.ring trip circuit block diagram.

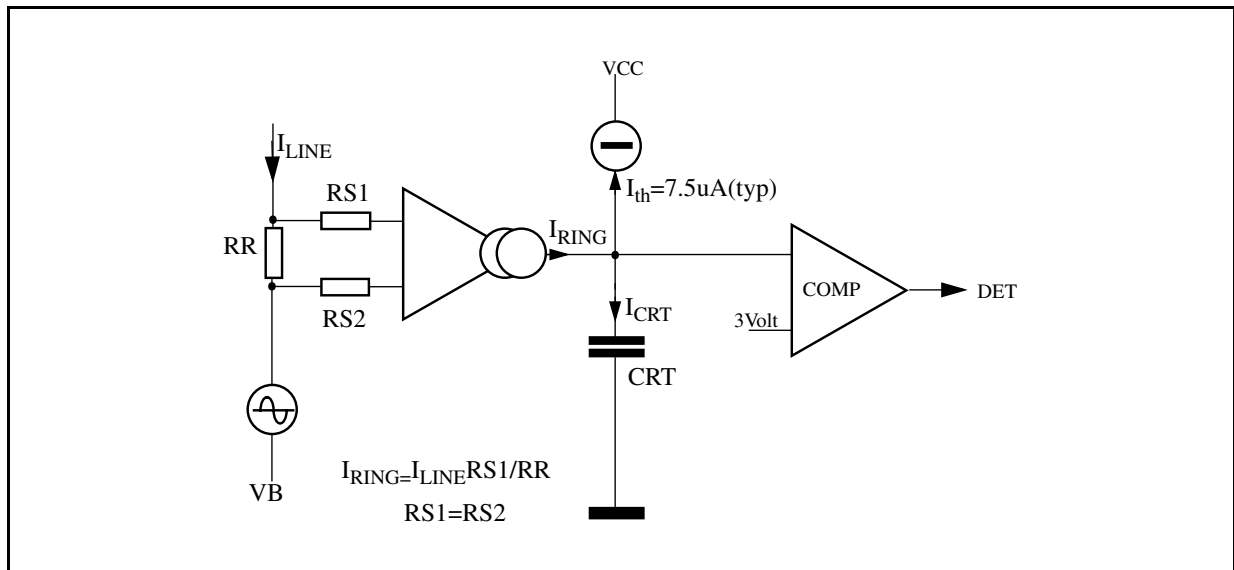
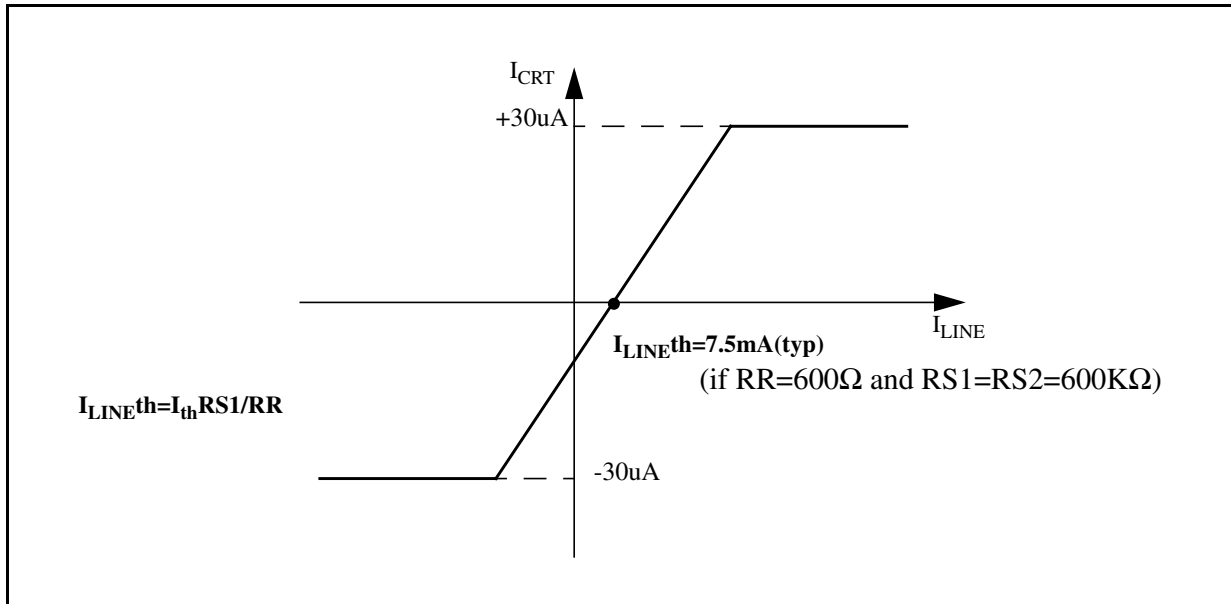


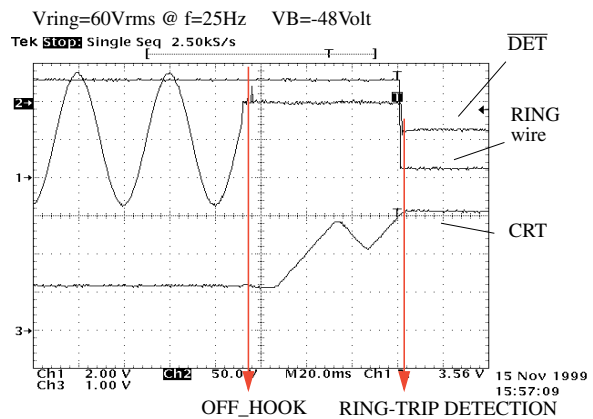
Figure D2. relation between I_{CRT} and I_{LINE} .



RS1 must be connected to the positive RR; RR should be connected directly to the ringing generator as it is in the figure. The ratio between RS1 and RR must be chosen considering that there is an offset current in the input stage equal to $7.5\mu A$. This offset has been introduced to take in account the leakage current of the line.

In fig.D2 is shown the relation between the CRT charging current I_{CRT} and the line current I_{LINE} . In the range $-30\mu A < I_{CRT} < +30\mu A$ I_{CRT} is proportional to I_{LINE} while it remains limited to $\pm 30\mu A$ for higher value of I_{LINE} . Consequently, in case of short loops, the ring-trip detection time is independent on the loop resistance, as the CRT charging is performed at a fixed current. In case of long loops the detection time will increase as the I_{CRT} decreases proportionally to the loop resistance.

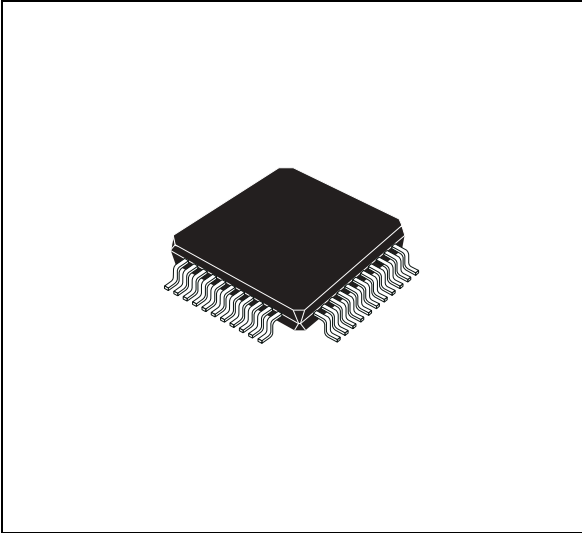
Figure D3. Ring Trip detection signals.



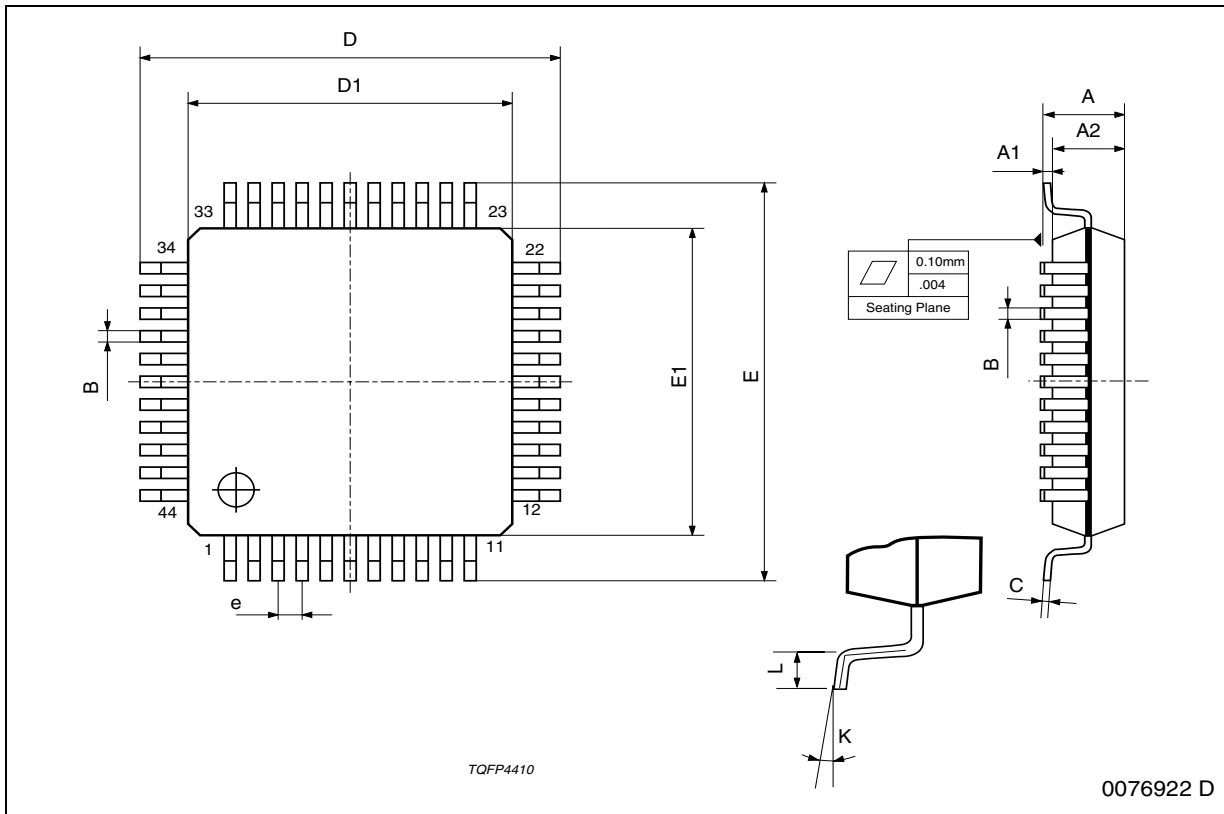
STLC3080

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0° (min.), 3.5° (typ.), 7° (max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10 x 1.4mm)



ESD - The STMicroelectronics Internal Quality Standards set a target of 2 KV that each pin of the device should withstand in a series of tests based on the Human Body Model (MIL-STD 883 Method 3015): with $C = 100\text{pF}$; $R = 1500\Omega$ and performing 3 pulses for each pin versus V_{CC} and GND.

Device characterization showed that, in front of the STMicroelectronics Internal Quality Standards, all pins of STLC3080 withstand at least 1000V. One particular pin (pin N° 41) withstand 500V only.

The above points are not expected to represent a practical limit for the correct device utilization nor for its reliability in the field. Nonetheless they must be mentioned in connection with the applicability of the different SURE 6 requirements to STLC3080.

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