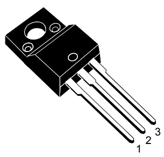
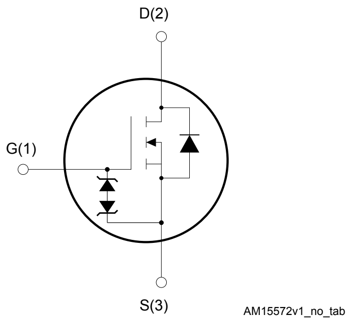
STF18N60M2(045Y)

Datasheet

N-channel 600 V, 0.255 Ω typ., 13 A MDmesh M2 Power MOSFET in a TO-220FP narrow leads package



TO-220FP narrow leads



Features

Order code	V_{DS} @T_{Jmax}	$R_{DS(on)}$ max.	I_D
STF18N60M2(045Y)	650 V	0.280 Ω	13 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LCC converters
- Resonant converters

Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Product status link
STF18N60M2(045Y)

Product summary	
Order code	STF18N60M2(045Y)
Marking	18N60M2
Package	TO-220FP narrow leads
Packing	Tube

1 Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	13	A
	Drain current (continuous) at T_C = 100 °C	8	A
I_{DM} (2)	Drain current (pulsed)	52	A
P_{TOT}	Total power dissipation at T_C = 25 °C	25	W
dv/dt (3)	Peak diode recovery voltage slope	15	V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2.5	kV
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Limited by maximum junction temperature.*
2. *Pulse width limited by safe operating area.*
3. $I_{SD} \leq 13$ *A, di/dt* ≤ 400 *A/µs;* $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400$ *V*
4. $V_{DS} \leq 480$ *V*

Table 2. **Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	°C/W

Table 3. **Avalanche characteristics**

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	3	A
E_{AS}	Single pulse avalanche energy (starting T_j=25 °C, I_D= I_{AR}, V_{DD}=50 V)	135	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6.5 A		0.255	0.280	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	791	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Reverse transfer capacitance		-	1.3	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	164.5	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	5.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 13 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	21.5	-	nC
Q_{gs}	Gate-source charge		-	3.2	-	nC
Q_{gd}	Gate-drain charge		-	11.3	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 6.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	12	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	47	-	ns
t_f	Fall time		-	10.6	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		13	A
I_{SDM} (1)	Source-drain current (pulsed)		-		52	A
V_{SD} (2)	Forward on voltage	I_{SD} = 13 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 13 A, di/dt = 100 A/μs	-	305		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	3.3		μC
I_{RRM}	Reverse recovery current		-	22		A
t_{rr}	Reverse recovery time	I_{SD} = 13 A, di/dt = 100 A/μs	-	417		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_j = 150 °C	-	4.6		μC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	22		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 μs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

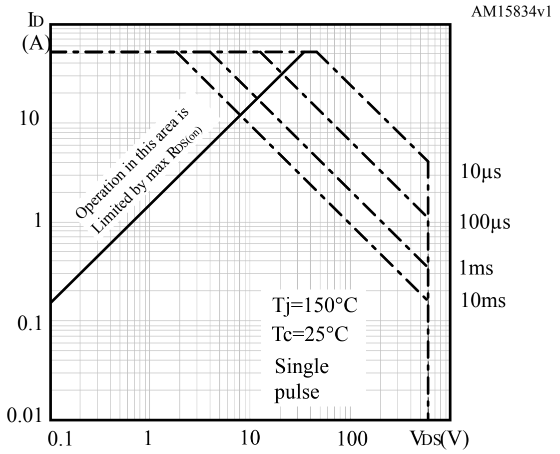


Figure 2. Thermal impedance

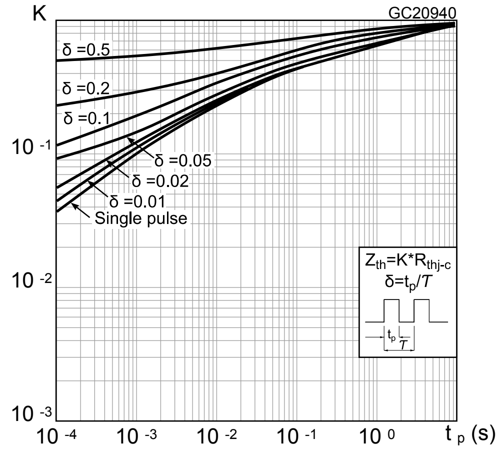


Figure 3. Output characteristics

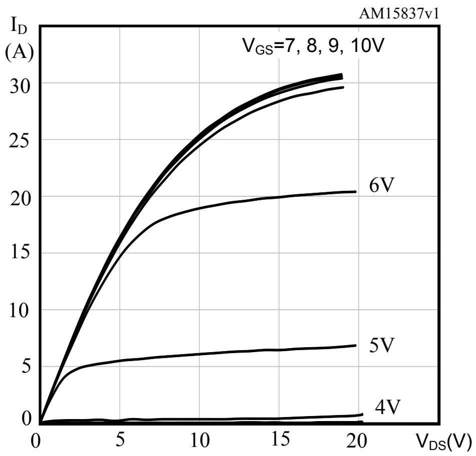


Figure 4. Transfer characteristics

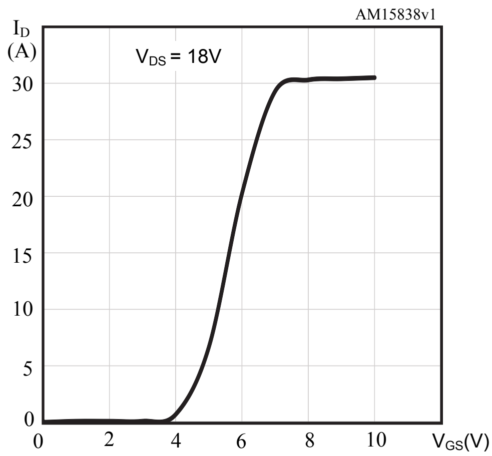


Figure 5. Gate charge vs gate-source voltage

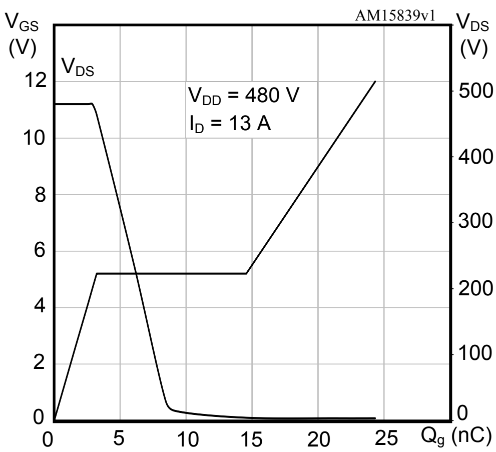


Figure 6. Static drain-source on-resistance

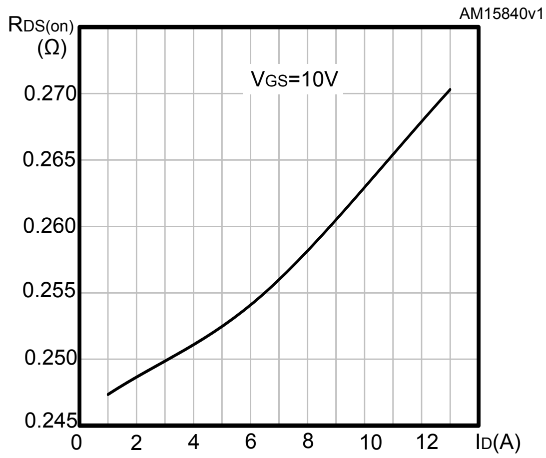


Figure 7. Capacitance variations

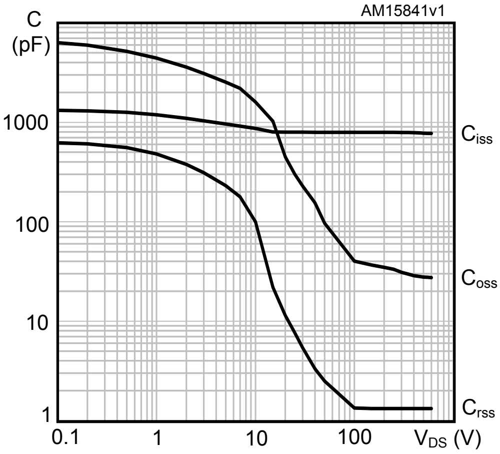


Figure 8. Normalized gate threshold voltage vs. temperature

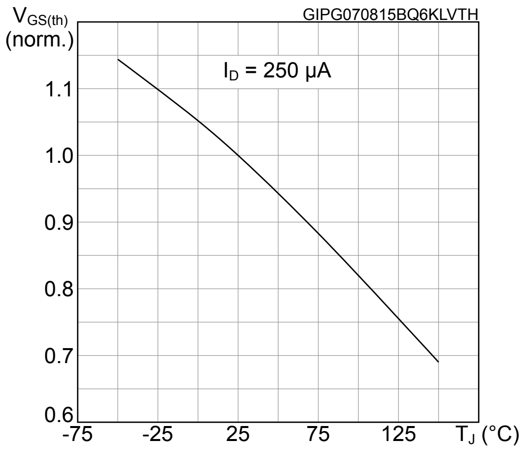


Figure 9. Normalized on-resistance vs temperature

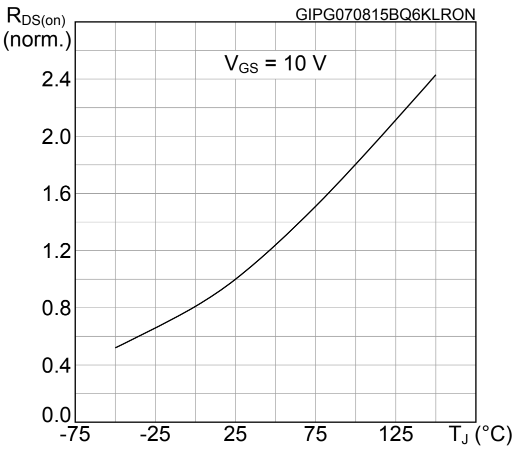


Figure 10. Source-drain diode forward characteristics

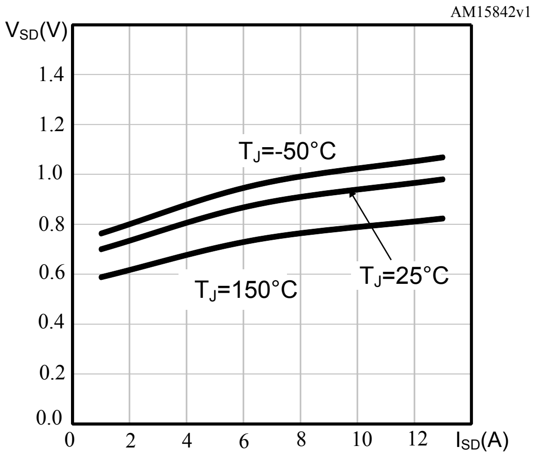


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

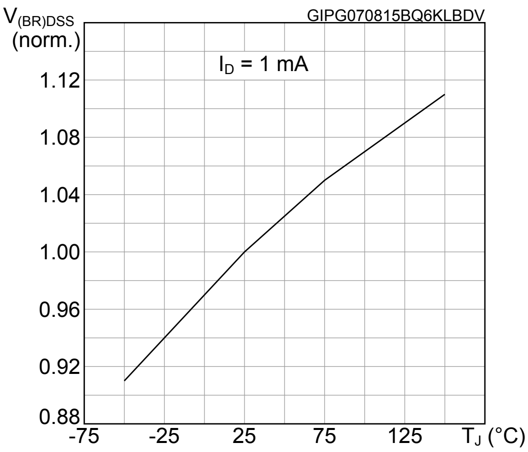
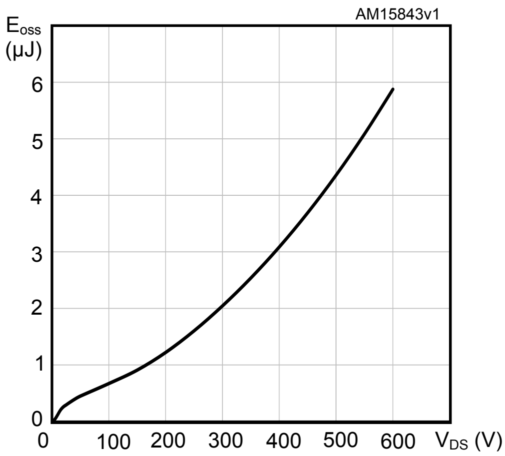


Figure 12. Output capacitance stored energy



3 Test circuits

Figure 13. Test circuit for resistive load switching times

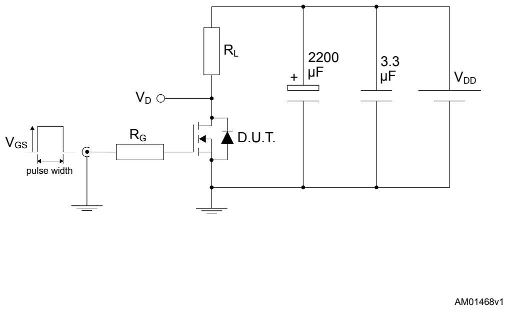


Figure 14. Test circuit for gate charge behavior

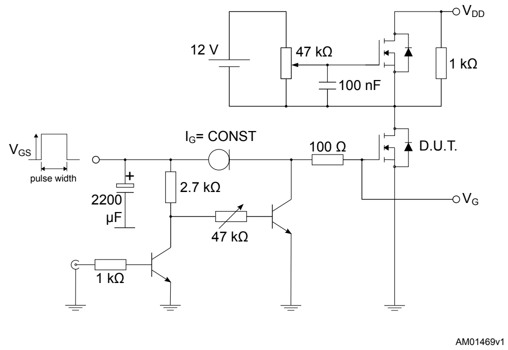


Figure 15. Test circuit for inductive load switching and diode recovery times

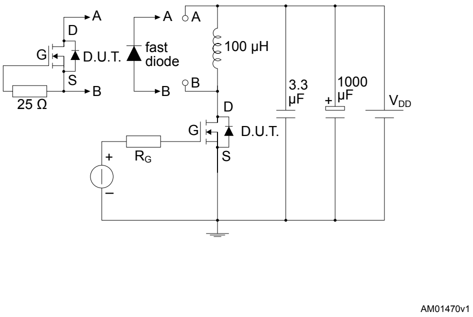


Figure 16. Unclamped inductive load test circuit

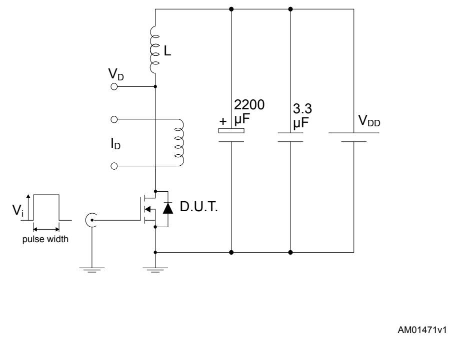


Figure 17. Unclamped inductive waveform

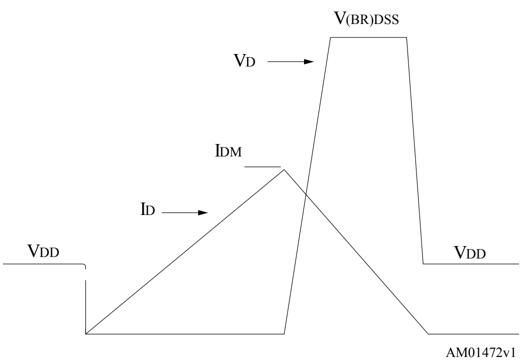
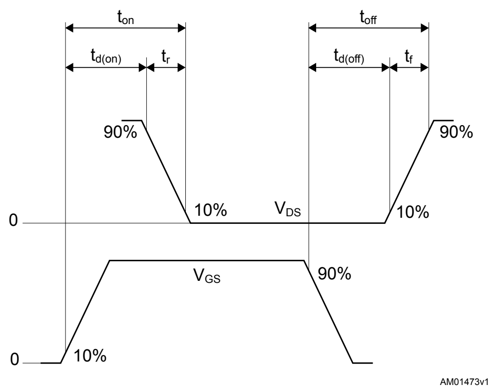


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP narrow leads package information

Figure 19. TO-220FP narrow leads package outline

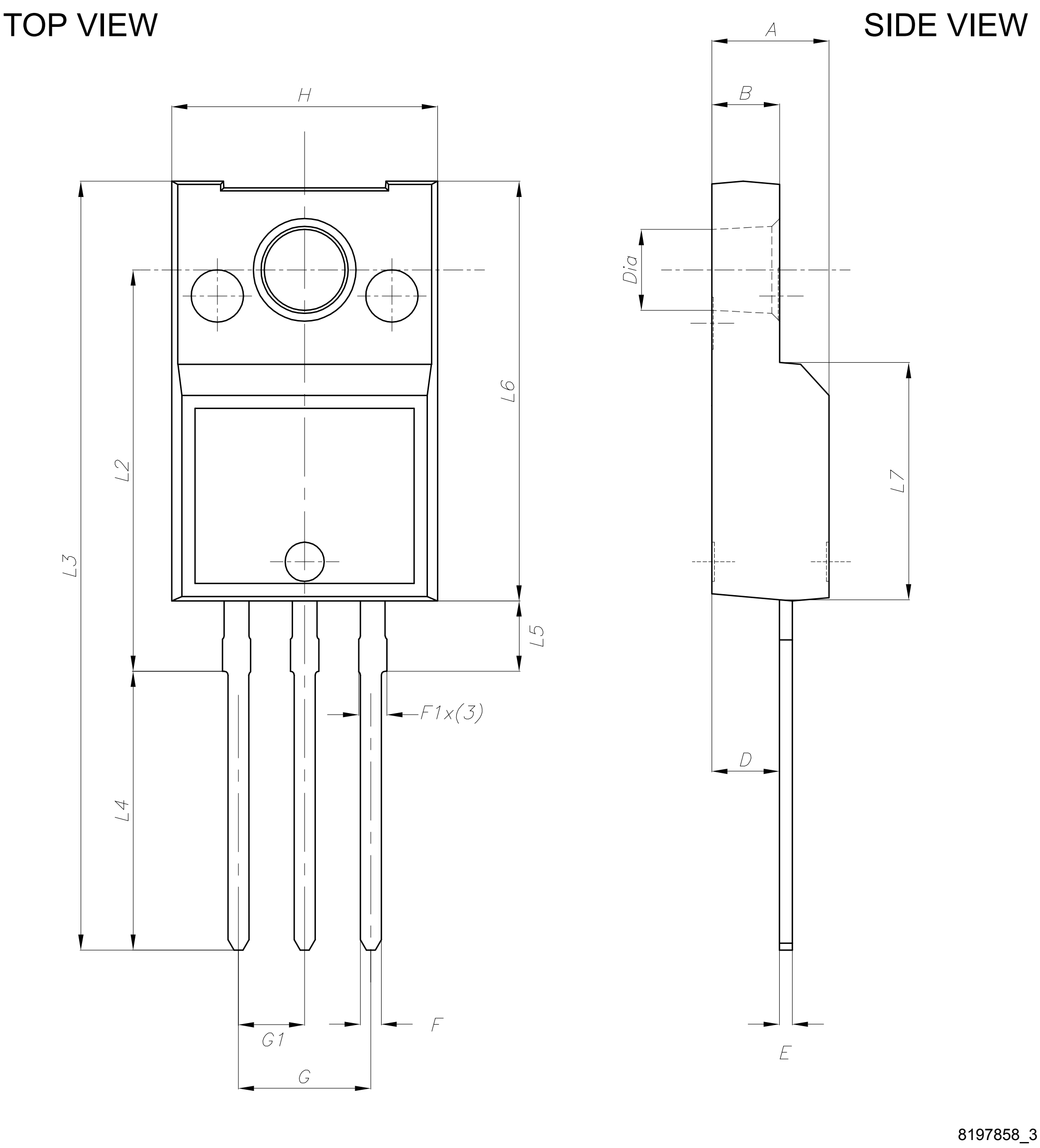


Table 8. TO-220FP narrow leads package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	0.95		1.20
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2	15.20		15.60
L3	28.60		30.60
L4	10.30		11.10
L5	2.60	2.70	2.90
L6	15.80	16.00	16.20
L7	9.00		9.30
Dia.	3.00		3.20

Revision history

Table 9. Document revision history

Date	Revision	Changes
27-May-2013	1	First release.
05-Jun-2013	2	– Added: *note 2* in *Table 2* – Modified: typical value for Ciss, Coss eq., Qg, Qgs, Qgd – Modified: *Figure 9* and *10* – Minor text changes
28-Feb-2014	3	– Modified: *note 1* in *Table 2* – $R_{thj\text{-}case}$ value in *Table 3* – Minor text changes
13-Jun-2019	4	Modified Section 1 Electrical ratings, Section 2 Electrical characteristics, Section 2.1 Electrical characteristics (curves). Updated Section 4.1 TO-220FP narrow leads package information. Minor text changes.

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