



MX27C2100/27C2048

2M-BIT [256Kx8/128x16] CMOS EPROM

FEATURES

- 128K x 16 organization(MX27C2048, JEDEC pin out)
- 256K x 8 or 128K x 16 organization(MX27C2100, ROM pin out compatible)
- +12.5V programming voltage
- Fast access time: 55/70/90/120/150 ns
- Totally static operation

- Completely TTL compatible
- Operating current: 40mA
- Standby current: 100uA
- Package type:
 - 40 pin plastic DIP
 - 44 pin PLCC(MX27C2048)
 - 40 pin TSOP(I)(MX27C2048)

GENERAL DESCRIPTION

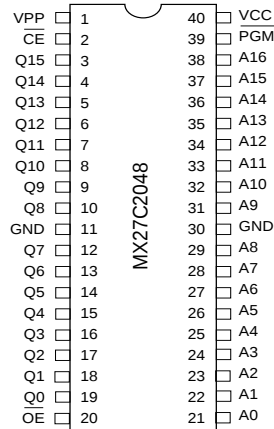
The MX27C2100/2048 is a 5V only, 2M-bit, One Time Programmable Read Only Memory. It is organized as 128K words by 16 bits per word(MX27C2048), 256K x 8 or 128K x 16(MX27C2100), operates from a single + 5 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM

programmers may be used. The MX27C2100/2048 supports a intelligent fast programming algorithm which can result in programming times of less than one minute.

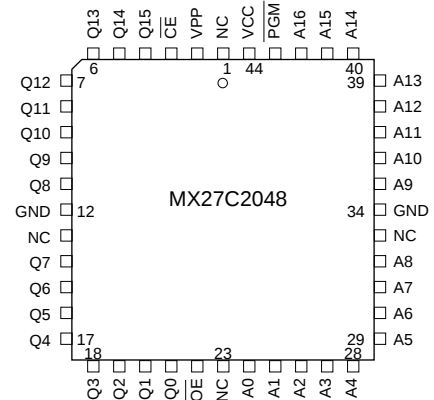
This EPROM is packaged in industry standard 40 pin dual-in-line packages, 44 lead PLCC, and 40 lead TSOP(I) packages.

PIN CONFIGURATIONS

PDIP(MX27C2048)



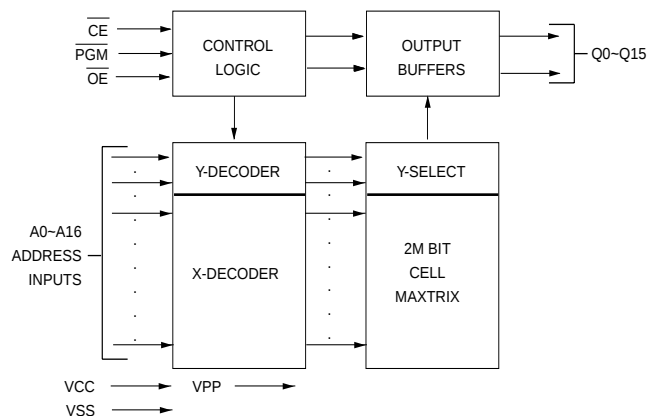
PLCC(MX27C2048)



40-TSOP(I)10x14mm (MX27C2048)



BLOCK DIAGRAM (MX27C2048)

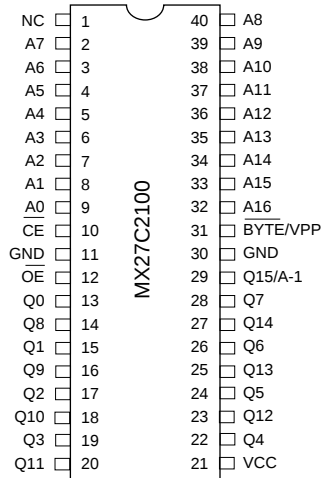




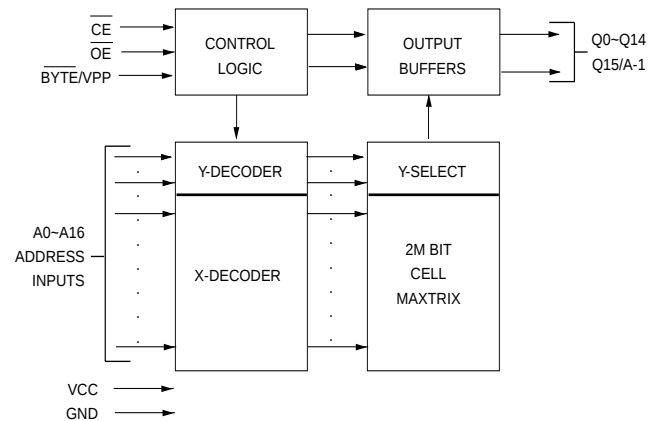
MX27C2100/27C2048

PIN CONFIGURATIONS

PDIP(MX27C2100)



BLOCK DIAGRAM (MX27C2100)



PIN DESCRIPTION(MX27C2100)

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q14	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
BYTE/VPP	Word/Byte Selection /Program Supply Voltage
Q15/A-1	Q15(Word mode)/LSB addr. (Byte mode)
VCC	Power Supply Pin (+5V)
GND	Ground Pin

PIN DESCRIPTION(MX27C2048)

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q15	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
PGM	Program Enable Input
VPP	Program Supply Voltage
VCC	Power Supply Pin (+5V)
GND	Ground Pin

TRUTH TABLE OF BYTE FUNCTION(MX27C2100)

BYTE MODE($\overline{BYTE} = \text{GND}$)

$\overline{CE}$	$\overline{OE}$	Q15/A-1	MODE	Q0-Q7	SUPPLY CURRENT
H	X	X	Non selected	High Z	Standby(ICC2)
L	H	X	Non selected	High Z	Operating(ICC1)
L	L	A-1 input	Selected	DOUT	Operating(ICC1)

WORD MODE($\overline{BYTE} = \text{VCC}$)

$\overline{CE}$	$\overline{OE}$	Q15/A-1	MODE	Q0-Q14	SUPPLY CURRENT
H	X	High Z	Non selected	High Z	Standby(ICC2)
L	H	High Z	Non selected	High Z	Operating(ICC1)
L	L	DOUT	Selected	DOUT	Operating(ICC1)

NOTE : X = H or L



FUNCTIONAL DESCRIPTION

THE PROGRAMMING OF THE MX27C2100/2048

When the MX27C2100/2048 is delivered, or it is erased, the chip has all 2M bits in the "ONE", or HIGH state. "ZEROS" are loaded into the MX27C2100/2048 through the procedure of programming.

For programming, the data to be programmed is applied with 16 bits in parallel to the data pins.

VCC must be applied simultaneously or before VPP, and removed simultaneously or after VPP. When programming an MXIC EPROM, a 0.1uF capacitor is required across VPP and ground to suppress spurious voltage transients which may damage the device.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage $VPP = 12.75V$ is applied, with $VCC = 6.25V$ and $PGM = VIL$ (or $OE = VIH$) (Algorithm is shown in Figure 1). The programming is achieved by applying a single TTL low level 100us pulse to the PGM input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at $VCC = VPP = 5V \pm 10\%$.

PROGRAM INHIBIT MODE

Programming of multiple MX27C2100/2048's in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX27C2100/2048 may be common. A TTL low-level program pulse applied to an MX27C2100/2048 $\overline{CE}$ input with $VPP = 12.5 \pm 0.5V$ will program the MX27C2100/2048. A high-level $\overline{CE}$ input inhibits the other MX27C2100/2048s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{OE}$ and $\overline{CE}$ at

VIL (for MX27C2048), $\overline{OE}$ at VIL , $\overline{CE}$ at VIH (for MX27C2100) and VPP at its programming voltage.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the $25^{\circ}C \pm 5^{\circ}C$ ambient temperature range that is required when programming the MX27C2100/2048.

To activate this mode, the programming equipment must force $12.0 \pm 0.5V$ on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH . All other address lines must be held at VIL during auto identify mode.

Byte 0 ($A0 = VIL$) represents the manufacturer code, and byte 1 ($A0 = VIH$), the device identifier code. For the MX27C2100/2048, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (Q15) defined as the parity bit.

READ MODE

The MX27C2100/2048 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$'s, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

WORD-WIDE MODE

With $BYTE/VPP$ at $VCC \pm 0.2V$ outputs Q0-7 present data Q0-7 and outputs Q8-15 present data Q8-15, after $\overline{CE}$ and $\overline{OE}$ are appropriately enabled.



BYTE-WIDE MODE

With BYTE/VPP at $GND \pm 0.2V$, outputs Q8-15 are tri-stated. If $Q15/A-1 = VIH$, outputs Q0-7 present data bits Q8-15. If $Q15/A-1 = VIL$, outputs Q0-7 present data bits Q0-7.

The location of the capacitor should be close to where the power supply is connected to the array.

STANDBY MODE

The MX27C2100/2048 has a CMOS standby mode which reduces the maximum VCC current to 100 μA . It is placed in CMOS standby when $\overline{CE}$ is at $VCC \pm 0.3 V$. The MX27C2100/2048 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH . When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between Vcc and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be used between VCC and GND for each eight devices.



MX27C2100/27C2048

MODE SELECT TABLE (MX27C2048)

MODE	PINS						
	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	VPP	OUTPUTS
Read	VIL	VIL	VIH	X	X	VCC	DOUT
Output Disable	VIL	VIH	VIH	X	X	VCC	High Z
Standby (TTL)	VIH	X	X	X	X	VCC	High Z
Standby (CMOS)	VCC $\pm$ 0.3V	X	X	X	X	VCC	High Z
Program	VIL	VIH	VIL	X	X	VPP	DIN
Program Verify	VIL	VIL	VIH	X	X	VPP	DOUT
Program Inhibit	VIH	X	X	X	X	VPP	High Z
Manufacturer Code(3)	VIL	VIL	X	VIL	VH	VCC	00C2H
Device Code(3)	VIL	VIL	X	VIH	VH	VCC	0122H

NOTES: 1. VH = 12.0 V $\pm$ 0.5 V
2. X = Either VIH or VIL

3. A1 - A8 = A10 - A16 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltage during programming.

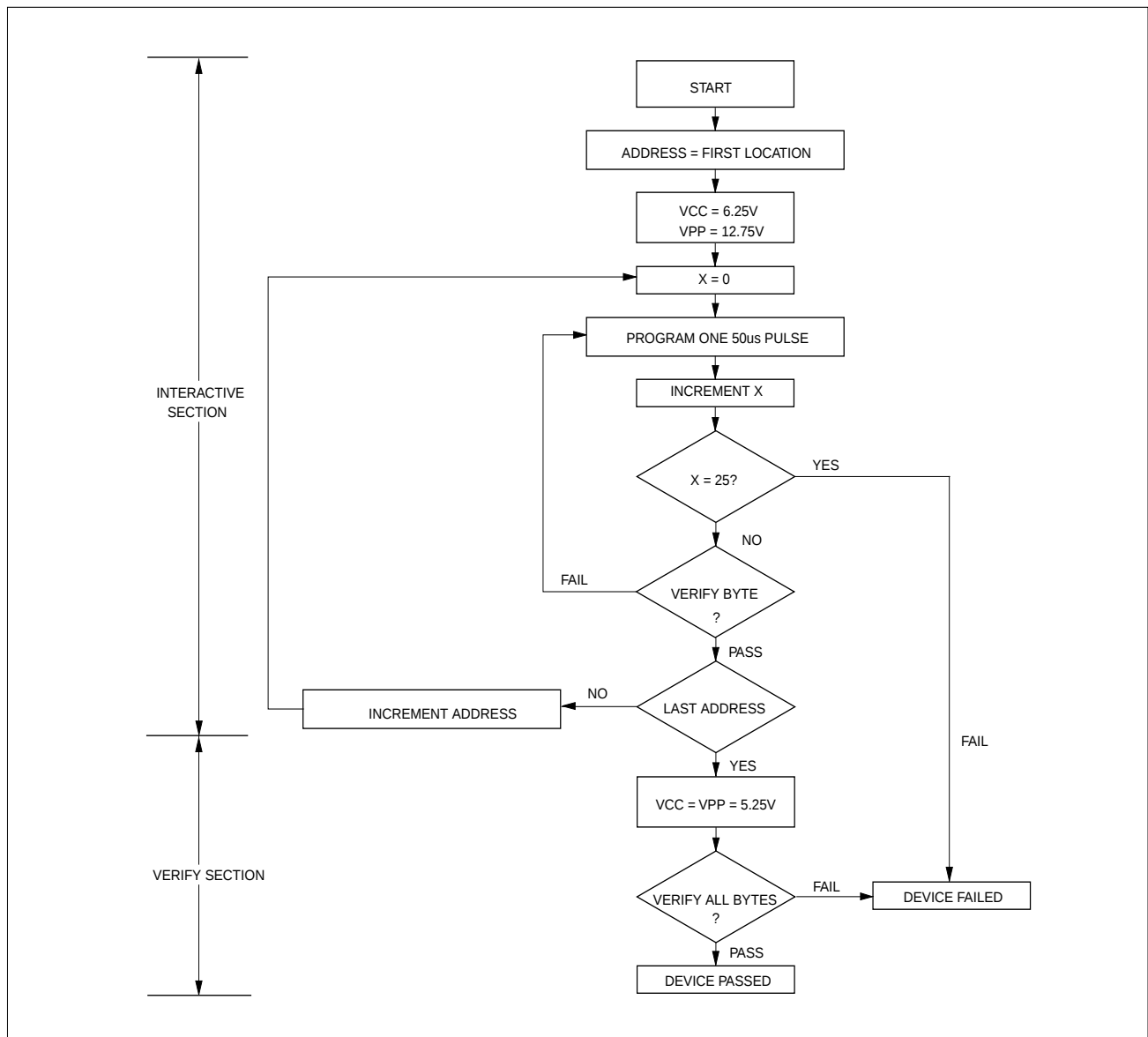
MODE SELECT TABLE (MX27C2100)

MODE	$\overline{BYTE/}$							
	$\overline{CE}$	$\overline{OE}$	A9	A0	Q15/A-1	VPP(5)	Q8-14	Q0-7
Read (Word)	VIL	VIL	X	X	Q15 Out	VCC	Q8-14 Out	Q0-7 Out
Read (Upper Byte)	VIL	VIL	X	X	VIH	GND	High Z	Q8-15 Out
Read (Lower Byte)	VIL	VIL	X	X	VIL	GND	High Z	Q0-7 Out
Output Disable	VIL	VIH	X	X	High Z	X	High Z	High Z
Standby	VIH	X	X	X	High Z	X	High Z	High Z
Program	VIL	VIH	X	X	Q15 In	VPP	Q8-14 In	Q0-7 In
Program Verify	VIH	VIL	X	X	Q15 Out	VPP	Q8-14 Out	Q0-7 Out
Program Inhibit	VIH	VIH	X	X	High Z	VPP	High Z	High Z
Manufacturer Code(3)	VIL	VIL	VH	VIL	0B	VCC	00H	C2H
Device Code(3)	VIL	VIL	VH	VIH	0B	VCC	01H	8AH

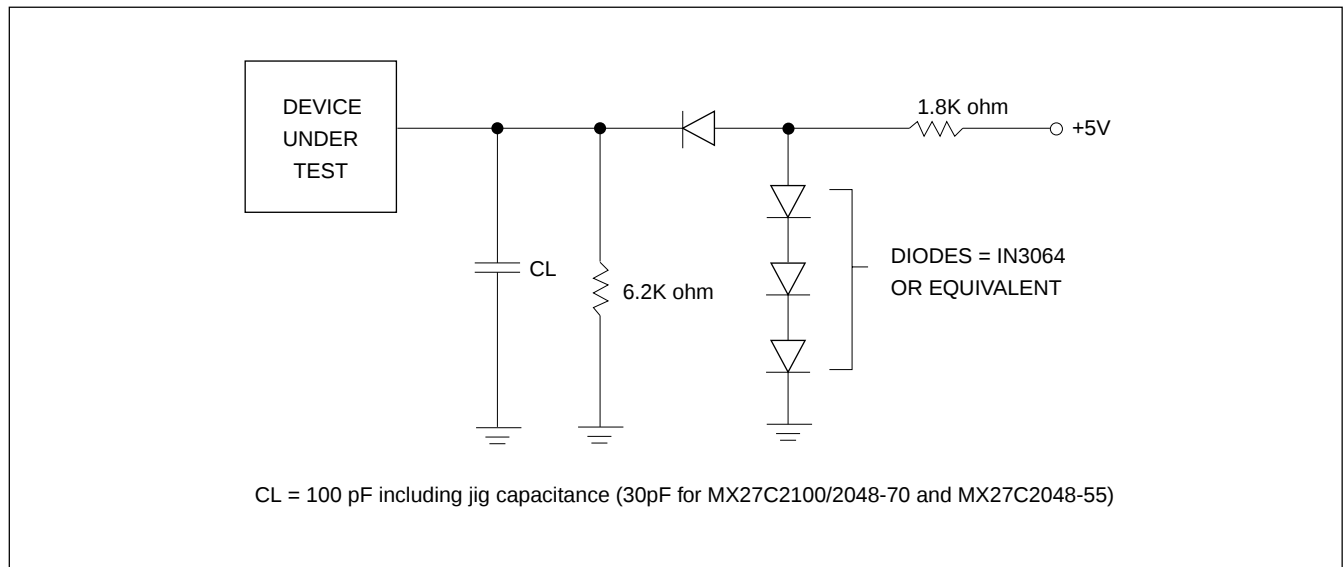
NOTES: 1. VH = 12.0V $\pm$ 0.5V
2. X = Either VIH or VIL.
3. A1 - A8, A10 - A16 = VIL(For auto select)

4. See DC Programming Characteristics for VPP voltages.
5. $\overline{BYTE/VPP}$ is intended for operation under DC Voltage conditions only.

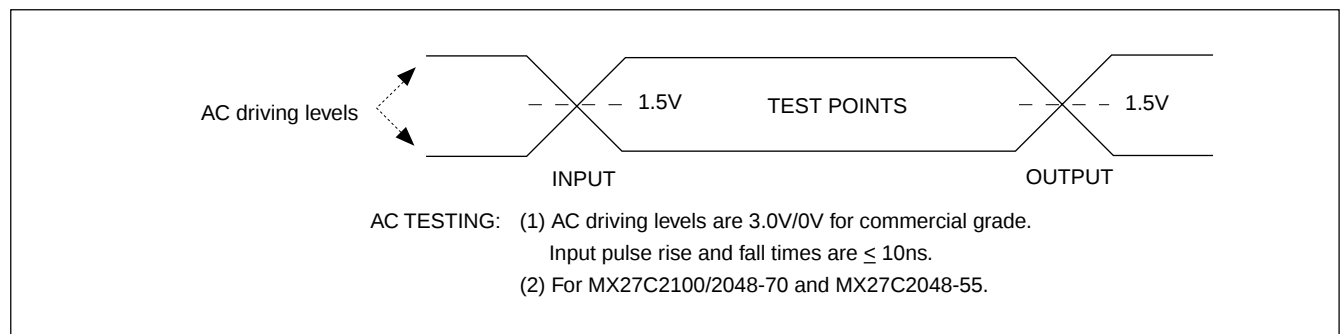
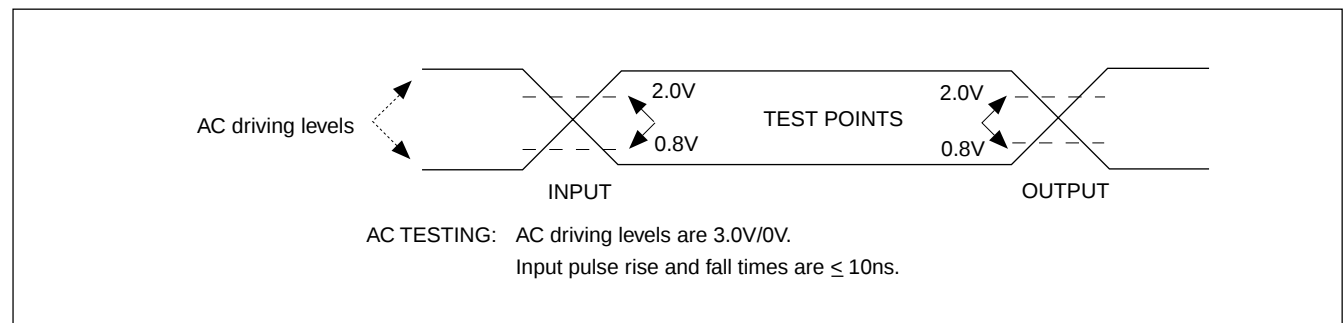
FIGURE 1. FAST PROGRAMMING FLOW CHART



SWITCHING TEST CIRCUITS



SWITCHING TEST WAVEFORMS





MX27C2100/27C2048

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & Vpp	-0.5V to 13.5V

NOTICE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:

Specifications contained within the following tables are subject to change.

DC/AC Operating Conditions for Read Operation

		MX27C2048		MX27C2100/2048		
		-55	-70	-90	-12	-15
Operating Temperature	Commercial	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C
Vcc Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	uA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	uA	$\overline{CE} = VCC \pm 0.3V$
ICC2	VCC Standby Current		1.5	mA	$\overline{CE} = VIH$
ICC1	VCC Active Current		40	mA	$\overline{CE} = VIL$, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		10	uA	$\overline{CE} = \overline{OE} = VIL$, VPP = 5.5V

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V



MX27C2100/27C2048

AC CHARACTERISTICS

SYMBOL	PARAMETER	2100/2048-55		2100/2048-70		2100/2048-90		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
tACC	Address to Output Delay		55		70		90	ns	$\overline{CE} = \overline{OE} = \text{VIL}$
tCE	Chip Enable to Output Delay		55		70		90	ns	$\overline{OE} = \text{VIL}$
tOE	Output Enable to Output Delay		30		30		40	ns	$\overline{CE} = \text{VIL}$
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	15	0	15	0	25	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		ns	

AC CHARACTERISTICS

SYMBOL	PARAMETER	2100/2048-12		2100/2048-15		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
tACC	Address to Output Delay		120		150	ns	$\overline{CE} = \overline{OE} = \text{VIL}$
tCE	Chip Enable to Output Delay		120		150	ns	$\overline{OE} = \text{VIL}$
tOE	Output Enable to Output Delay		50		65	ns	$\overline{CE} = \text{VIL}$
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	35	0	50	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		ns	

AC CHARACTERISTICS

SYMBOL	PARAMETER	27C2100-70		27C2100-90		27C2100-12		27C2100-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tBHA	$\overline{\text{BYTE}}$ Access Time		70		90		120		150	ns
tOHB	$\overline{\text{BYTE}}$ Output Hold Time	0		0		0		0		ns
tBHZ	$\overline{\text{BYTE}}$ Output Delay Time		70		70		70		70	ns
tBLZ	$\overline{\text{BYTE}}$ Output Set Time	10		10		10		10		ns



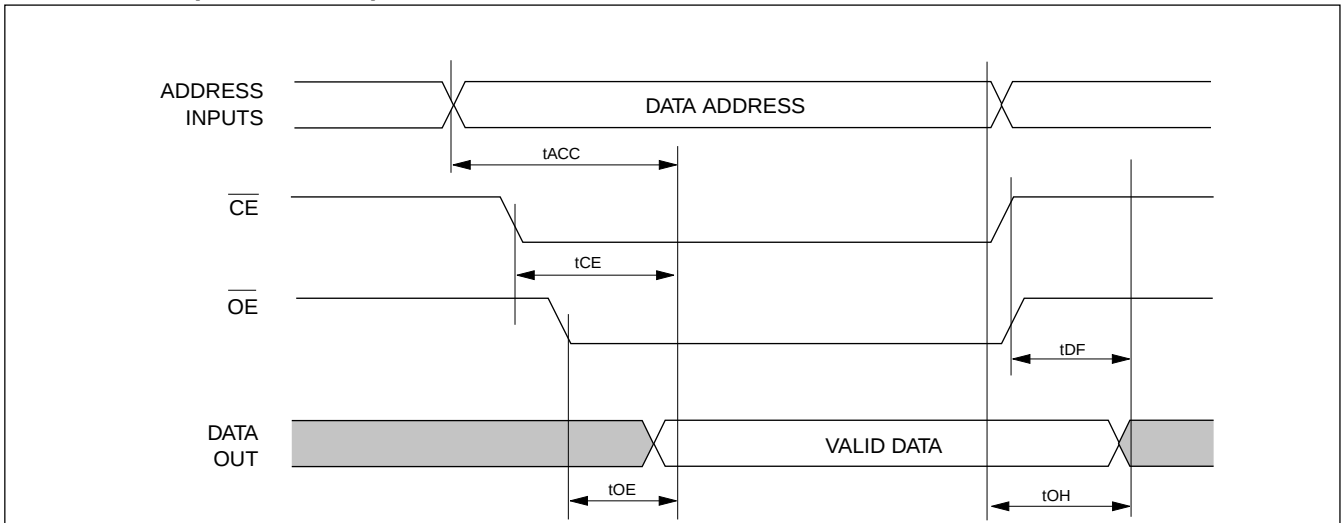
DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program & Verify)		50	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$
VCC1	Fast Programming Supply Voltage	6.00	6.50	V	
VPP1	Fast Programming Voltage	12.5	13.0	V	

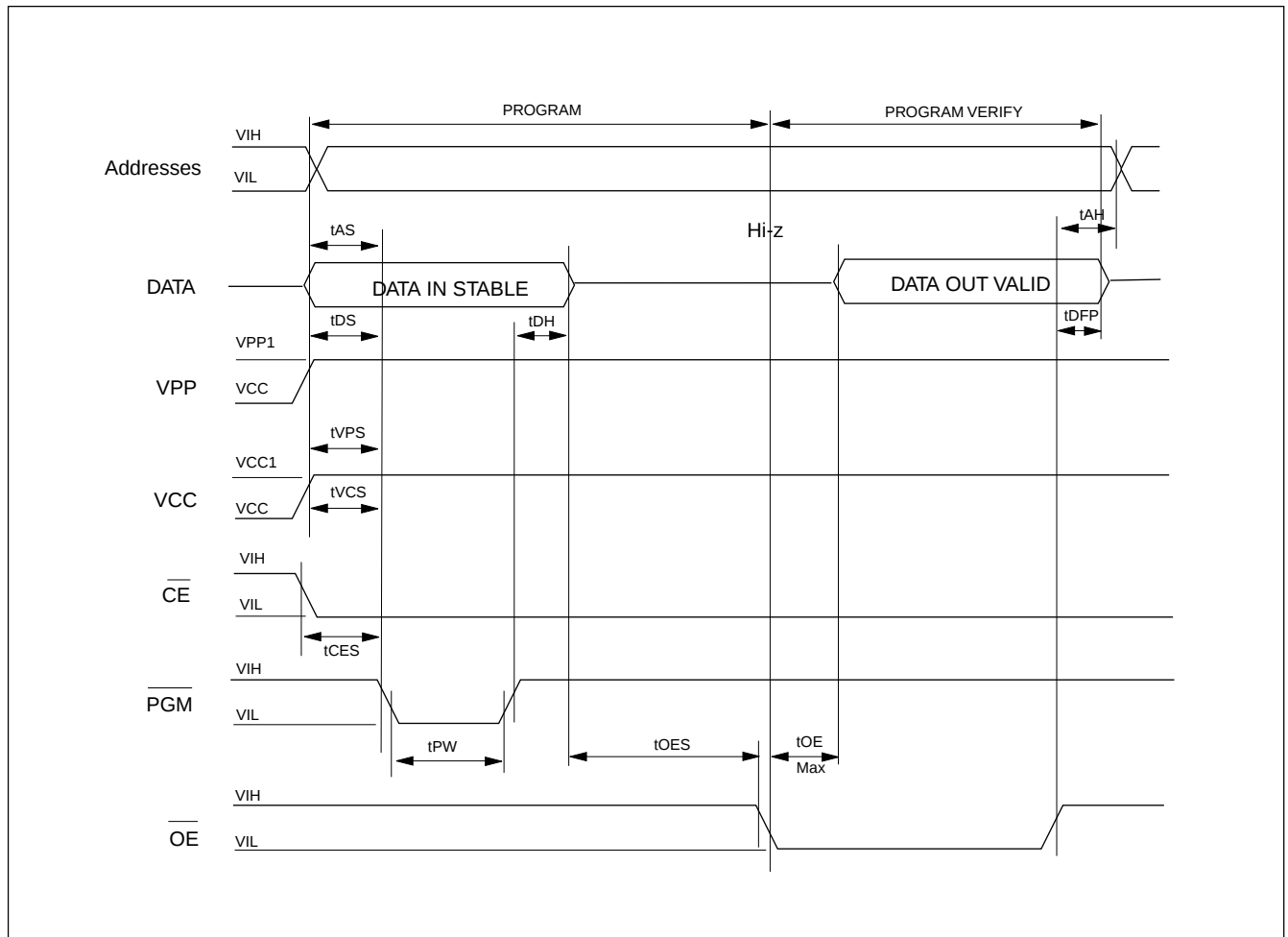
AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time	2.0		us	
tOES	$\overline{OE}$ Setup Time	2.0		us	
tDS	Data Setup Time	2.0		us	
tAH	Address Hold Time	0		us	
tDH	Data Hold Time	2.0		us	
tDFP	Out put Enable to Output Float Delay	0	130	ns	
tVPS	VPP Setup Time	2.0		us	
tPW	$\overline{PGM}$ Program Pulse Width	95	105	us	
tVCS	VCC Setup Time	2.0		us	
tCES	$\overline{CE}$ Setup Time	2.0		us	
tOE	Data valid from $\overline{OE}$		150	ns	

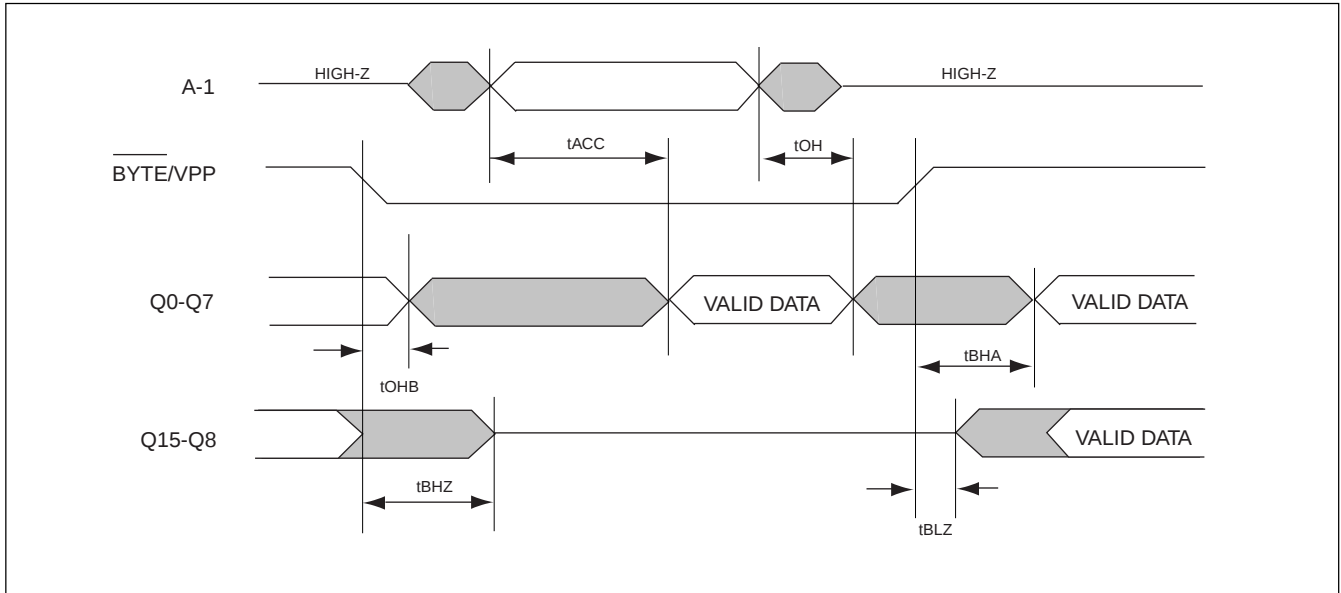
WAVEFORMS(MX27C2048) READ CYCLE (WORD MODE)



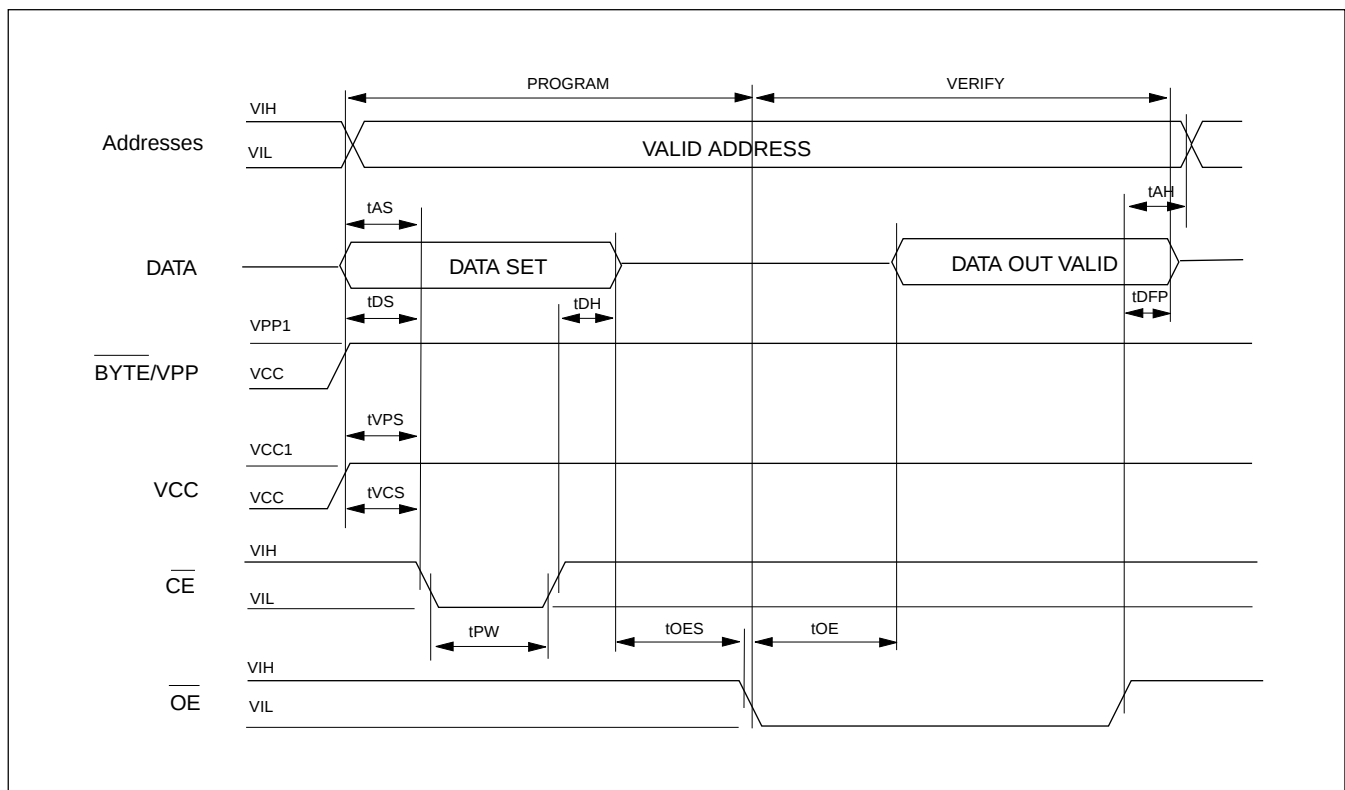
FAST PROGRAMMING ALGORITHM WAVEFORM



WAVEFORMS(MX27C2100) READ CYCLE (BYTE MODE)



FAST PROGRAMMING ALGORITHM WAVEFORM





MX27C2100/27C2048

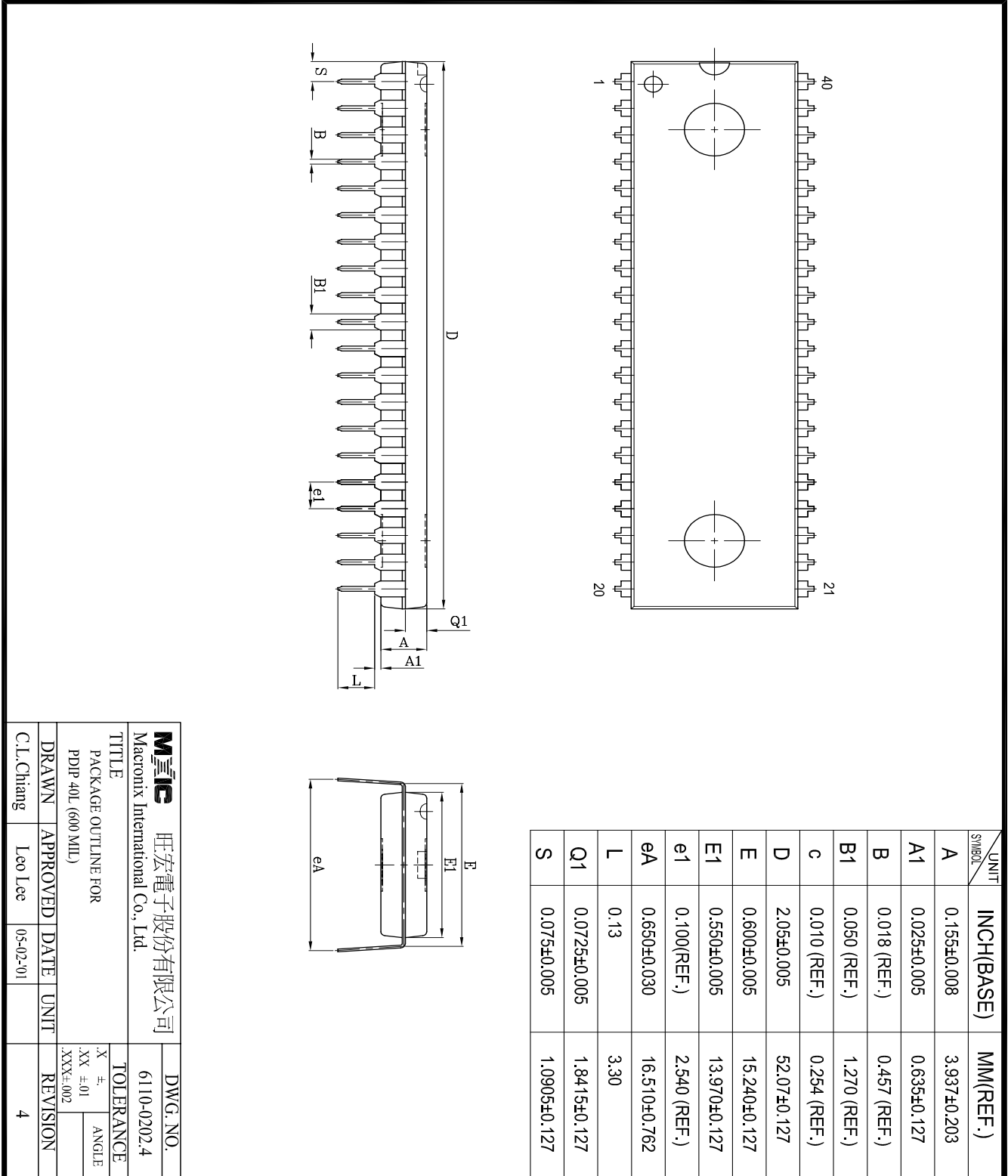
ORDERING INFORMATION

PLASTIC PACKAGE

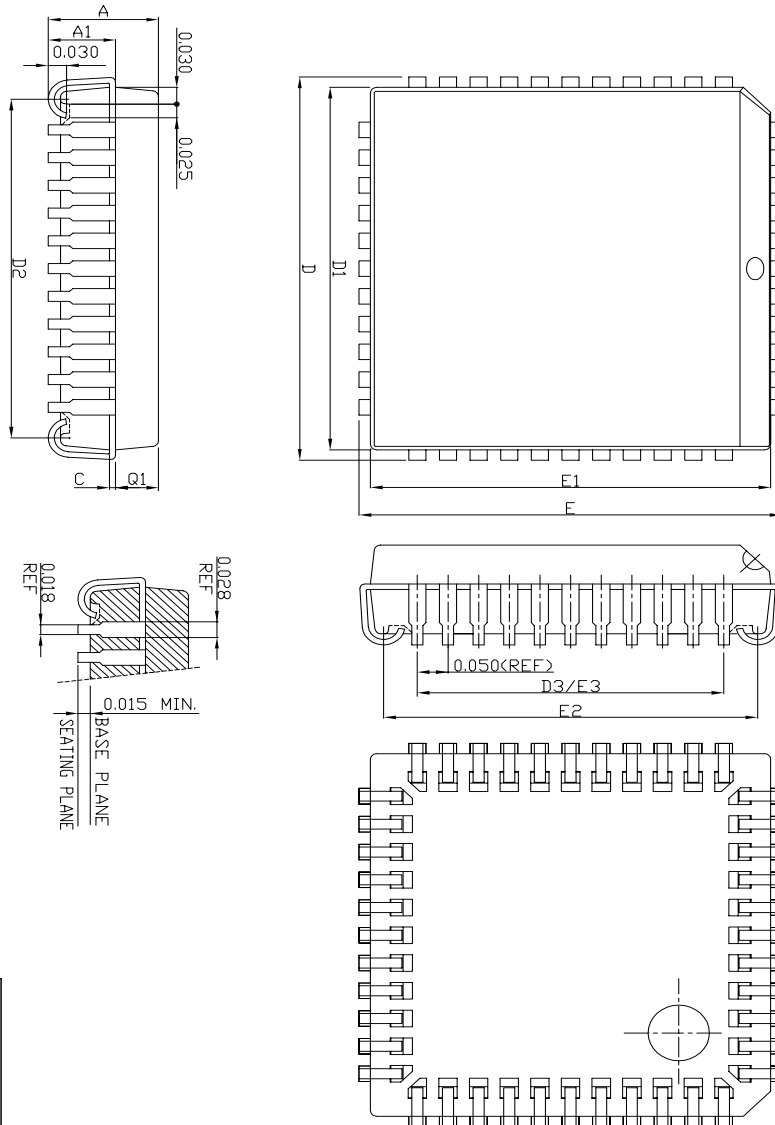
PART NO.	ACCESS TIME	OPERATING CURRENT	STANDBY CURRENT	PACKAGE
		(ns)	MAX.(mA)	MAX.(uA)
MX27C2100PC-70	70	40	100	40 Pin DIP(ROM pin out)
MX27C2100PC-90	90	40	100	40 Pin DIP(ROM pin out)
MX27C2100PC-12	120	40	100	40 Pin DIP(ROM pin out)
MX27C2100PC-15	150	40	100	40 Pin DIP(ROM pin out)
MX27C2048PC-55	55	40	100	40 Pin DIP(JEDEC pin out)
MX27C2048PC-70	70	40	100	40 Pin DIP(JEDEC pin out)
MX27C2048PC-90	90	40	100	40 Pin DIP(JEDEC pin out)
MX27C2048PC-12	120	40	100	40 Pin DIP(JEDEC pin out)
MX27C2048PC-15	150	40	100	40 Pin DIP(JEDEC pin out)
MX27C2048QC-55	55	40	100	44 Pin PLCC
MX27C2048QC-70	70	40	100	44 Pin PLCC
MX27C2048QC-90	90	40	100	44 Pin PLCC
MX27C2048QC-12	120	40	100	44 Pin PLCC
MX27C2048QC-15	150	40	100	44 Pin PLCC
MX27C2048TC-55	55	40	100	40 Pin TSOP(I)
MX27C2048TC-70	70	40	100	40 Pin TSOP(I)
MX27C2048TC-90	90	40	100	40 Pin TSOP(I)
MX27C2048TC-12	120	40	100	40 Pin TSOP(I)
MX27C2048TC-15	150	40	100	40 Pin TSOP(I)

PACKAGE INFORMATION

40-PIN PLASTIC DIP(600 mil)



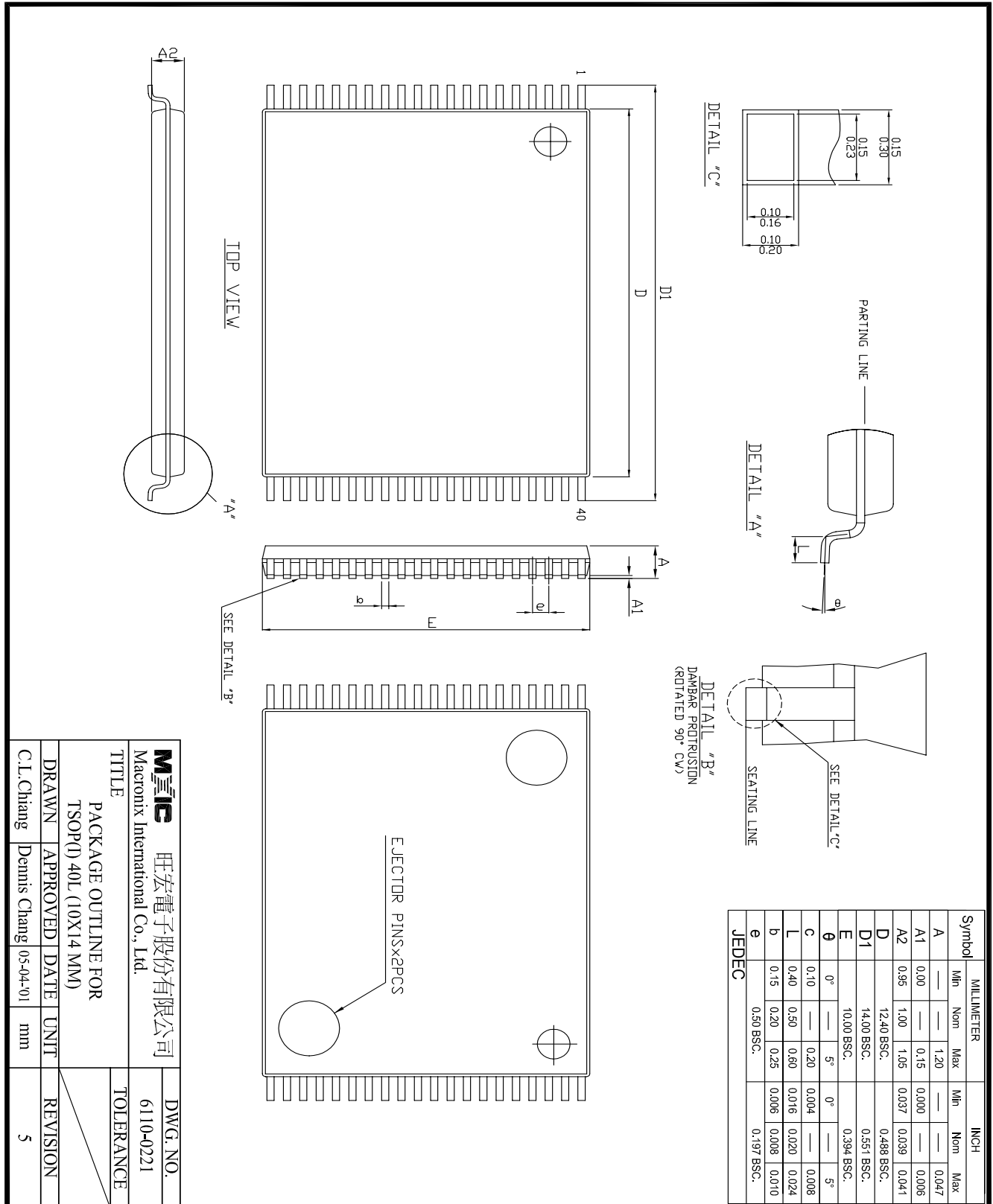
44-PIN PLASTIC LEADED CHIP CARRIER(PLCC)



Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A			0.180			4.57
A1	0.100	0.105	0.110	2.54	2.67	2.79
Q1	0.068	0.070	0.072	1.73	1.78	1.83
C		0.010(REF)			0.25(REF)	
D	0.685	0.690	0.695	17.40	17.53	17.65
D1	0.650	0.653	0.656	16.51	16.59	16.66
D2	0.600	0.610	0.620	15.24	15.49	15.75
D3		0.500(REF)			12.70(REF)	
E	0.685	0.690	0.695	17.40	17.53	17.65
E1	0.650	0.653	0.656	16.51	16.59	16.66
E2	0.600	0.610	0.620	15.24	15.49	15.75
E3		0.500(REF)			12.70(REF)	

REFERENCE DOCUMENT : JEDEC SPEC -MS-016a

MIIIC 旺宏電子股份有限公司				DWG. NO.	
Macronix International Co., Ltd.				6110-0209.3	
TITLE				TOLERANCE	
PACKAGE OUTLINE FOR				.X ±.	
PLCC 44L				XX ±01	
DRAWN				.XXX±.002	
APPROVED				REVISION	
DATE				2	
UNIT					
C.L.Chang					
Dennis Chang					
05-03-'01					
inch					



REVISION HISTORY

Revision No.	Description	Page	Date
3.0	SWITCHING TEST WAVEFORMS: For 90/120/150ns, the AC driving level are revised from 2.4V/0.4V to 3.0V/0V.		10/23/1996
4.0	1)Eliminate Interactive Programming Mode. 2)40-CDIP package quartz len, change to square shape.		6/13/1997
4.1	IPP : 100uA----> 10uA		8/8/1997
4.2	Cancel Ceramic DIP package type	P1,2,3,13,14	MAR/01/2000
4.3	Cancel "Ultraviolet Erasable" wording in General Description To modify Package Information	P1 P14~16	AUG/22/2001



MX27C2100/27C2048

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