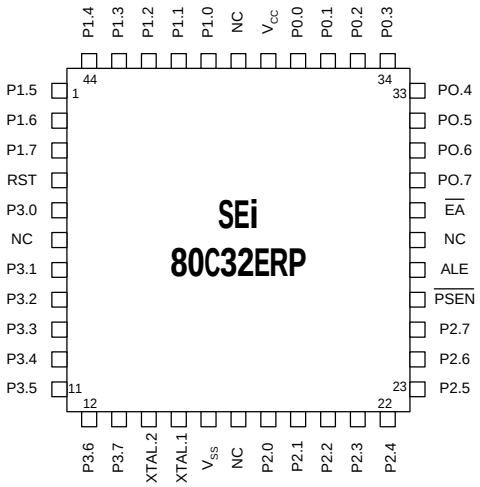
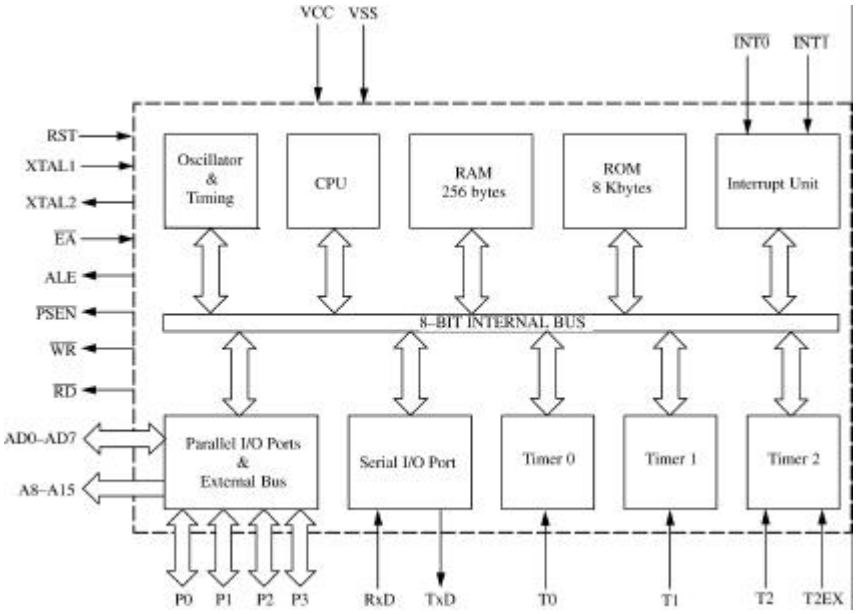
PRELIMINARY

SPACE ELECTRONICS INC.
SPACE PRODUCTS

CMOS 8-BIT MICROCONTROLLER

80C32ERP





FEATURES:

- CMOS Single-chip 8-bit microcontroller
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness >100 Krad (Si); dependent upon orbit
- Package:
  - 44 pin RAD-PAK® quad flat pack
- Power control modes
- 256 x 8-Bit RAM
- 32 programmable I/O lines
- Three 16-bit timer
- 64K program memory space
- Fully static design
- Boolean processor
- 6 interrupt sources
- Programmable serial port
- 64K data memory space

DESCRIPTION:

Space Electronics' 80C32ERP (RP for RAD-PAK®) high performance CMOS single-chip 8-bit microcontroller features a typical 100krad(Si) total dose tolerance; dependent upon orbit. The 80C32ERP fully static design allows to reduce system power consumption by bringing the clock frequency down to any value without loss of data and greatly enhances the radiation tolerance. Its features include: 256 bytes of RAM, 32 I/O lines, three 16-bit timers, a 6-source, 2-level interrupt structure, a full duplex serial port, and on-chip oscillator and clock circuits. The patented radiation-hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. Capable of surviving in space environment, the 80C32ERP is ideal for satellite, spacecraft, and space probe missions. It is available with packaging and screening up to Class S.

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TABLE 1. 80C32ERP PIN DESCRIPTION

PIN/PORT	DESCRIPTION
V_{SS}	Circuit ground potential
V_{CC}	Supply voltage during Normal, Idle, and Power Down Operation
RST	High level of RST for 2 machine cycles while oscillator is running resets the device
ALE	Address Latch Enable output for latching during accesses to external memory
	Can sink/source 8 LS TTL inputs and drive CMOS inputs without an external pullup
$\overline{PSEN}$	Program Store Enable output is the read strobe to external Program Memory
	Activated twice each machine cycle during fetches from external Program Memory
	Not activated during fetches from internal Program Memory
	Can sink/source 8 LS TTL inputs and drive CMOS inputs and drive CMOS inputs without an external pullup
$\overline{EA}$	When $\overline{EA}$ is held high, the CPU executes out of internal Program Memory (unless the Program Counter exceeds 1 FFFH)
	When $\overline{EA}$ is held low, the CPU executes only out of external Program Memory
	Must not be floated
XTAL1	Input to inverting amplifier that forms the oscillator
	Receives the external oscillator signal when an external oscillator is used
XTAL2	Outut of the inverting amplifier that forms the oscillator
	Should be floated when an external oscillator is used
Port 0	8-bit open drain bi-directional I/O port
	Pins that have 1's written to them float and can be used as high-impedance inputs when in that state
	Multiplexed low-order address and data bus during accesses to external Program and Data Memory
	Uses strong internal pullups when emitting 1's
	Outputs code butes during program verification
	Can sink 8 LS TTL inputs
Port 1	8-bit open drain bi-directional I/O port
	Pins that have 1's written to them are pulled high by internal pullups and can be used as inputs in that state
	Receives low order address bute during program verification
	Can sink/source 3 LS TTL inputs and drive CMOS inputs without external pullups
	2 inputs are also used for timer/counter 2: - P1.0 [T2}: External clock input for timer/counter 2 - P1.1 [T2EX]: Trigger input for timer/counter 2 to be captured or reloaded causing the timer/counter 2 interrupt
Port 2	8-bit open drain bi-directional I/O port
	Pins that have 1's writen to them are pulled high by internal pullups and can be used as inputs in that state
	Can sink/source 3 LS TTL inputs and drive CMOS inputs without external pullups
Port 3	8-bit open drain bi-directional I/O port
	Pins that have 1's written to them are pulled high by internal pullups and can be used as inputs in that state

TABLE 2. 80C32ERP ABSOLUTE MAXIMUM RATINGS

(V_{CC} = 5 V ± 10%, V_{SS} = 0 V, F = 0 TO 36 MHz, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Voltage on any pin relative to V_{SS}	V_{SS}	-0.5	V_{CC} + 0.7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5	7	V
Operating Temperature	T_A	-55	125	°C
Storage Temperature	T_{STG}	-65	150	°C
Power Dissipation	P_D	--	1	W

TABLE 3. 80C32ERP DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 V ± 10%, V_{SS} = 0 V, F = 0 TO 36 MHz, T_A = -55 TO 125 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Input Low Voltage	V_{IL}		-0.5	0.2 V_{CC}-0.1	V
Input High Voltage (except XTAL, RST)	V_{IH}		0.2 V_{CC}+1.4	V_{CC}+0.5	V
Input High Voltage (for XTAL, RST)	V_{IH1}		0.7 V_{CC}	V_{CC}+0.5	V
Output Low Voltage (Port 1,2,3)	V_{OL}	I_{OL} = 1.6 mA [1]	--	0.45	V
Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)	V_{OL1}	I_{OL} = 3.2 mA [1]	--	0.45	V
Output High Voltage (Port 1,2,3)	V_{OH}	I_{OH} = -60 uA V_{CC} = 5 V ±10% I_{OH} = -25 uA I_{OH} = -10 uA	2.4 -- 0.75 V_{CC} 0.9 V_{CC}	-- -- -- --	V
Output High Voltage (Port 0 in External Bus Mode, ALE $\overline{PSEN}$)	V_{OH1}	I_{OH} = -400 uA V_{CC} = 5 V ±10% I_{OH} = -150 uA I_{OH} = -40 uA	2.4 -- 0.75 V_{CC} 0.9 V_{CC}	-- -- -- --	V
Logical 0 Input Currents Ports 1,2,3	I_{IL}	V_{IN} = 0.45 V	--	-75	uA
Logical 1 to 0 Transition Current (Ports 1,2,3)	I_{TL}	V_{IN} = 2 V	--	-750	uA
Input Leakage Current	ILI	0.45 < V_{IN} < V_{CC}	--	±10	uA
RST Pulldown Resistor	RRST		50	200	kW
Capacitance of I/O Buffer	$C_{I/O}$	f_c = 1 MHz, T_A = 25 °C	--	10	pF
Power Down Current	I_{PD}	V_{CC} = 2 V to 5.5 V [2]	--	75	uA
Power Supply Current	I_{CC}	VCC = 5.5 V [1,2]			mA
Freq = 1 MHz I_{CC}op			--	1.8	
I_{CC} idle			--	1	
Freq = 6 MHz I_{CC}op			--	10	
I_{CC} idle			--	--	
Freq ≥ 12 MHz I_{CC}op = 1.25 Freq (MHz) + 5 mA			--	4	
I_{CC} idle = 0.36 Freq (MHz) + 2.7 mA			--	--	

1. I_{CC} is measured with all output pins disconnected; STAL1 is driven with TCLCH, TCHCL 5 ns, V_{IL} = V_{SS} + 0.5 V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = V_{CC}. I_{CC} would be slightly higher if a crystal oscillator used.

2. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLS of ALE and Port 3. The noise is due to external bus capacitance discharging onto the Port 0 and Port 2 pins when these pins make the transitions during bus operations. In the worst case (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45V with maximum VOL peak 0.6 V. A Schmitt Trigger use in not necessary.

TABLE 4. EXTERNAL PROGRAM MEMORY CHARACTERISTICS

(T_A = -55 TO 125 °C, V_{SS} = 0, V_{CC} = 5 V ± 10%, F = 0 TO 36 MHz)

PARAMETER	SYMBOL	MIN	MAX	UNIT
ALE Pulse Width	TLHLL			ns
16 MHz		110	--	
20 MHz		90	--	
25 MHz		70	--	
30 MHz		60	--	
36 MHz		50	--	
Address Valid to ALE	TAVLL			ns
16 MHz		40	--	
20 MHz		30	--	
25 MHz		20	--	
30 MHz		15	--	
36 MHz		10	--	
Address Hold After ALE	TLLAX			ns
16 MHz		35	--	
20 MHz		35	--	
25 MHz		35	--	
30 MHz		35	--	
36 MHz		35	--	
ALE to Valid Instrument In	TLLIV			ns
16 MHz		--	185	
20 MHz		--	170	
25 MHz		--	130	
30 MHz		--	100	
36 MHz		--	80	
ALE to PSEN	TLLPL			ns
16 MHz		45	--	
20 MHz		40	--	
25 MHz		30	--	
30 MHz		25	--	
36 MHz		20	--	
PSEN Pulse Width	TPLPH			ns
16 MHz		165	--	
20 MHz		130	--	
25 MHz		100	--	
30 MHz		80	--	
36 MHz		75	--	

TABLE 4. EXTERNAL PROGRAM MEMORY CHARACTERISTICS

(T_A = -55 TO 125 °C, V_{SS} = 0, V_{CC} = 5 V ± 10%, F = 0 TO 36 MHz)

PARAMETER	SYMBOL	MIN	MAX	UNIT
PSEN to Valid Instrument in 16 MHz	TPLIV			ns
16 MHz		--	125	
20 MHz		--	110	
25 MHz		--	85	
30 MHz		--	65	
36 MHz		--	50	
Input Instrument Hold After PSEN	TPXIX			ns
16 MHz		0	--	
20 MHz		0	--	
25 MHz		0	--	
30 MHz		0	--	
36 MHz		0	--	
Input Instrument Float After PSEN	TPXIZ			ns
16 MHz		--	50	
20 MHz		--	45	
25 MHz		--	35	
30 MHz		--	30	
36 MHz		--	25	
PSEN to Address Valid	TPXAV			ns
16 MHz		55	--	
20 MHz		50	--	
25 MHz		40	--	
30 MHz		35	--	
36 MHz		30	--	
Address to Valid Instrument in 16 MHz	TAVIV			ns
16 MHz		--	230	
20 MHz		--	210	
25 MHz		--	170	
30 MHz		--	130	
36 MHz		--	90	
PSEN Low to Address Float [1]	TPLAZ			ns
16 MHz		--	10	
20 MHz		--	10	
25 MHz		--	8	
30 MHz		--	6	
36 MHz		--	5	

1. Not tested.

TABLE 5. EXTERNAL DATA MEMORY CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
RD Pulse Width	TRLRH			ns
16 MHz		340	--	
20 MHz		270	--	
25 MHz		210	--	
30 MHz		180	--	
36 MHz		120	--	
WR Pulse Width	TWLWH			ns
16 MHz		340	--	
20 MHz		270	--	
25 MHz		210	--	
30 MHz		180	--	
36 MHz		120	--	
Address Hold After ALE	TLLAX			ns
16 MHz		85	--	
20 MHz		85	--	
25 MHz		70	--	
30 MHz		55	--	
36 MHz		35	--	
RD to Valid Data In	TRLDV			ns
16 MHz		--	240	
20 MHz		--	210	
25 MHz		--	175	
30 MHz		--	135	
36 MHz		--	110	
Data Hold After RD	TRHDX			ns
16 MHz		0	--	
20 MHz		0	--	
25 MHz		0	--	
30 MHz		0	--	
36 MHz		0	--	
Data Float After RD	TRHDZ			ns
16 MHz		--	90	
20 MHz		--	90	
25 MHz		--	80	
30 MHz		--	70	
36 MHz		--	50	
ALE to Valid Data In	TLLDV			ns
16 MHz		--	435	
20 MHz		--	370	
25 MHz		--	290	
30 MHz		--	235	
36 MHz		--	170	

TABLE 5. EXTERNAL DATA MEMORY CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Address to Valid Data In	TAVDV			ns
16 MHz		--	480	
20 MHz		--	400	
25 MHz		--	320	
30 MHz		--	260	
36 MHz		--	190	
ALE to WR or RD	TLLWL			ns
16 MHz		150	250	
20 MHz		135	170	
25 MHz		120	130	
30 MHz		90	115	
36 MHz		70	100	
Address to WR or RD	TAVWL			ns
16 MHz		180	--	
20 MHz		180	--	
25 MHz		140	--	
30 MHz		115	--	
36 MHz		75	--	
Data Valid to WR Transition	TQVWX			ns
16 MHz		35	--	
20 MHz		35	--	
25 MHz		30	--	
30 MHz		20	--	
36 MHz		15	--	
Data Setup to WR Transition	TQVWH			ns
16 MHz		380	--	
20 MHz		325	--	
25 MHz		250	--	
30 MHz		215	--	
36 MHz		170	--	
Data Hold After WR	TWHQX			ns
16 MHz		40	--	
20 MHz		35	--	
25 MHz		30	--	
30 MHz		20	--	
36 MHz		15	--	
RD Low to Address Float	TRLAZ			ns
16 MHz		--	0	
20 MHz		--	0	
25 MHz		--	0	
30 MHz		--	0	
36 MHz		--	0	

TABLE 5. EXTERNAL DATA MEMORY CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
RD or WR High to ALE High	TWHLH			ns
16 MHz		35	90	
20 MHz		35	60	
25 MHz		25	45	
30 MHz		20	40	
36 MHz		20	40	

TABLE 6. SERIAL PORT TIMING - SHIFT REGISTER MODE (VALUES IN NS) [1]

PARAMETER	SYMBOL	MIN	MAX	UNIT
Serial Port Clock Cycle Time	TXLXL			ns
16 MHz		750	--	
20 MHz		600	--	
25 MHz		480	--	
30 MHz		400	--	
36 MHz		330	--	
Output Data Setup to Clock Rising Edge	TQVXH			ns
16 MHz		563	--	
20 MHz		480	--	
25 MHz		380	--	
30 MHz		300	--	
36 MHz		220	--	
Output Data Hold After Clock Rising Edge	TXHQX			ns
16 MHz		63	--	
20 MHz		90	--	
25 MHz		65	--	
30 MHz		50	--	
36 MHz		45	--	
Input Data Hold After Clock Rising Edge	TXHDX			ns
16 MHz		0	--	
20 MHz		0	--	
25 MHz		0	--	
30 MHz		0	--	
36 MHz		0	--	
Clock Rising Edge to Input Data Valid	TXHDV			ns
16 MHz		--	563	
20 MHz		--	450	
25 MHz		--	350	
30 MHz		--	300	
36 MHz		--	250	

1. Not tested.

TABLE 7. EXTERNAL CLOCK DRIVE CHARACTERISTICS (XTAL1)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Oscillator Frequency	FCLCL	--	36	MHz
Oscillator Period	TCLCL	27.8	--	ns
High Time	TCHCX	5	--	ns
Low Time	TCLCX	5	--	ns
Rise Time	TCLCH	--	5	ns
Fall Time	TCHCL	--	5	ns

FIGURE 1. EXTERNAL CLOCK DRIVE WAVEFORMS

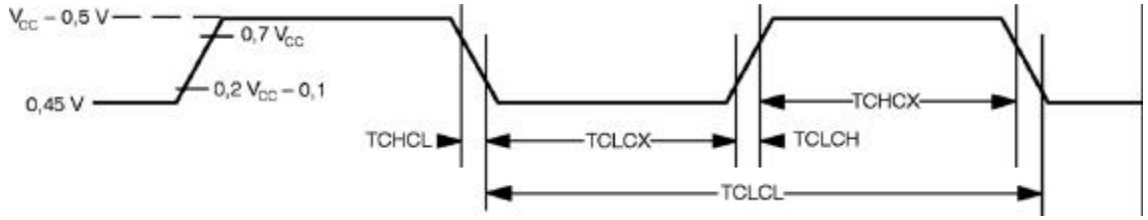


FIGURE 2. EXTERNAL PROGRAM MEMORY READ CYCLE

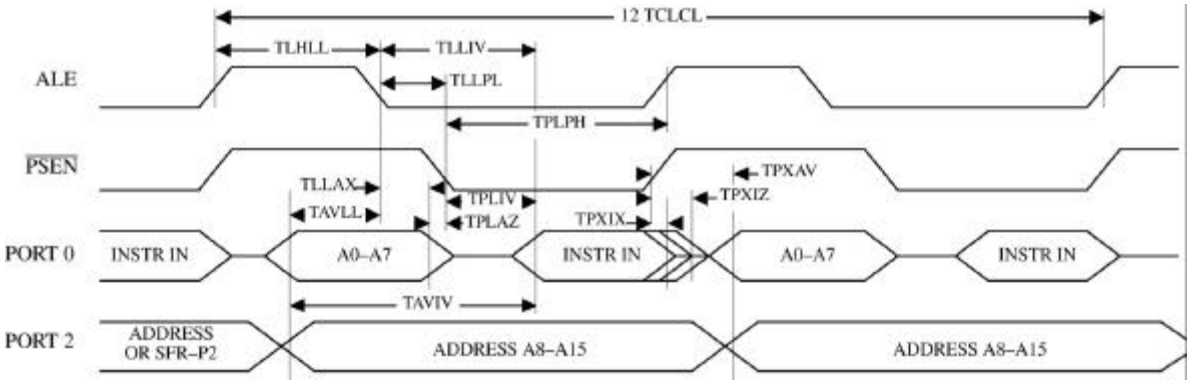


FIGURE 3. EXTERNAL DATA MEMORY WRITE CYCLE

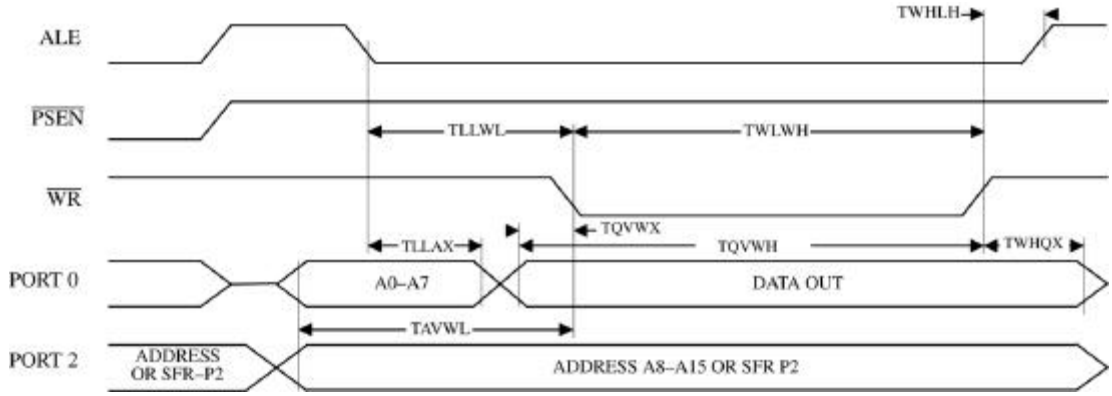


FIGURE 4. EXTERNAL DATA MEMORY READ CYCLE

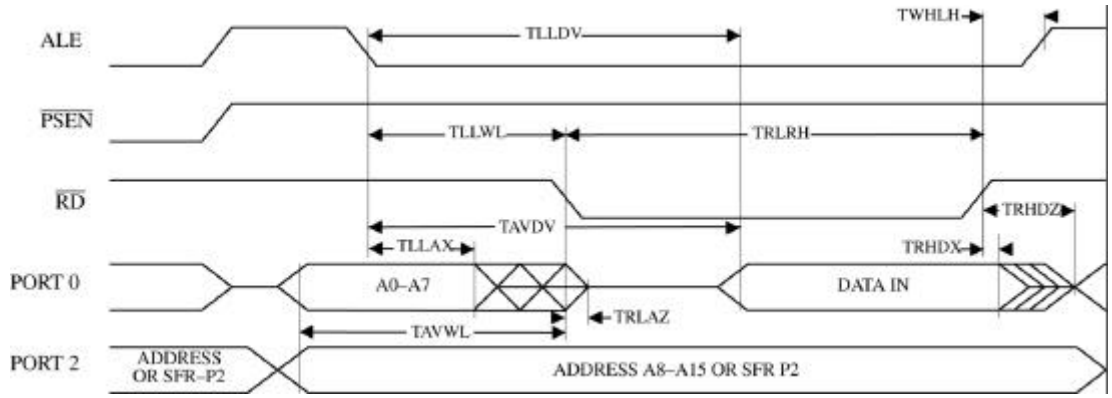
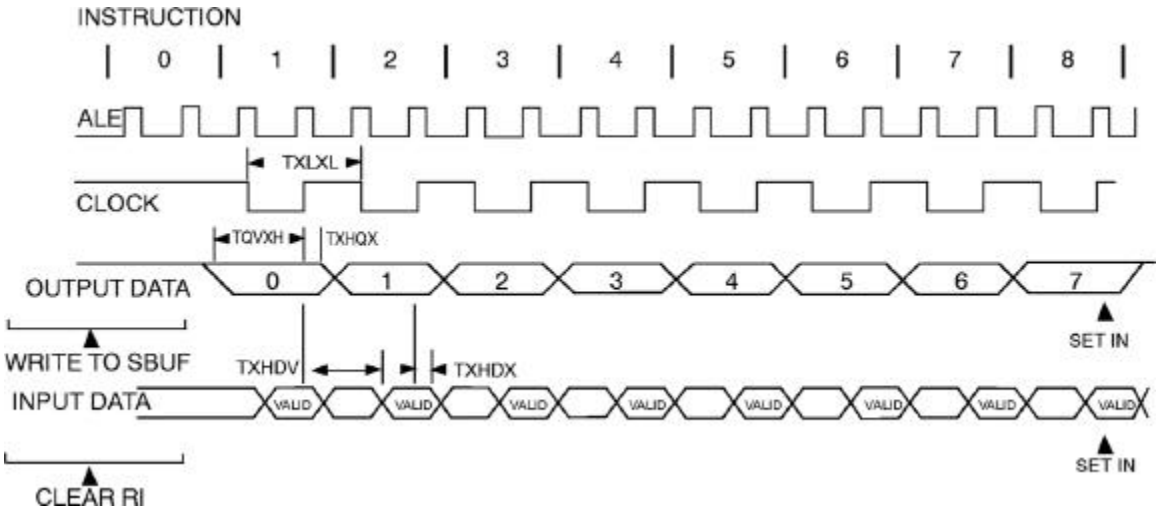
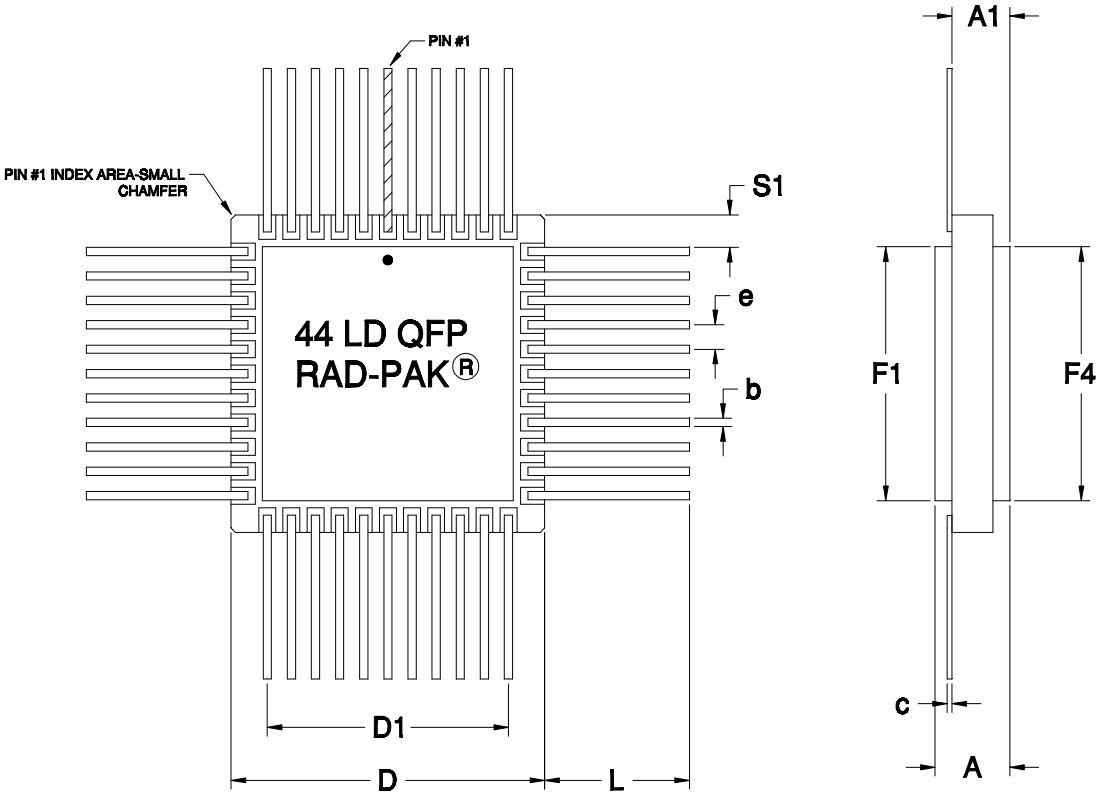


FIGURE 5. SHIFT REGISTER TIMING WAVEFORM





44 PIN RAD-PAK® QUAD FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.139	0.153	0.167
b	0.015	0.017	0.019
c	0.007	0.010	0.010
D	0.642	0.650	0.658
D1	0.500 BSC		
e	0.050 BSC		
S1	0.013	0.067	--
F1	0.495	0.500	0.525
F4	0.469	0.475	0.481
L	0.265	0.275	0.285
A1	0.097	0.108	0.199
N	44		

Q44-03

Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Space Electronics verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Space Electronics assumes no responsibility for the use of this information.

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