



ALPHA & OMEGA
SEMICONDUCTOR



AO4806

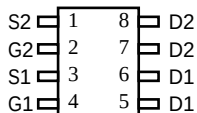
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

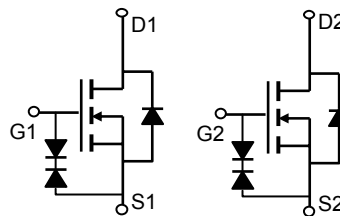
The AO4806 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. They offer operation over a wide gate drive range from 1.8V to 12V. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration.
Standard Product AO4806 is Pb-free (meets ROHS & Sony 259 specifications). AO4806L is a Green Product ordering option. AO4806 and AO4806L are electrically identical.

Features

V_{DS} (V) = 20V
 I_D = 9.4A (V_{GS} = 10V)
 $R_{DS(ON)} < 14m\Omega$ (V_{GS} = 10V)
 $R_{DS(ON)} < 15m\Omega$ (V_{GS} = 4.5V)
 $R_{DS(ON)} < 21m\Omega$ (V_{GS} = 2.5V)
 $R_{DS(ON)} < 30m\Omega$ (V_{GS} = 1.8V)
ESD Rating: 2000V HBM



SOIC-8



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^A	I_D	9.4	A
		7.5	
Pulsed Drain Current ^B	I_{DM}	40	
Power Dissipation	P_D	2	W
		1.28	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	45	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		72	110	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	34	40	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=16\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^{\circ}\text{C}$			10 25	μA
I_{GSS}	Gate-Source leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 10\text{V}$			± 10	μA
BV_{GSO}	Gate-Source Breakdown Voltage	$V_{DS}=0\text{V}$, $I_G=\pm 250\mu\text{A}$	± 12			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.5	0.75	1	V
$I_{D(ON)}$	On state drain current	$V_{GS}=4.5\text{V}$, $V_{DS}=5\text{V}$	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=9.4\text{A}$ $T_J=125^{\circ}\text{C}$		11 14.3	14 17	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=8\text{A}$		12.6	16	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}$, $I_D=6\text{A}$		16.5	22	$\text{m}\Omega$
		$V_{GS}=1.8\text{V}$, $I_D=4\text{A}$		23.4	30	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=9.4\text{A}$		37		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$		0.72	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=10\text{V}$, $f=1\text{MHz}$		1810		pF
C_{oss}	Output Capacitance			232		pF
C_{rss}	Reverse Transfer Capacitance			200		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		1.6		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	$V_{GS}=4.5\text{V}$, $V_{DS}=10\text{V}$, $I_D=9.4\text{A}$		17.9		nC
Q_{gs}	Gate Source Charge			1.5		nC
Q_{gd}	Gate Drain Charge			4.7		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=10\text{V}$, $R_L=1.1\Omega$, $R_{GEN}=3\Omega$		3.3		ns
t_r	Turn-On Rise Time			5.9		ns
$t_{D(off)}$	Turn-Off DelayTime			44		ns
t_f	Turn-Off Fall Time			7.7		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=9.4\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		22		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=9.4\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		8.6		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

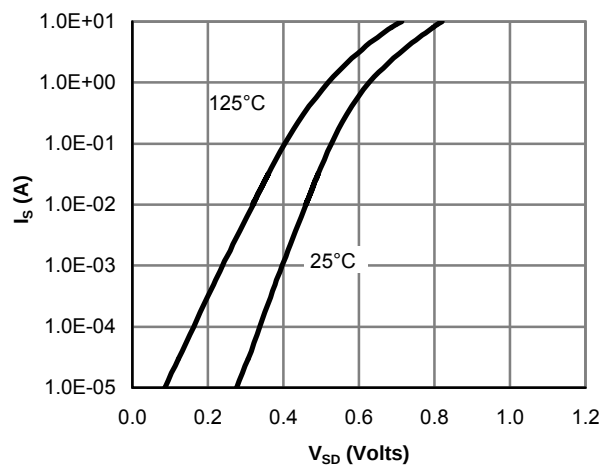
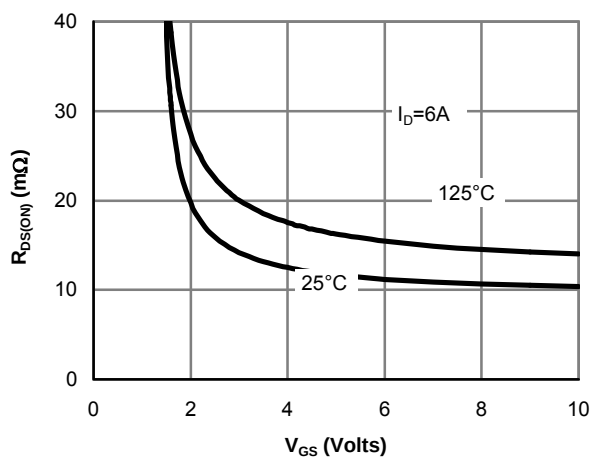
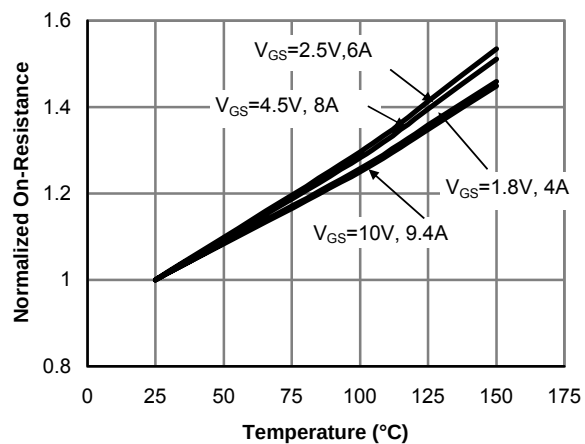
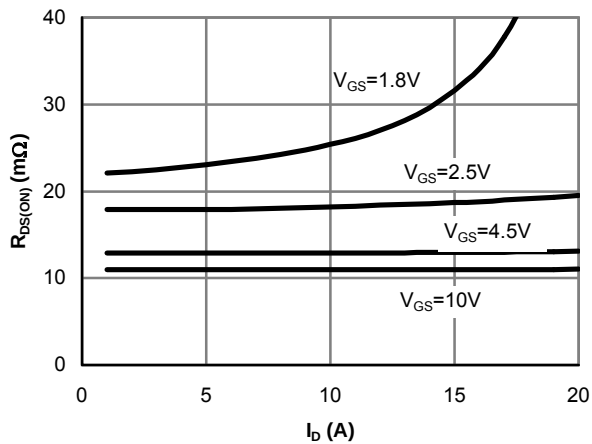
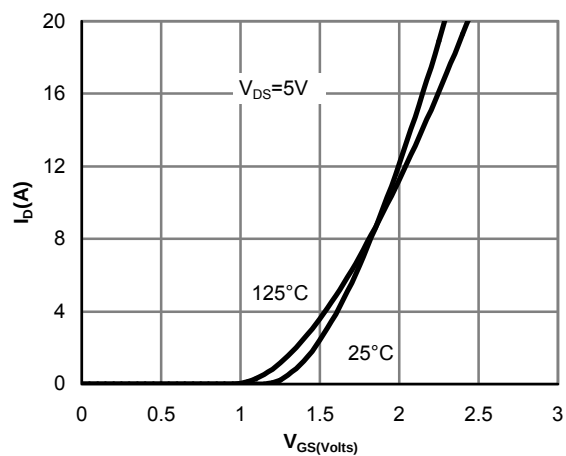
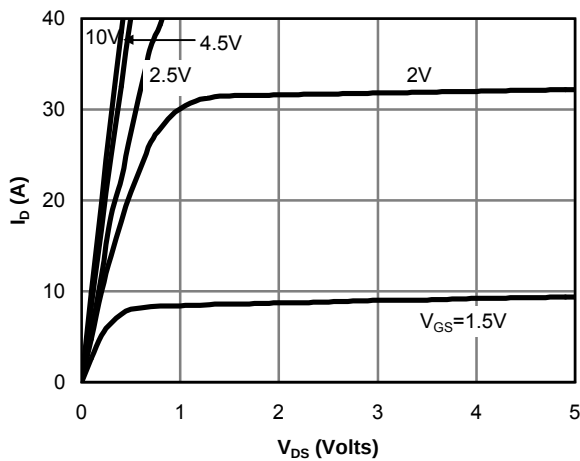
D. The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

Rev 3 : Sept 2005

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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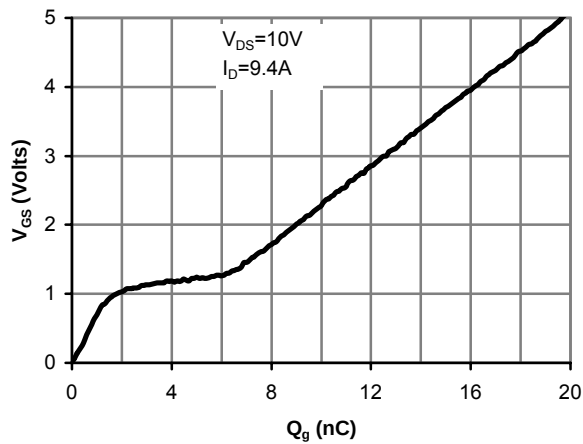


Figure 7: Gate-Charge Characteristics

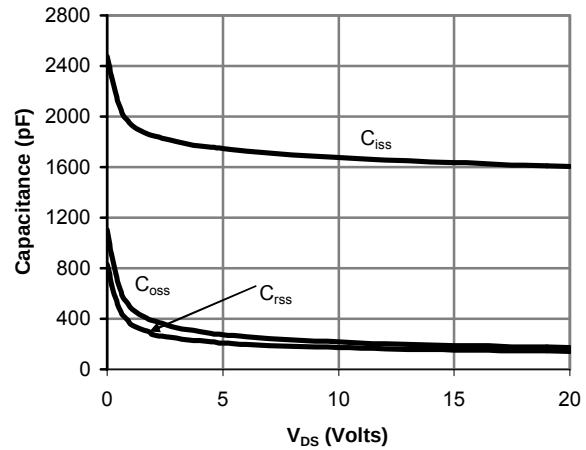


Figure 8: Capacitance Characteristics

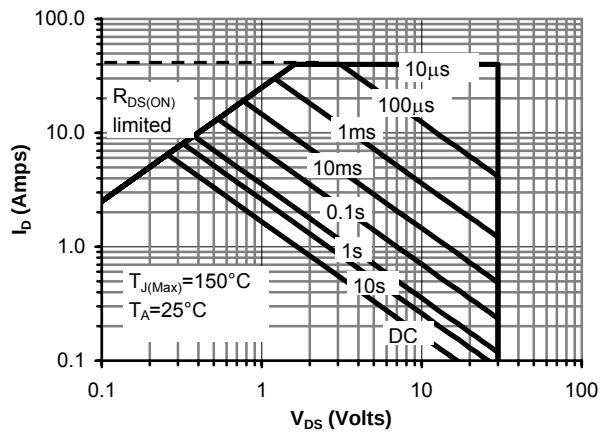


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

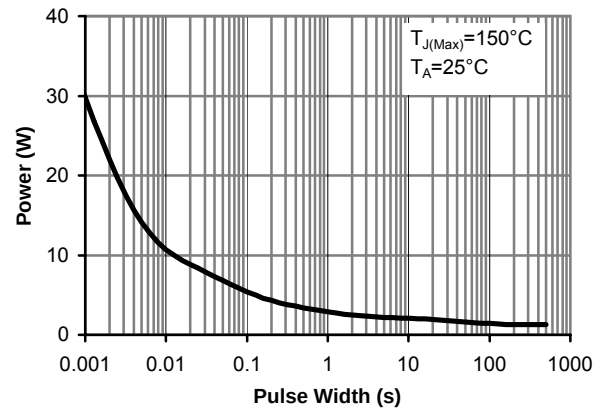


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

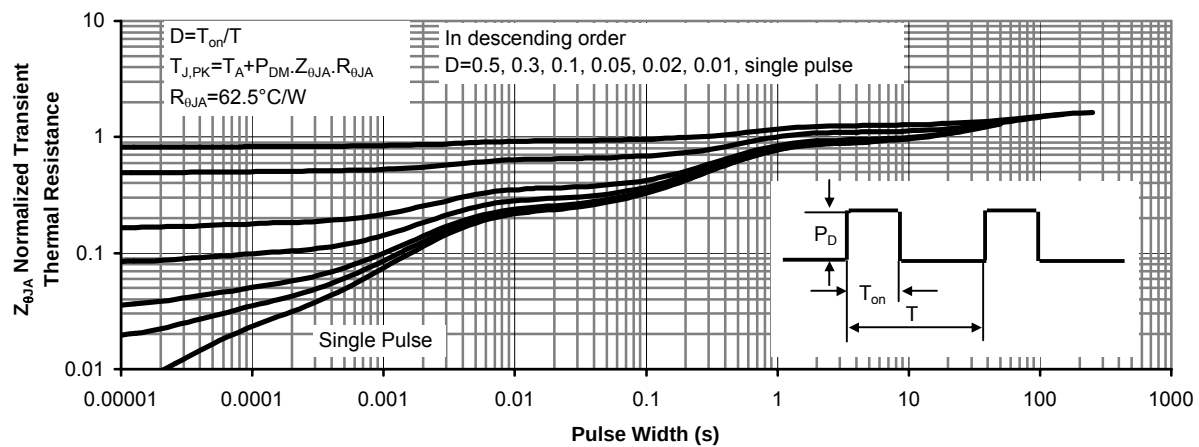


Figure 11: Normalized Maximum Transient Thermal Impedance