

74LV4051

8-channel analog multiplexer/demultiplexer

Rev. 04 — 10 August 2009

Product data sheet

1. General description

The 74LV4051 is an 8-channel analog multiplexer/demultiplexer with three digital select inputs (S0 to S2), an active-LOW enable input ($\bar{E}$), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). It is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC4051 and 74HCT4051. With $\bar{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by S0 to S2. With $\bar{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S0 to S2.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S0 to S2, and $\bar{E}$). The V_{CC} to GND ranges are 1.0 V to 6.0 V. The analog inputs/outputs (Y0 to Y7, and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6.0 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

2. Features

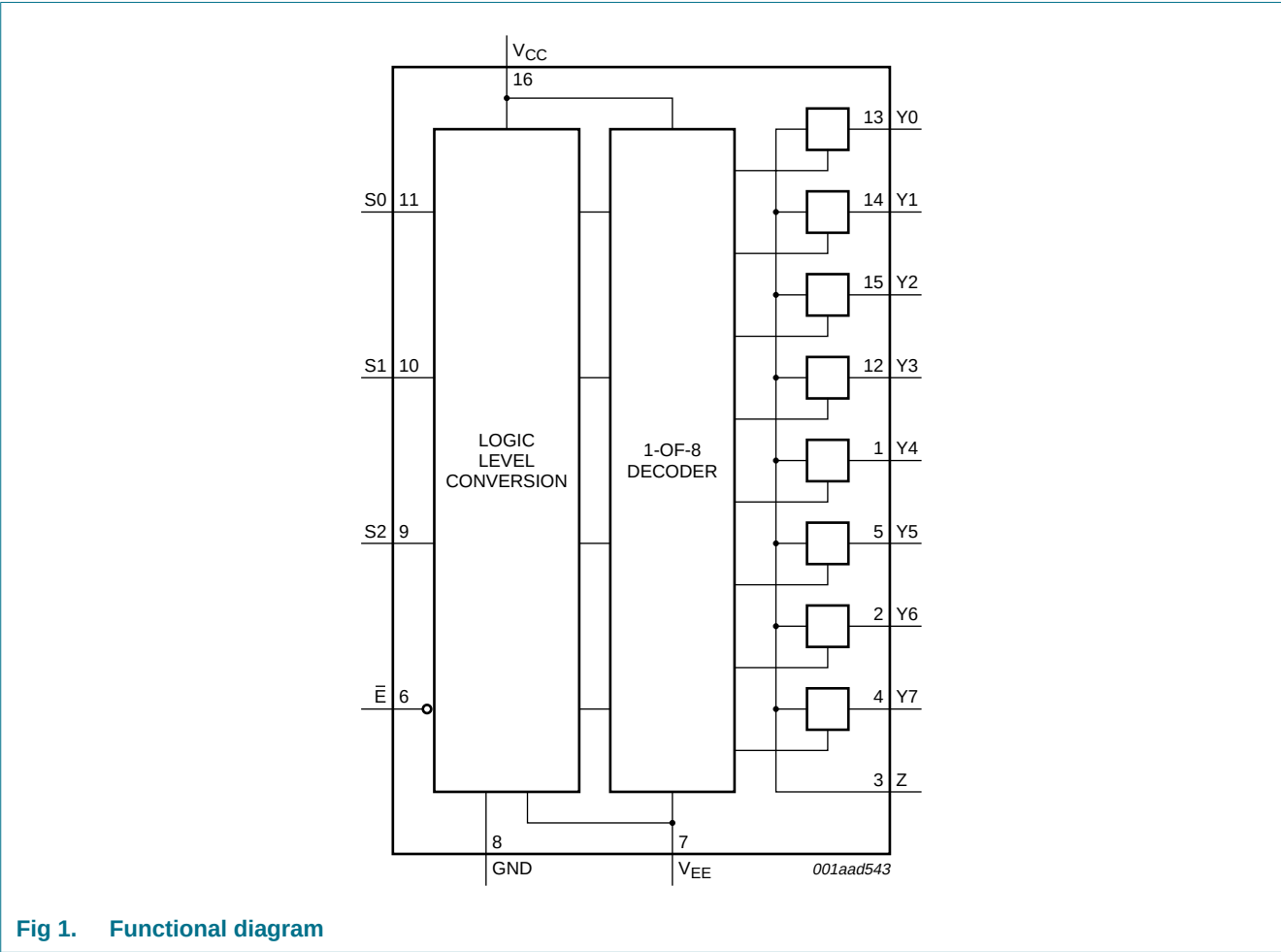
- Optimized for low-voltage applications: 1.0 V to 6.0 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Low ON resistance:
 - ◆ 145 Ω (typical) at $V_{CC} - V_{EE} = 2.0$ V
 - ◆ 80 Ω (typical) at $V_{CC} - V_{EE} = 3.0$ V
 - ◆ 60 Ω (typical) at $V_{CC} - V_{EE} = 4.5$ V
- Logic level translation:
 - ◆ To enable 3 V logic to communicate with ± 3 V analog signals
- Typical 'break before make' built in
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4051N	−40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74LV4051D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4051DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LV4051PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LV4051BQ	−40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram



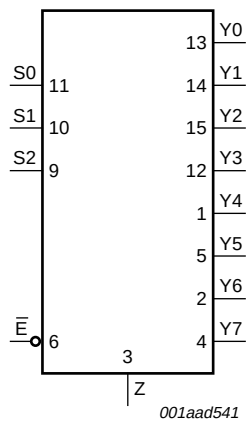


Fig 2. Logic symbol

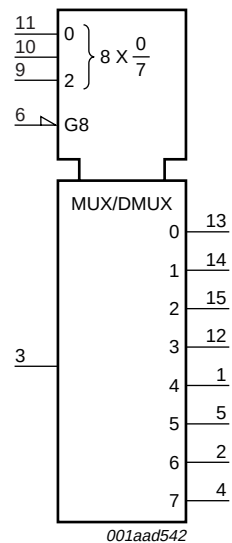


Fig 3. IEC logic symbol

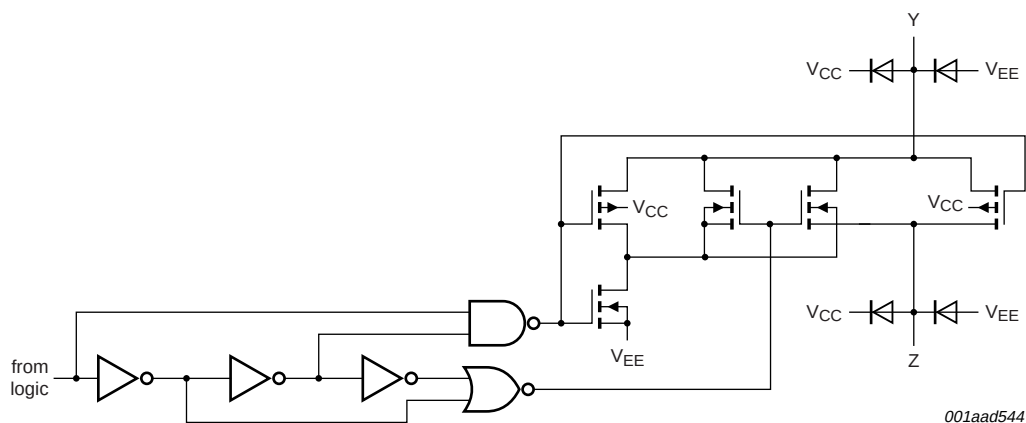
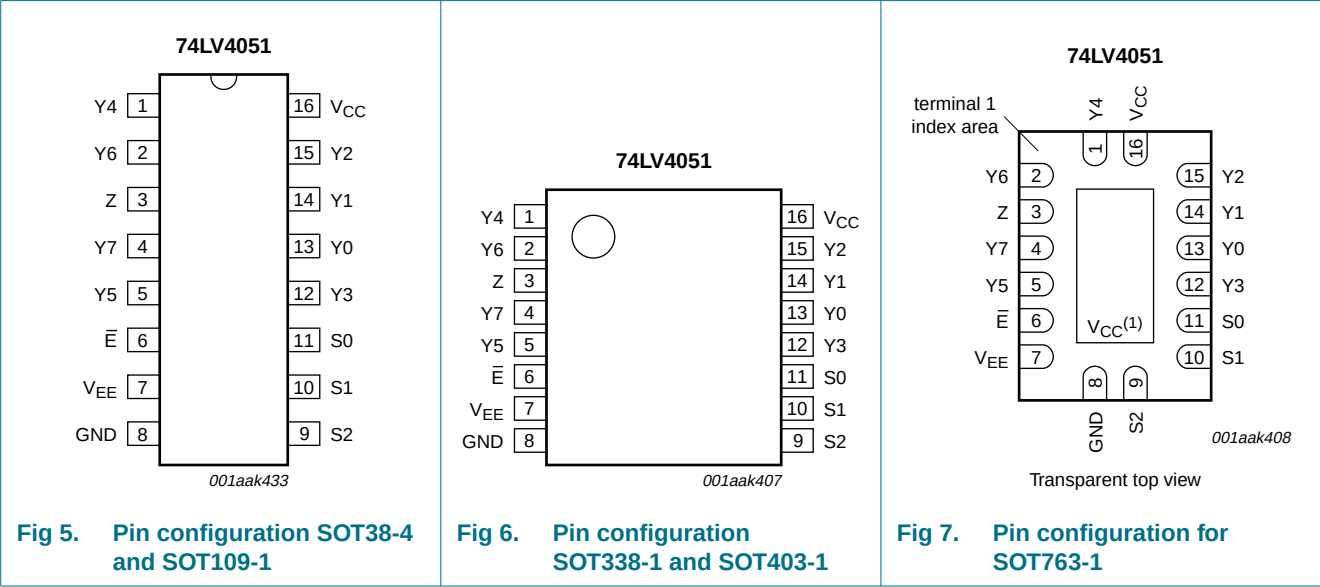


Fig 4. Schematic diagram (one switch)

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{E}$	6	enable input (active LOW)
V_{EE}	7	supply voltage
GND	8	ground supply voltage
S0, S1, S2	11, 10, 9	select input
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	13, 14, 15, 12, 1, 5, 2, 4	independent input or output
Z	3	common output or input
V_{CC}	16	supply voltage

6. Functional description

6.1 Function table

Table 3. Function table^[1]

Input				Channel ON
$\bar{E}$	S2	S1	S0	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	switches off

- [1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0$ V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		^[1] -0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	^[2] -	±20	mA
I_{SK}	switch clamping current	$V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V	^[2] -	±20	mA
I_{SW}	switch current	$V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V; source or sink current	^[2] -	±25	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	^[3]		
		DIP16 package	-	750	mW
		SO16 package	-	500	mW
		TSSOP16 package	-	500	mW
		DHVQFN16 package	-	500	mW

- [1] To avoid drawing V_{CC} current out of terminal Z, when switch current flows into terminals Y_n , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_n , and in this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or V_{EE} .
- [2] The minimum input voltage rating may be exceeded if the input current rating is observed.
- [3] For DIP16 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.
For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For SSOP16 and TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage	see Figure 8	1	3.3	6	V
V _I	input voltage		0	-	V _{CC}	V
V _{SW}	switch voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V _{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V _{CC} = 2.7 V to 3.6 V	-	-	100	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to 6.0 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

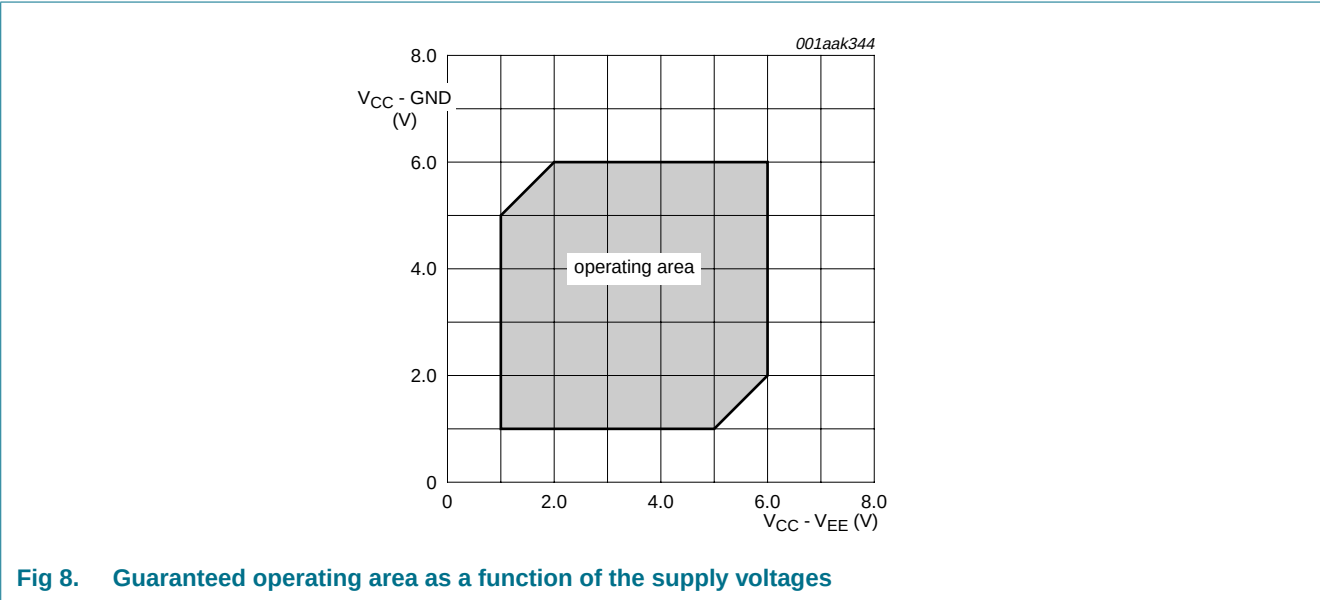


Fig 8. Guaranteed operating area as a function of the supply voltages

9. Static characteristics

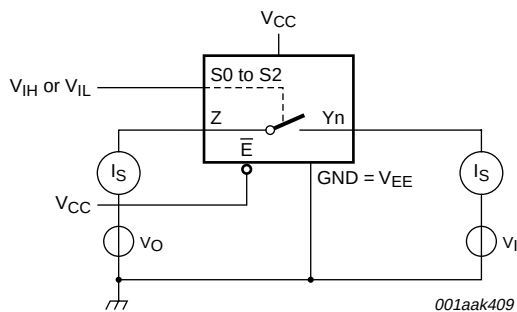
Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V _{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V	3.15	-	-	3.15	-	V
		V _{CC} = 6.0 V	4.20	-	-	4.20	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V _{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V	-	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.80	-	1.80	V
I _I	input leakage current	V _I = V _{CC} or GND						
		V _{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V _{CC} = 6.0 V	-	-	2.0	-	2.0	μA
I _{S(OFF)}	OFF-state leakage current	V _I = V _{IH} or V _{IL} ; see Figure 9						
		V _{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V _{CC} = 6.0 V	-	-	2.0	-	2.0	μA
I _{S(ON)}	ON-state leakage current	V _I = V _{IH} or V _{IL} ; see Figure 10						
		V _{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V _{CC} = 6.0 V	-	-	2.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A						
		V _{CC} = 3.6 V	-	-	20	-	40	μA
		V _{CC} = 6.0 V	-	-	40	-	80	μA
ΔI _{CC}	additional supply current	per input; V _I = V _{CC} − 0.6 V; V _{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C _I	input capacitance		-	3.5	-	-	-	pF
C _{SW}	switch capacitance	independent pins Y _n	-	5	-	-	-	pF
		common pin Z	-	25	-	-	-	pF

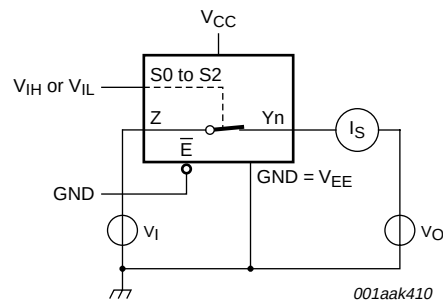
[1] Typical values are measured at T_{amb} = 25 °C.

9.1 Test circuits



$V_I = V_{CC}$ or V_{EE} and $V_O = V_{EE}$ or V_{CC} .

Fig 9. Test circuit for measuring OFF-state leakage current



$V_I = V_{CC}$ or V_{EE} and $V_O = \text{open circuit}$.

Fig 10. Test circuit for measuring ON-state leakage current

9.2 ON resistance

Table 7. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see [Figure 11](#) and [Figure 12](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	$V_I = 0 \text{ V to } V_{CC} - V_{EE}$						
		$V_{CC} = 1.2 \text{ V}; I_{SW} = 100 \mu\text{A}$ ^[2]	-	-	-	-	-	Ω
		$V_{CC} = 2.0 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	145	325	-	375	Ω
		$V_{CC} = 2.7 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	90	200	-	235	Ω
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	80	180	-	210	Ω
		$V_{CC} = 4.5 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	60	135	-	160	Ω
		$V_{CC} = 6.0 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	55	125	-	145	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_I = 0 \text{ V to } V_{CC} - V_{EE}$						
		$V_{CC} = 1.2 \text{ V}; I_{SW} = 100 \mu\text{A}$ ^[2]	-	-	-	-	-	Ω
		$V_{CC} = 2.0 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	5	-	-	-	Ω
		$V_{CC} = 2.7 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	4	-	-	-	Ω
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	4	-	-	-	Ω
		$V_{CC} = 4.5 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	3	-	-	-	Ω
		$V_{CC} = 6.0 \text{ V}; I_{SW} = 1000 \mu\text{A}$	-	2	-	-	-	Ω

Table 7. ON resistance ...continued

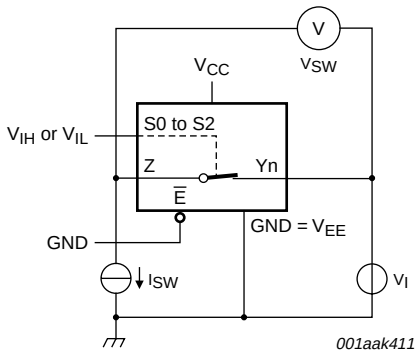
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see [Figure 11](#) and [Figure 12](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
R _{ON(rail)}	ON resistance (rail)	V _I = GND						
		V _{CC} = 1.2 V; I _{SW} = 100 µA ^[2]	-	225	-	-	-	Ω
		V _{CC} = 2.0 V; I _{SW} = 1000 µA	-	110	235	-	270	Ω
		V _{CC} = 2.7 V; I _{SW} = 1000 µA	-	70	145	-	165	Ω
		V _{CC} = 3.0 V to 3.6 V; I _{SW} = 1000 µA	-	60	130	-	150	Ω
		V _{CC} = 4.5 V; I _{SW} = 1000 µA	-	45	100	-	115	Ω
R _{ON(rail)}	ON resistance (rail)	V _I = V _{CC} – V _{EE}						
		V _{CC} = 1.2 V; I _{SW} = 100 µA ^[2]	-	250	-	-	-	Ω
		V _{CC} = 2.0 V; I _{SW} = 1000 µA	-	120	320	-	370	Ω
		V _{CC} = 2.7 V; I _{SW} = 1000 µA	-	75	195	-	225	Ω
		V _{CC} = 3.0 V to 3.6 V; I _{SW} = 1000 µA	-	70	175	-	205	Ω
		V _{CC} = 4.5 V; I _{SW} = 1000 µA	-	50	130	-	150	Ω
		V _{CC} = 6.0 V; I _{SW} = 1000 µA	-	45	120	-	135	Ω

[1] Typical values are measured at T_{amb} = 25 °C.

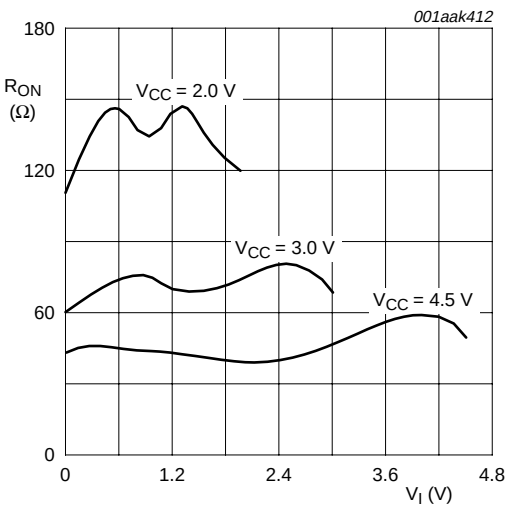
[2] When supply voltages (V_{CC} – V_{EE}) near 1.2 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 1.2 V, it is recommended to use these devices only for transmitting digital signals.

9.3 On resistance waveform and test circuit



$R_{ON} = V_{SW} / I_{SW}$.

Fig 11. Test circuit for measuring R_{ON}



$V_i = 0 \text{ V to } V_{CC} - V_{EE}$

Fig 12. Typical R_{ON} as a function of input voltage

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 15](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	Yn to Z, Z to Yn; see Figure 13 ^[2]						
		$V_{CC} = 1.2\text{ V}$	-	25	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	9	17	-	20	ns
		$V_{CC} = 2.7\text{ V}$	-	6	13	-	15	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	-	5	10	-	12	ns
		$V_{CC} = 4.5\text{ V}$	-	4	9	-	10	ns
		$V_{CC} = 6.0\text{ V}$	-	3	8	-	8	ns
t_{en}	enable time	$\bar{E}$ to Yn, Z; see Figure 14 ^[2]						
		$V_{CC} = 1.2\text{ V}$	-	145	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	49	94	-	112	ns
		$V_{CC} = 2.7\text{ V}$	-	36	69	-	83	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$ ^[3]	-	23	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	-	28	55	-	66	ns
		$V_{CC} = 4.5\text{ V}$	-	25	47	-	56	ns
		$V_{CC} = 6.0\text{ V}$	-	19	38	-	43	ns
		Sn to Yn; see Figure 14 ^[2]						
		$V_{CC} = 1.2\text{ V}$	-	140	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	48	90	-	107	ns
		$V_{CC} = 2.7\text{ V}$	-	35	66	-	79	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$ ^[3]	-	22	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	-	27	53	-	63	ns
		$V_{CC} = 4.5\text{ V}$	-	24	45	-	54	ns
		$V_{CC} = 6.0\text{ V}$	-	18	34	-	41	ns

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 15](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{dis}	disable time	$\bar{E}$ to Yn, Z; see Figure 14 ^[2]						
		$V_{CC} = 1.2\text{ V}$	-	145	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	51	93	-	110	ns
		$V_{CC} = 2.7\text{ V}$	-	38	69	-	82	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$ ^[3]	-	25	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	-	30	56	-	66	ns
		$V_{CC} = 4.5\text{ V}$	-	29	48	-	56	ns
		$V_{CC} = 6.0\text{ V}$	-	21	37	-	44	ns
		Sn to Yn; see Figure 14 ^[2]						
		$V_{CC} = 1.2\text{ V}$	-	115	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	41	73	-	90	ns
		$V_{CC} = 2.7\text{ V}$	-	31	54	-	67	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$ ^[3]	-	20	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	-	24	44	-	54	ns
		$V_{CC} = 4.5\text{ V}$	-	22	37	-	46	ns
		$V_{CC} = 6.0\text{ V}$	-	17	29	-	36	ns
C_{PD}	power dissipation capacitance	$C_L = 50\text{ pF}; f_i = 1\text{ MHz}; V_i = \text{GND to }V_{CC}$ ^[4]	-	25	-	-	-	pF

[1] All typical values are measured at $T_{amb} = 25\text{ °C}$.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3\text{ V}$).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma((C_L + C_{SW}) \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz, f_o = output frequency in MHz

C_L = output load capacitance in pF

C_{SW} = maximum switch capacitance in pF;

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1 Waveforms

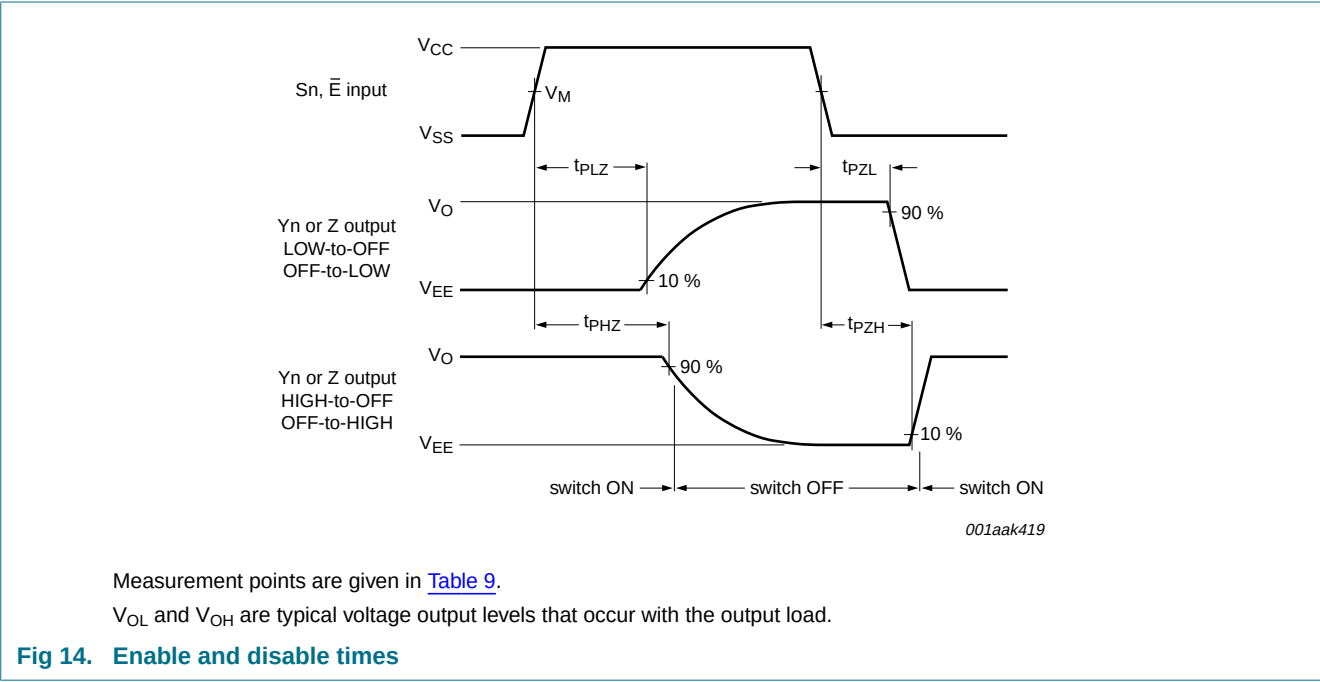
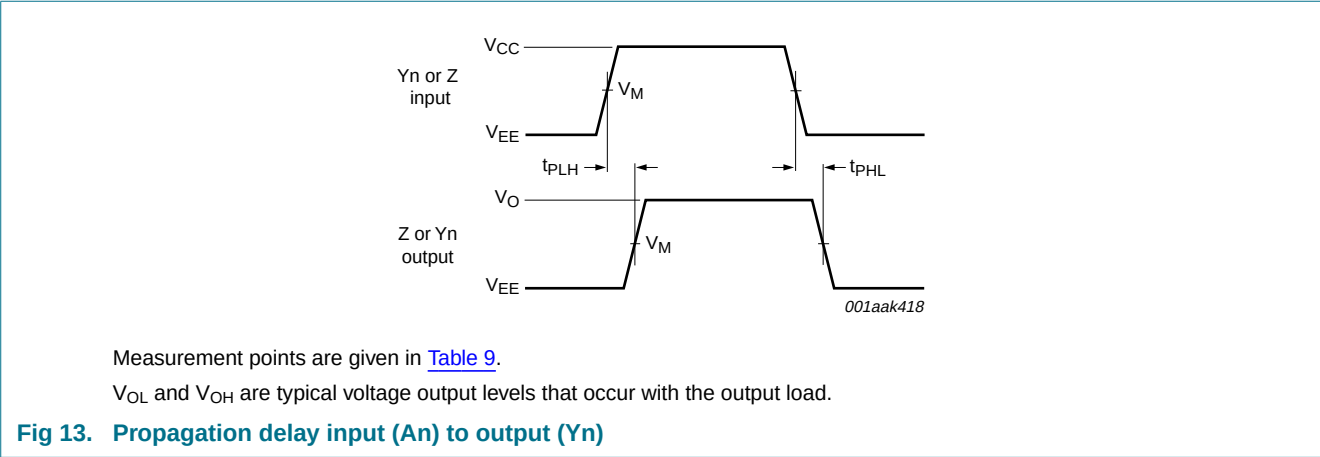
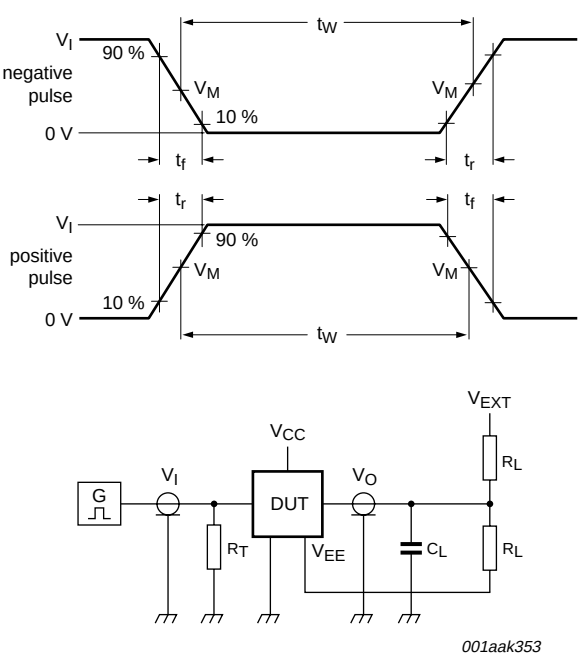


Table 9. Measurement points

Supply voltage	Input	Output		
V _{CC}	V _M	V _M	V _X	V _Y
< 2.7 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.1V _{CC}	V _{OH} - 0.1V _{CC}
2.7 V to 3.6 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V
> 3.6 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.1V _{CC}	V _{OH} - 0.1V _{CC}



Test data is given in [Table 10](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 15. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 6 ns	50 pF	1 k Ω	open	V_{EE}	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 6 ns	15 pF, 50 pF	1 k Ω	open	V_{EE}	$2V_{CC}$
> 3.6 V	V_{CC}	≤ 6 ns	50 pF	1 k Ω	open	V_{EE}	$2V_{CC}$

10.2 Additional dynamic parameters

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = \text{GND}$ or V_{CC} (unless otherwise specified); $t_r = t_f \leq 6.0 \text{ ns}$; $T_{amb} = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 1 \text{ kHz}$; $C_L = 50 \text{ pF}$; $R_L = 10 \text{ k}\Omega$; see Figure 20				
		$V_{CC} = 3.0 \text{ V}$; $V_I = 2.75 \text{ V}$ (p-p)	-	0.8	-	%
		$V_{CC} = 6.0 \text{ V}$; $V_I = 5.5 \text{ V}$ (p-p)	-	0.4	-	%
		$f_i = 10 \text{ kHz}$; $C_L = 50 \text{ pF}$; $R_L = 10 \text{ k}\Omega$; see Figure 20				
		$V_{CC} = 3.0 \text{ V}$; $V_I = 2.75 \text{ V}$ (p-p)	-	2.4	-	%
		$V_{CC} = 6.0 \text{ V}$; $V_I = 5.5 \text{ V}$ (p-p)	-	1.2	-	%
$f_{(-3\text{dB})}$	-3 dB frequency response	$C_L = 50 \text{ pF}$; $R_L = 50 \Omega$; see Figure 16	[1]			
		$V_{CC} = 3.0 \text{ V}$	-	180	-	MHz
		$V_{CC} = 6.0 \text{ V}$	-	200	-	MHz
α_{iso}	isolation (OFF-state)	$f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 600 \Omega$; see Figure 18	[2]			
		$V_{CC} = 3.0 \text{ V}$	-	-50	-	dB
		$V_{CC} = 6.0 \text{ V}$	-	-50	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; $f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 600 \Omega$; see Figure 21	[2]			
		$V_{CC} = 3.0 \text{ V}$	-	0.11	-	V
		$V_{CC} = 6.0 \text{ V}$	-	0.12	-	V
Xtalk	crosstalk	between switches; $f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 600 \Omega$; see Figure 22				
		$V_{CC} = 3.0 \text{ V}$	-	-60	-	dB
		$V_{CC} = 6.0 \text{ V}$	-	-60	-	dB

[1] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 50 Ω).

[2] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 600 Ω).

10.2.1 Test circuits

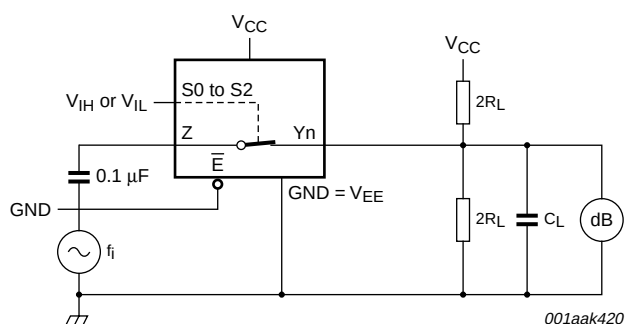
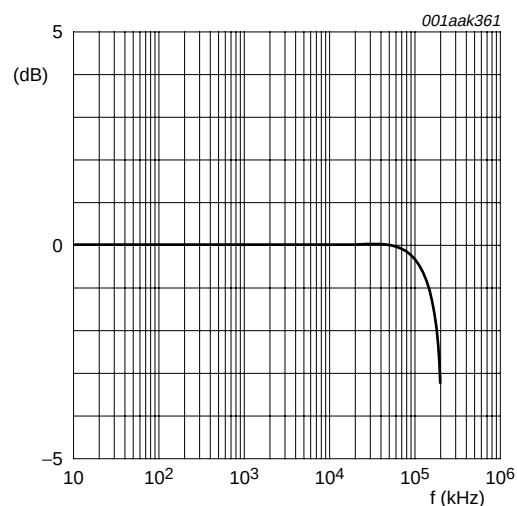


Fig 16. Test circuit for measuring frequency response



$V_{CC} = 3.0 \text{ V}$; $GND = 0 \text{ V}$; $V_{EE} = -3.0 \text{ V}$; $R_L = 50 \text{ }\Omega$;
 $R_{SOURCE} = 1 \text{ k}\Omega$.

Fig 17. Typical frequency response

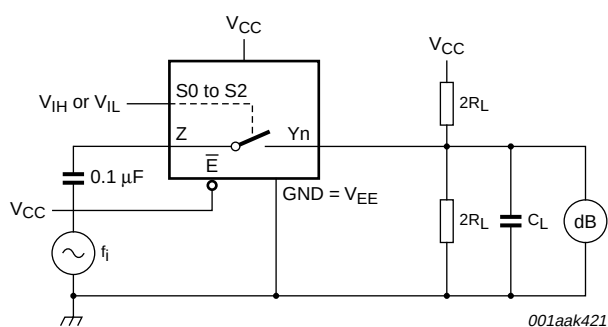
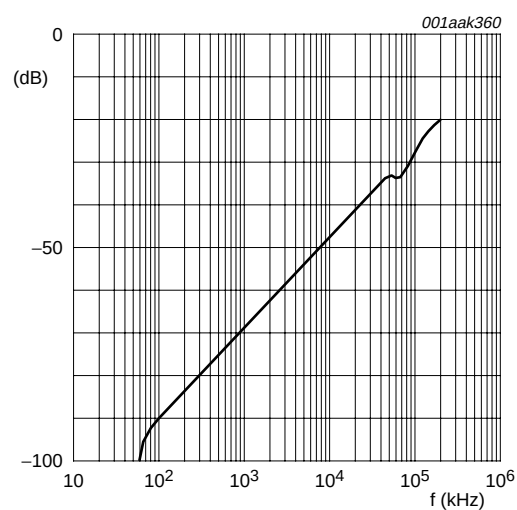


Fig 18. Test circuit for measuring isolation (OFF-state)



$V_{CC} = 3.0\text{ V}$; $GND = 0\text{ V}$; $V_{EE} = -3.0\text{ V}$; $R_L = 50\text{ }\Omega$;
 $R_{SOURCE} = 1\text{ k}\Omega$.

Fig 19. Typical isolation (OFF-state) as function of frequency

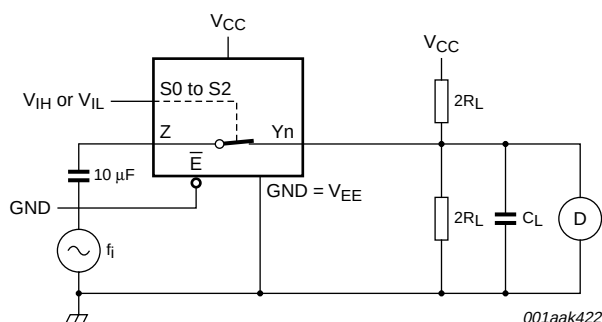
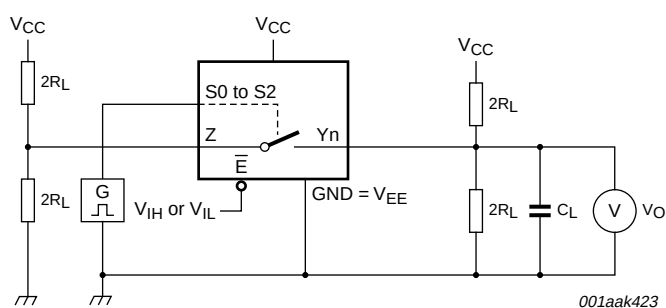
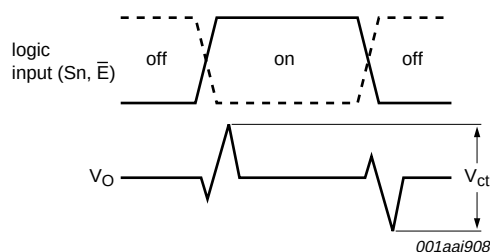


Fig 20. Test circuit for measuring total harmonic distortion



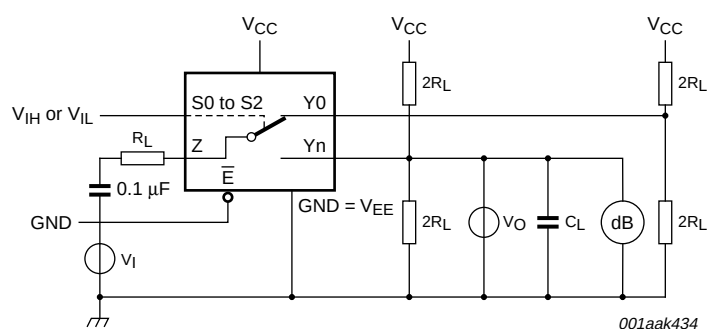
a. Test circuit



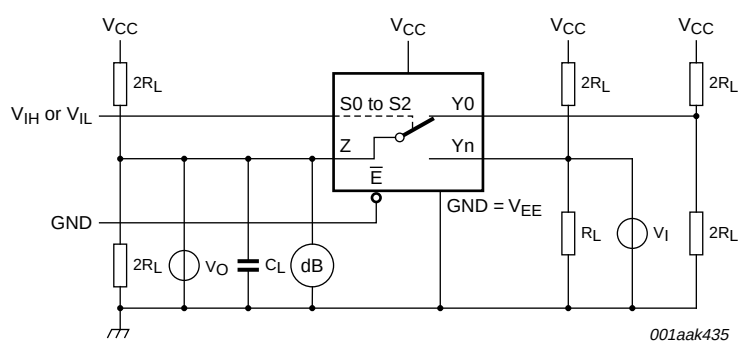
b. Input and output pulse definitions

V_I may be connected to S_n or $\bar{E}$.

Fig 21. Test circuit for measuring crosstalk voltage between digital inputs and switch



a. Switch closed condition



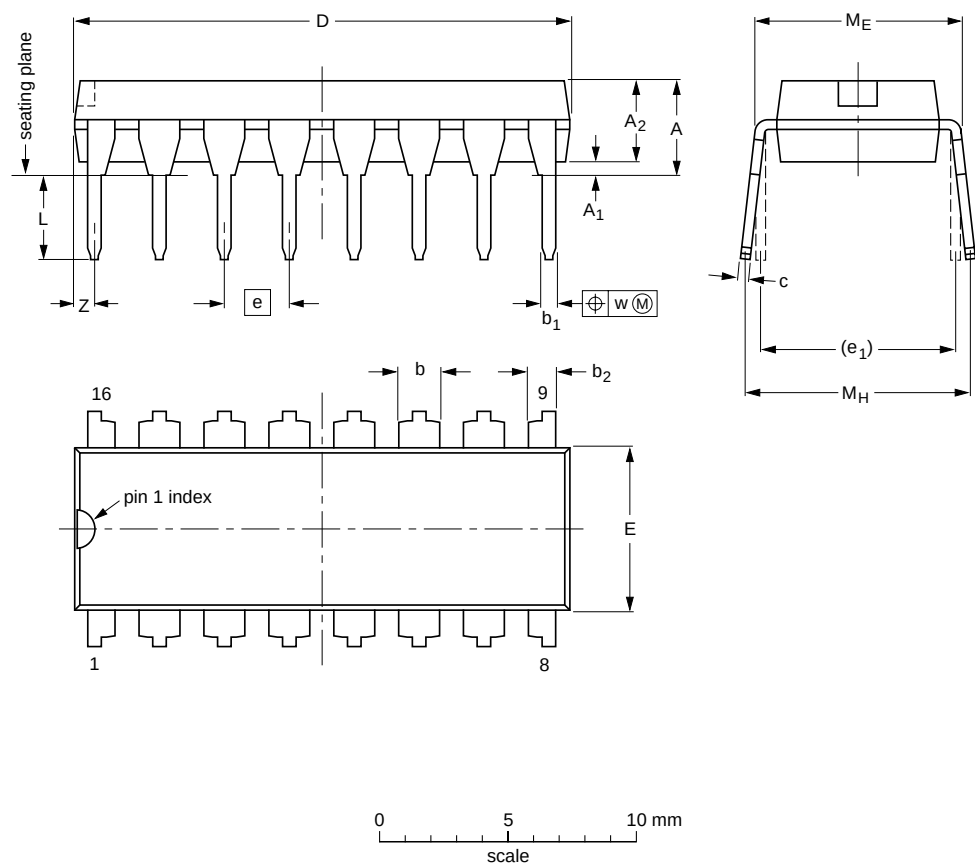
b. Switch open condition

Fig 22. Test circuit for measuring crosstalk between switches

11. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

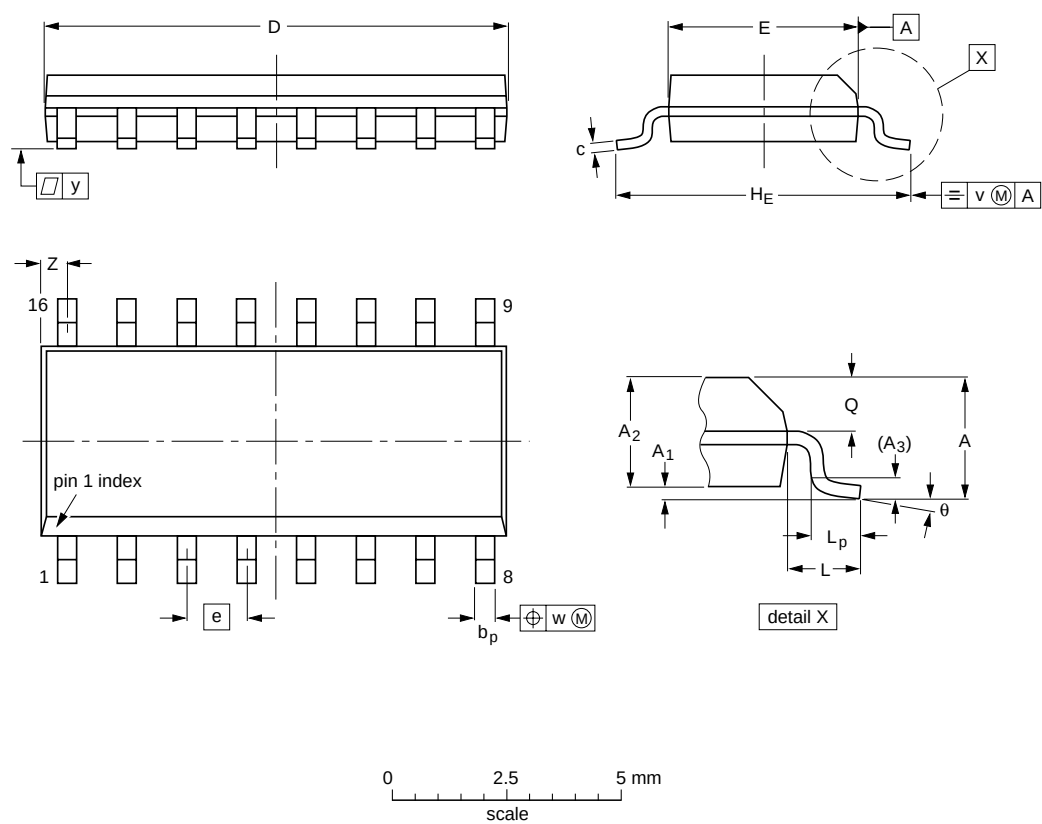
Note
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						95-01-14 03-02-13

Fig 23. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note
 1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 24. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

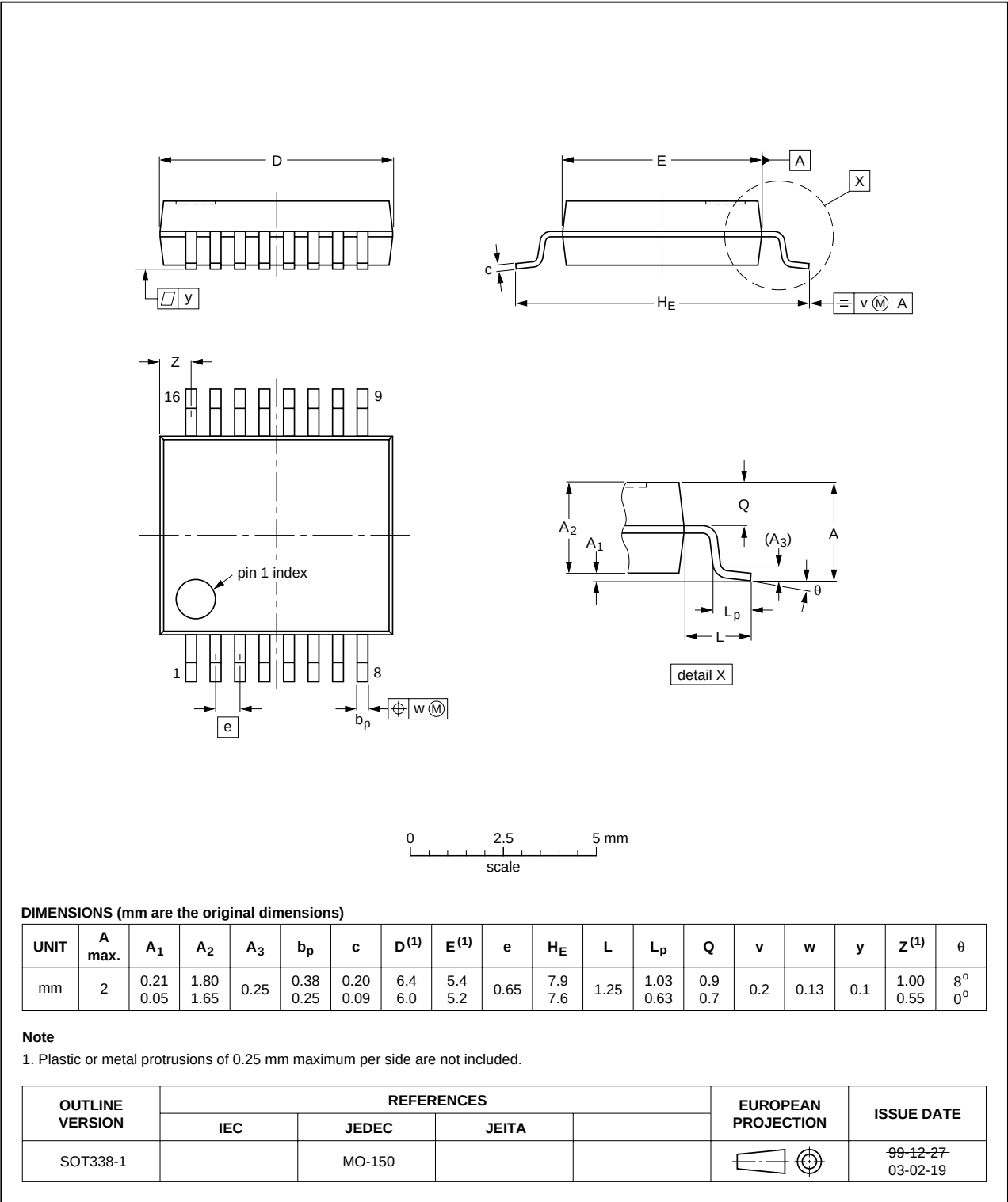


Fig 25. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

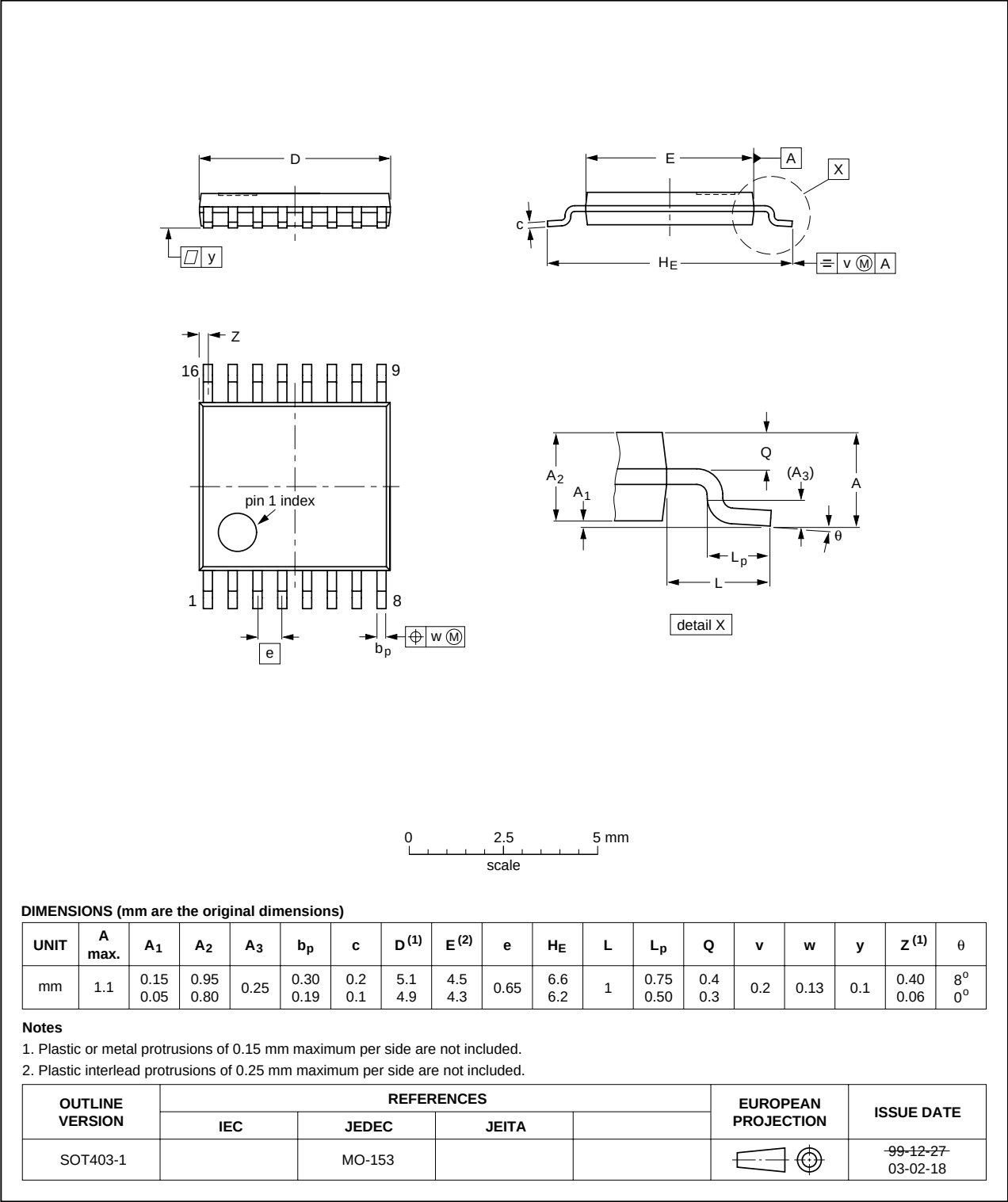


Fig 26. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

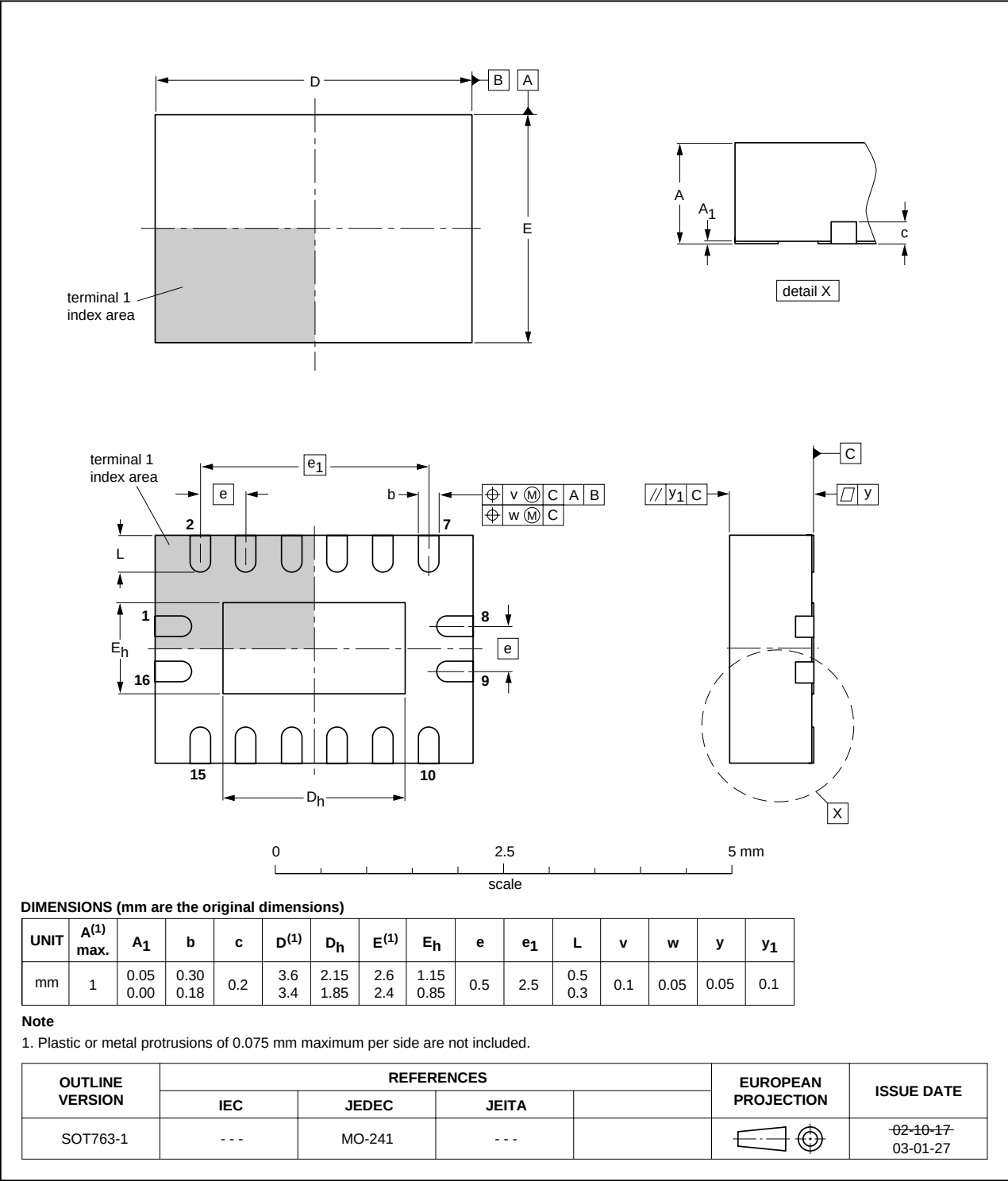


Fig 27. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4051_4	20090810	Product data sheet	-	74LV4051_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added type number 74LV4051BQ (DHVQFN16 package)			
74LV4051_3	19960623	Product specification	-	74LV4051_2
74LV4051_2	19970715	Product specification	-	74LV4051_1

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

14.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

14.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

15. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

16. Contents

1	General description	1
2	Features	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	4
5.1	Pinning	4
5.2	Pin description	4
6	Functional description	5
6.1	Function table	5
7	Limiting values	5
8	Recommended operating conditions	6
9	Static characteristics	7
9.1	Test circuits	8
9.2	ON resistance	8
9.3	On resistance waveform and test circuit.	10
10	Dynamic characteristics	11
10.1	Waveforms	13
10.2	Additional dynamic parameters	15
10.2.1	Test circuits	16
11	Package outline	19
12	Abbreviations	24
13	Revision history	24
14	Legal information	25
14.1	Data sheet status	25
14.2	Definitions	25
14.3	Disclaimers	25
14.4	Trademarks	25
15	Contact information	25
16	Contents	26

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

founded by

PHILIPS

© NXP B.V. 2009.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 10 August 2009

Document identifier: 74LV4051_4