

74LVT244B; 74LVTH244B

3.3 V octal buffer/line driver; 3-state

Rev. 8 — 8 July 2024

Product data sheet

1. General description

The 74LVT244B; 74LVTH244B is an 8-bit buffer/line driver with 3-state outputs. The device can be used as two 4-bit buffers or one 8-bit buffer. The device features two output enables (1OE and 2OE), each controlling four of the 3-state outputs. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs.

2. Features and benefits

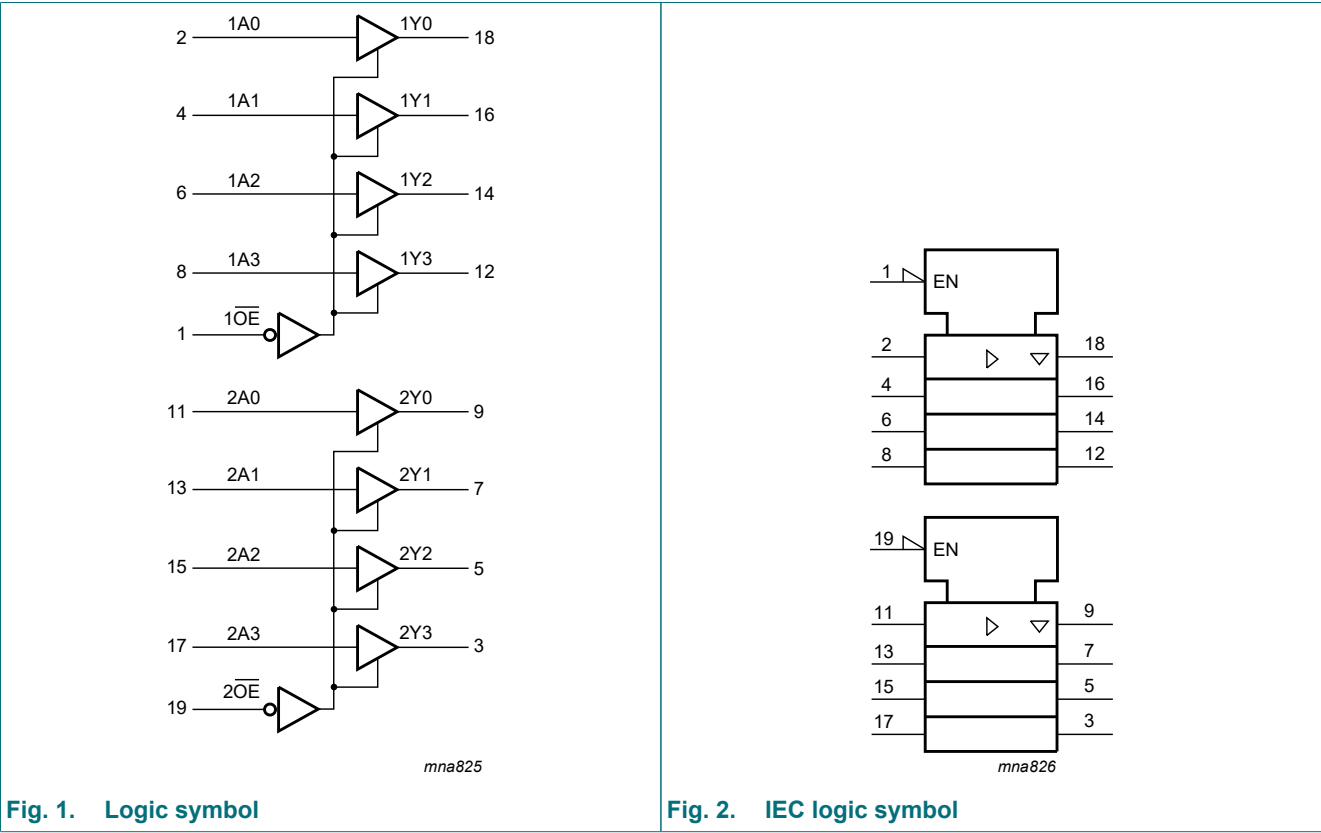
- Octal bus interface
- 3-state buffers
- Speed upgrade of 74LVT244A
- Wide supply voltage range from 2.7 to 3.6 V
- BiCMOS high speed and output drive
- Output capability: +64 mA and -32 mA
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- Live insertion and extraction permitted
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
 - JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

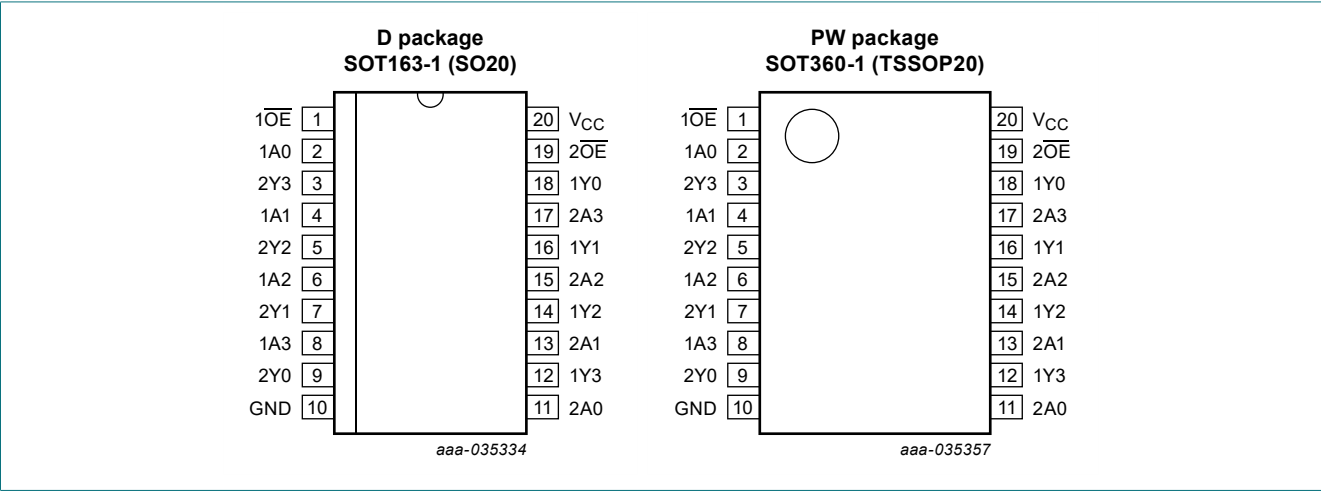
Type number	Package			
	Temperature range	Name	Description	Version
74LVT244BD 74LVTH244BD	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT244BPW 74LVTH244BPW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable input (active low)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	data output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	[1]	-0.5	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature	[2]	-	150	°C
P _{tot}	total power dissipation	T _{amb} = -40 to +85 °C	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.7	-	3.6	V
V _I	input voltage		0	-	5.5	V
I _{OH}	HIGH-level output current		-32	-	-	mA
I _{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f _i ≥ 1 kHz	-	-	64	mA
T _{amb}	ambient temperature	in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T _{amb} = -40 °C to +85 °C						
V _{IK}	input clamping voltage	V _{CC} = 2.7 V; I _{IK} = -18 mA	-1.2	-0.9	-	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _{CC} = 2.7 V; I _{OH} = -100 μA	V _{CC} - 2.0	V _{CC} - 2.1	-	V
		V _{CC} = 2.7 V; I _{OH} = -8 mA	2.4	2.5	-	V
		V _{CC} = 3.0 V; I _{OH} = -32 mA	2.0	2.2	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 2.7 V; I _{OL} = 100 μA	-	0.1	0.2	V
		V _{CC} = 2.7 V; I _{OL} = 24 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 16 mA	-	0.25	0.4	V
		V _{CC} = 3.0 V; I _{OL} = 32 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 64 mA	-	0.4	0.55	V
I _I	input leakage current	all input pins				
		V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	0.1	10	μA
		control pins				
		V _{CC} = 3.6 V; V _I = V _{CC} or GND	-1	±0.1	1	μA
		data pins [2]				
		V _{CC} = 3.6 V; V _I = V _{CC}	-	0.1	1	μA
I _{OFF}	power-off leakage current	V _{CC} = 3.6 V; V _I = 0 V	-5	-1	-	μA
		V _{CC} = 3.6 V; V _I = 0 V	-	-	-	μA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-100	1	+100	μA
I _{BHL}	bus hold LOW current	V _{CC} = 3 V; V _I = 0.8 V	75	130	-	μA
I _{BHH}	bus hold HIGH current	V _{CC} = 3 V; V _I = 2.0 V	-	-140	-75	μA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 3.6 V; V _I = 0 V to 3.6 V [3]	500	-	-	μA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 3.6 V; V _I = 0 V to 3.6 V	-	-	-500	μA
I _{EX}	external current	nYn output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.3 V	-	60	125	μA

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; $n\overline{OE} = \text{don't care}$ [4]	-100	± 1	+100	μA
I_{OZ}	OFF-state output current	$V_{CC} = 3.6\text{ V}$; $V_I = V_{IH}$ or V_{IL}				
		$V_O = 3.0\text{ V}$	-	1	5	μA
		$V_O = 0.5\text{ V}$	-5	-1	-	μA
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$				
		output HIGH	-	0.13	0.19	mA
		output LOW	-	2	5	mA
		outputs disabled [5]	-	0.13	0.19	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3.0\text{ V}$ to 3.6 V ; one input at $V_{CC} - 0.6\text{ V}$ and other inputs at V_{CC} or GND [6]	-	0.1	0.2	mA
C_I	input capacitance	$V_I = 0\text{ V}$ or 3.0 V	-	4	-	pF
C_O	output capacitance	outputs disabled; $V_O = 0\text{ V}$ or 3.0 V	-	8	-	pF

- [1] Typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$.
- [2] Unused pins at V_{CC} or GND.
- [3] This is the bus hold overdrive current required to force the input to the opposite logic state.
- [4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.
From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ a transition time of 100 μs is permitted. This parameter is valid for $T_{amb} = 25\text{ }^{\circ}\text{C}$ only.
- [5] I_{CC} is measured with outputs pulled to V_{CC} or GND.
- [6] This is the increase in supply current for each input at $V_{CC} - 0.6\text{ V}$.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$						
t_{PLH}	LOW to HIGH propagation delay	nAn to nYn; see Fig. 3				
		$V_{CC} = 2.7\text{ V}$	-	-	3.8	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	1.1	1.9	3.5	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to nYn; see Fig. 3				
		$V_{CC} = 2.7\text{ V}$	-	-	3.6	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	1.3	2.0	3.3	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nYn; see Fig. 4				
		$V_{CC} = 2.7\text{ V}$	-	-	5.3	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	1.1	2.8	4.5	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nYn; see Fig. 4				
		$V_{CC} = 2.7\text{ V}$	-	-	4.9	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	1.4	2.3	4.4	ns

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t _{PHZ}	HIGH to OFF-state propagation delay	n $\overline{\text{OE}}$ to nYn; see Fig. 4				
		V _{CC} = 2.7 V	-	-	4.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.9	2.9	4.4	ns
t _{PLZ}	LOW to OFF-state propagation delay	n $\overline{\text{OE}}$ to nYn; see Fig. 4				
		V _{CC} = 2.7 V	-	-	4.4	ns
		V _{CC} = 3.0 V to 3.6 V	1.8	2.5	4.4	ns

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

10.1. Waveforms and test circuit

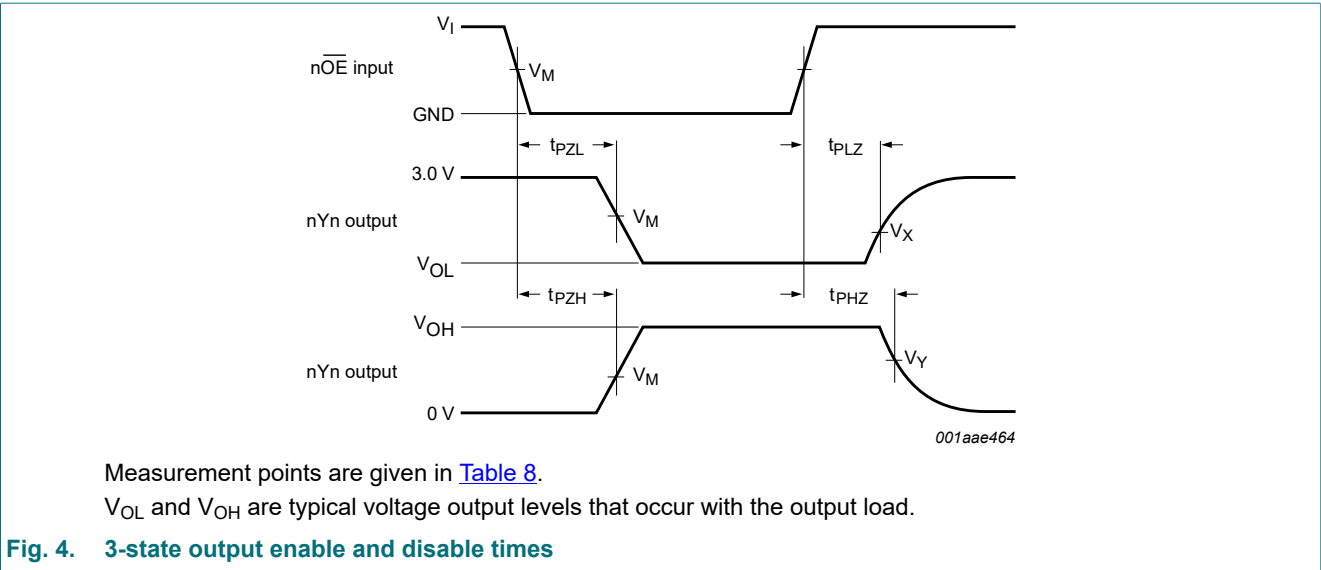
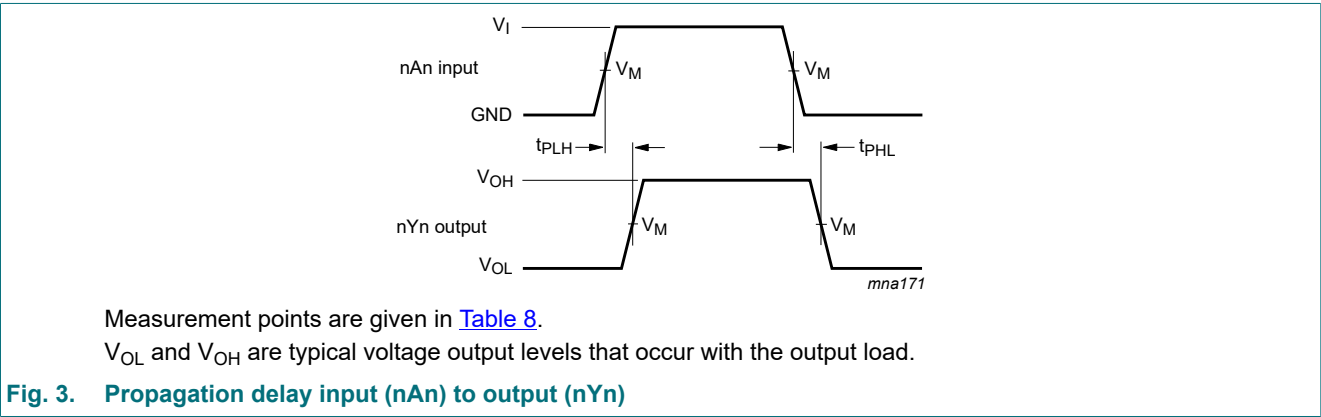


Table 8. Measurement points

Input	Output		
V _M	V _M	V _X	V _Y
1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V

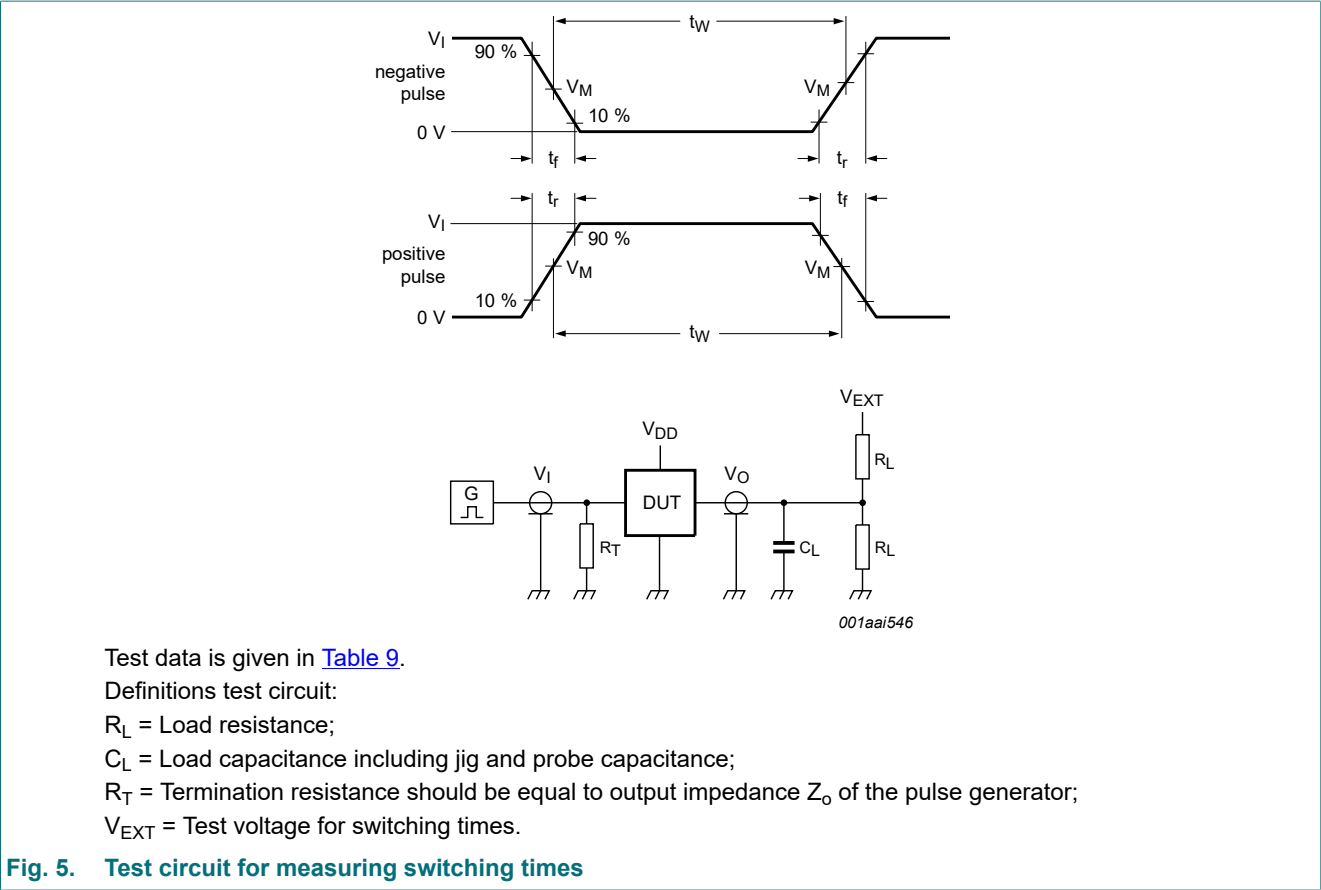


Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

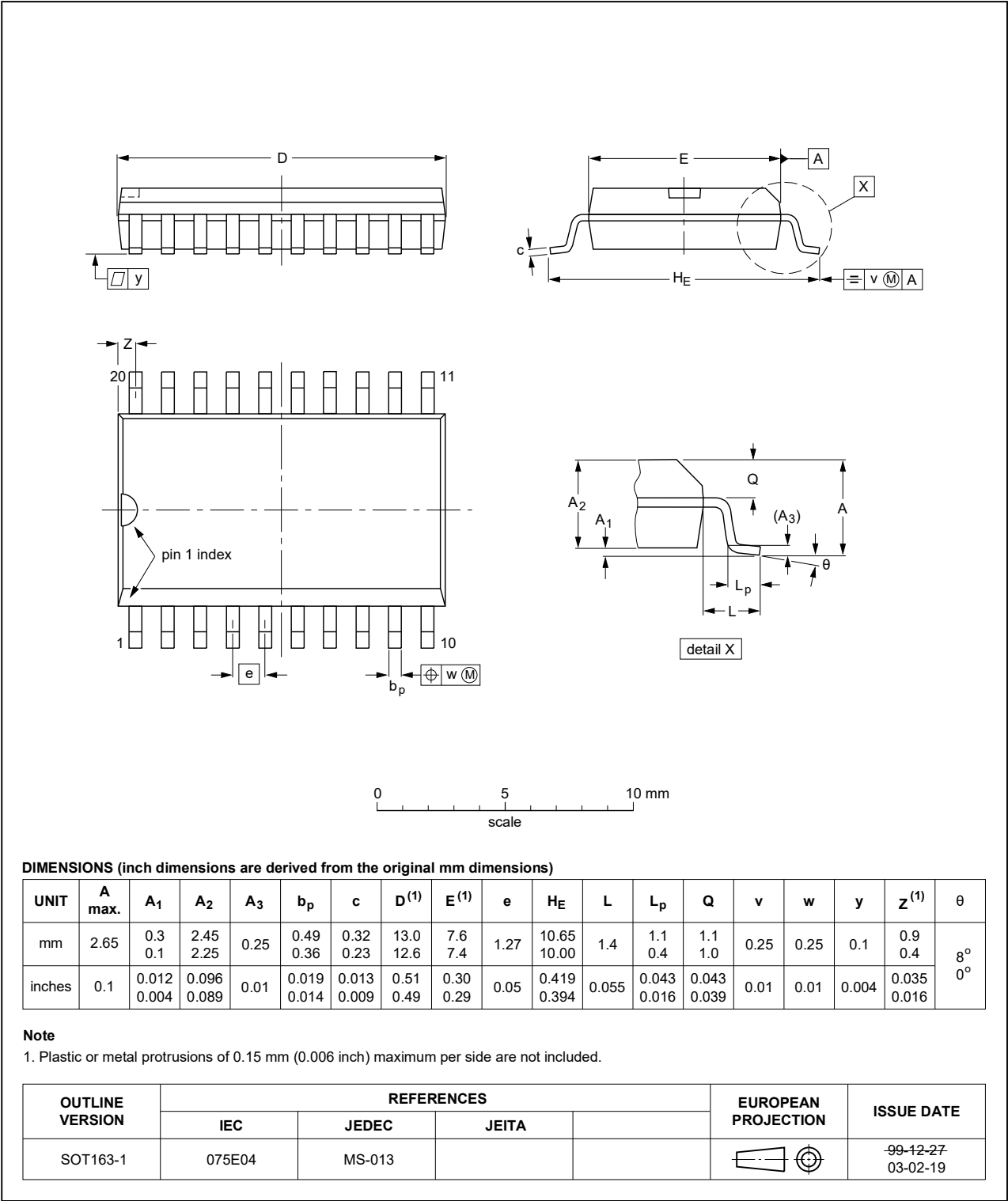


Fig. 6. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

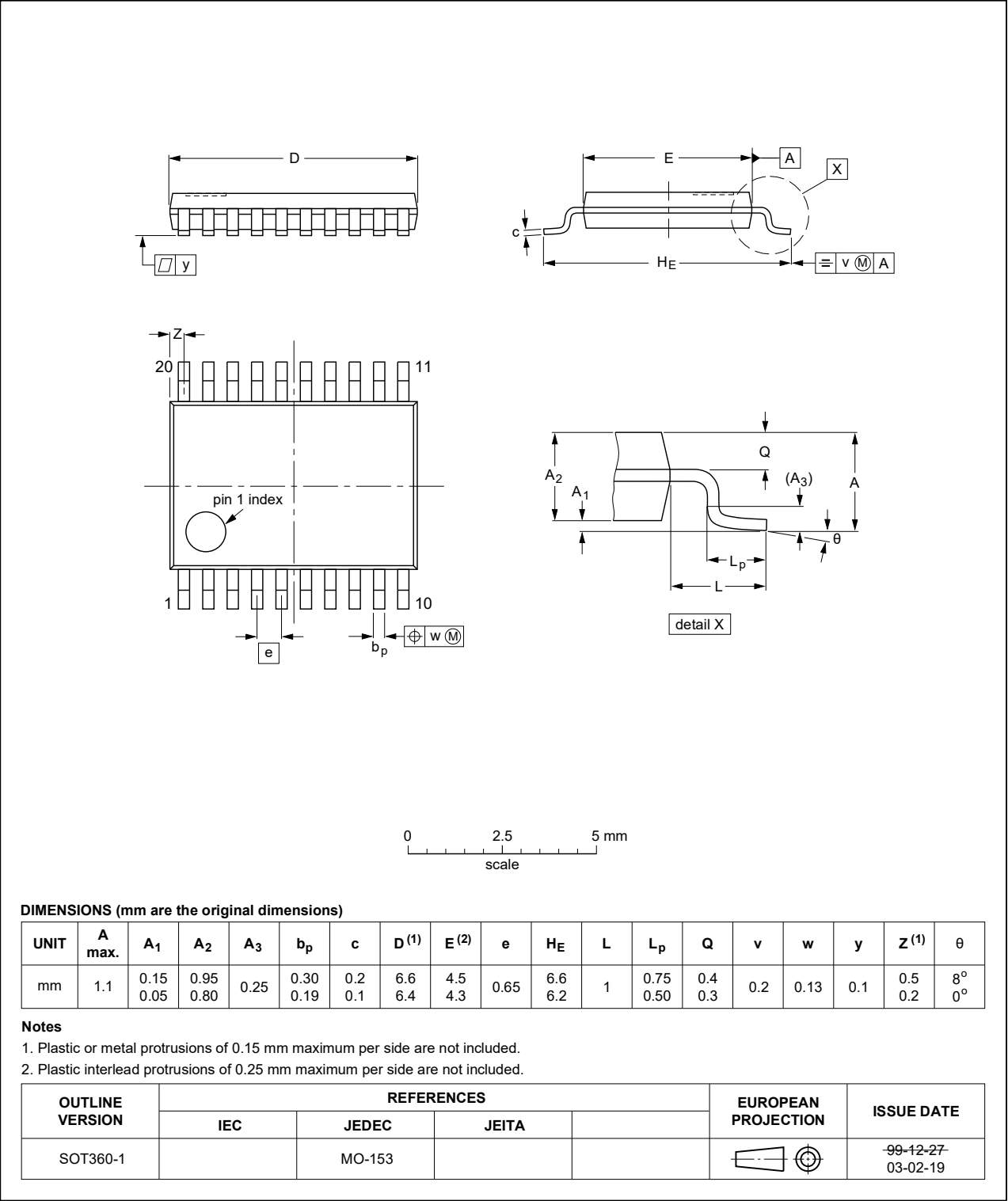


Fig. 7. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH244B v.7	20240708	Product data sheet	-	74LVT_LVTH244B v.6
Modifications:	Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVT_LVTH244B v.6	20210812	Product data sheet	-	74LVT_LVTH244B v.5
Modifications:	Type number 74LVT244BDB (SOT339-1/SSOP20) removed.			
74LVT_LVTH244B v.5	20210212	Product data sheet	-	74LVT_LVTH244B v.4
Modifications:	- Type number 74LVTH244BDB (SOT339-1 / SSOP20) removed. Section 1 and Section 2 updated.			
74LVT_LVTH244B v.4	20170614	Product data sheet	-	74LVT_LVTH244B v.3
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate.			
74LVT_LVTH244B v.3	20060303	Product data sheet	-	74LVT244B v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Section 3: Added type numbers 74LVTH244BD, 74LVTH244BDB and 74LVTH244BPW.			
74LVT244B v.2	20030919	Product specification	-	74LVT244B v.1
74LVT244B v.1	19981101	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Ordering information..... 1

4. Functional diagram..... 2

5. Pinning information..... 2

5.1. Pinning..... 2

5.2. Pin description..... 3

6. Functional description..... 3

7. Limiting values..... 3

8. Recommended operating conditions..... 4

9. Static characteristics..... 4

10. Dynamic characteristics..... 5

10.1. Waveforms and test circuit..... 6

11. Package outline..... 8

12. Abbreviations..... 10

13. Revision history..... 10

14. Legal information..... 11

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