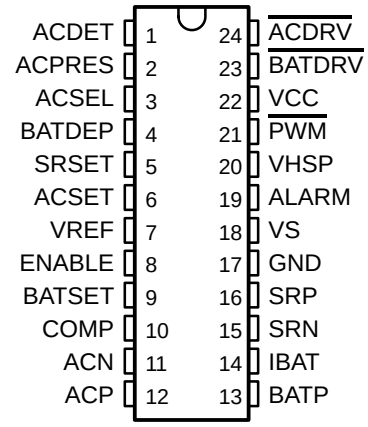
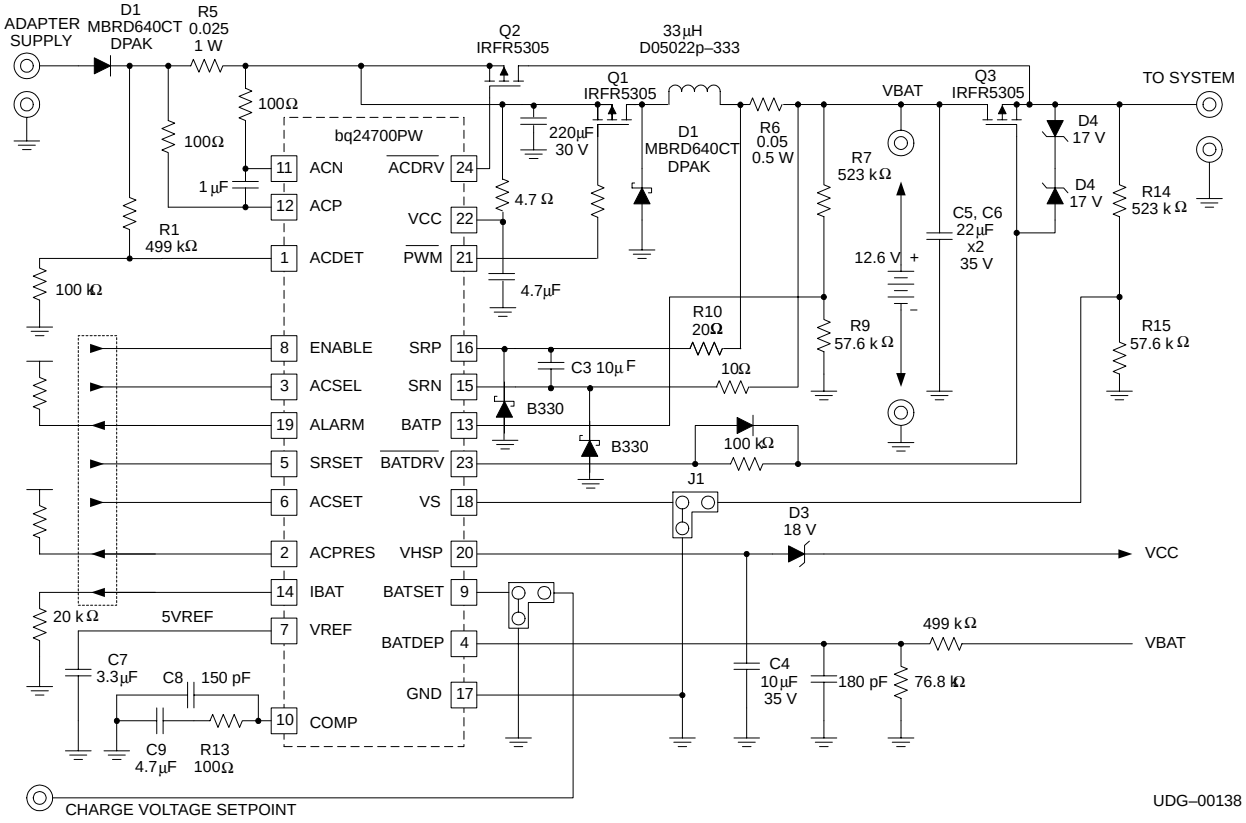
- **Dynamic Power Management, DPM Minimizes Battery Charge Time**
- **Integrated Selector Supports Battery Conditioning and Smart Battery Learn Cycle**
- **Selector Feedback Circuit Insures Break-Before-Make Transition**
- **±0.4% Charge Voltage Accuracy, Suitable for Charging Li-Ion Cells**
- **±4% Charge Current Accuracy**
- **300-kHz Integrated PWM Controller for High-Efficiency Buck Regulation**
- **Depleted Battery Detection and Indication to Protect Battery From Over Discharge**
- **15-μA Sleep Mode Current for Low Battery Drain**
- **Designed for Charge Management of NiCd/NiMH and Li-Ion/Li-Pol Battery Packs**
- **24-Pin TSSOP Package**

PW PACKAGE
(TOP VIEW)



application schematic



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description

The bq24700/bq24701 is a highly integrated battery charge controller and selector tailored for the notebook and sub-notebook PC applications.

The bq24700/bq24701 uses dynamic power management (DPM) to minimize battery charge time by maximizing use of available wall-adapter power. This is achieved by dynamically adjusting the battery charge current based on the total system (adapter) current.

The bq24700/bq24701 uses a fixed frequency, pulse width modulator (PWM) to accurately control battery charge current and voltage. Charge current limits can be programmed from a keyboard controller DAC or by external resistor dividers from the precision 5-V, ±0.6%, externally bypassed voltage reference (VREF), supplied by the bq24700/bq24701.

The battery voltage limit can be programmed by using the internal 1.25-V, ±0.5% precision reference, making it suitable for the critical charging demands of lithium-ion cells. Also, the bq24700/bq24701 provides an option to override the precision 1.25-V reference and drive the error amplifier either directly from an external reference or from a resistor divider off the 5 V supplied by the integrated circuit.

The selector function allows the manual selection of the system power source, battery or wall-adapter power. The bq24700 supports battery-conditioning and battery-lean cycles through the ACSEL function. The ACSEL function allows manual selection of the battery or wall power as the main system power. It also provides autonomous switching to the remaining source (battery or ac power) should the selected system power source terminate (refer to Table 1 for the differences between the bq24700 and the bq24701). The bq24700/bq24701 also provides an alarm function to indicate a depleted battery condition.

The bq24700/bq24701 PWM controller is ideally suited for operation in a buck converter for applications when the wall-adapter voltage is greater than the battery voltage.

AVAILABLE OPTIONS

Condition **–40 C T_A 85 C**	**Selector Operation**	
	bq24700PW	**bq24701PW**
Battery as Power Source		
Battery removal	Automatically selects ac	Automatically selects ac
Battery reinserted	Selection based on selector inputs	Selection based on selector inputs
ac as Power Source		
AC removal	Automatically selects battery	Automatically selects battery
AC reinserted	Selection based on selector inputs	Selection based on selector inputs
Depleted Battery Condition		
Battery as power source	Sends ALARM signal	**Automatically selects ac** Sends ALARM signal
AC as power source	Sends ALARM signal	Sends ALARM signal
ALARM Signal Active		
	Depleted battery condition	Depleted battery condition
	Selector inputs do not match selector outputs	

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

Supply voltage range: VCC . . . . . –0.3 V to 20 V
Battery voltage range: SRP, SRN . . . . . –0.3 V to 19 V
Input voltage: ACN, ACP . . . . . –0.3 V to 20 V
Virtual junction temperature range, T_J . . . . . –40°C to 85°C
Storage temperature range T_{stg} . . . . . –65°C to 150°C
Lead temperature (Soldering, 10 seconds) . . . . . 300°C

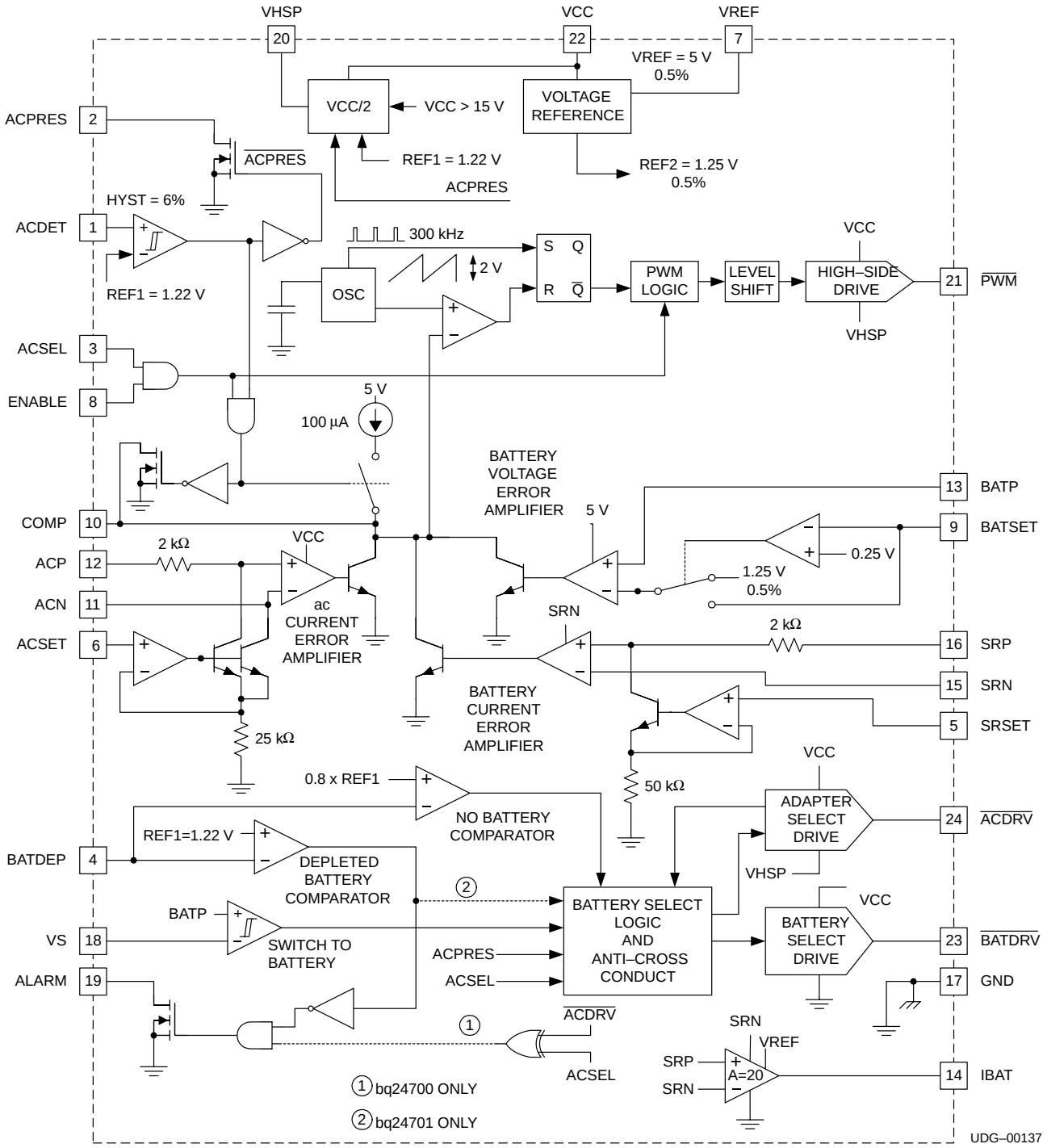
† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to ground. Currents are positive into and negative out of the specified terminals. Consult the *Packaging* section of the databook for thermal limitations and considerations of the package.

recommended operating conditions ($T_A = T_{OPR}$) all voltages relative to Vss

		MIN	MAX	UNIT
Supply voltage, (VCC)	Analog and PWM operation	7.0	20	V
	Selector operation	4.5	20	
Negative ac current sense, (ACN)		7.0	20	V
Positive ac current sense, (ACP)		7.0	20	V
Negative battery current sense, (SRN)		5.0	18	V
Positive battery current sense, (SRP)		5.0	18	V
AC or adapter power detection (ACDET)		–0.3	8	V
AC power indicator (ACPRES)		–0.3	8	V
AC adapter power select (ACSEL)		–0.3	8	V
Depleted battery level (BATDEP)		–0.3	8	V
Battery charge current programming voltage (SRSET)		–0.3	8	V
Charge enable (ENABLE)		–0.3	8	V
External override to an internal 0.5% precision reference (BATSET)		–0.3	8	V
Inverting input to the PWM comparator (COMP)		–0.3	8	V
Battery charge regulation voltage measurement input to the battery—voltage g_m amplifier (BATP)		–0.3	8	V
Battery current differential amplifier output (IBAT)		–0.3	8	V
System load voltage input pin (VS)		–0.3	8	V
Depleted battery alarm output (ALARM)		–0.3	8	V
Gate drive output ($\overline{PWM}$)		–0.3	20	V
Battery power source select output ($\overline{BATDRV}$)		–0.3	20	V
AC or adapter power source selection output ($\overline{ACDRV}$)		–0.3	20	V
Operating free–air temperature, T_A		–40	85	°C

block diagram



electrical characteristics ($T_A = T_{OPR}$, 7.0 Vdc V_{CC} 20.0 Vdc, all voltages relative to V_{SS}) (unless otherwise specified)

quiescent current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DDOP}	Total chip operating current, switching and no load on PWMB	ACPRES = High, PWM ON, V_{CC} = 30 V	1	3	6	mA
I_{SLEEP}	Total battery sleep current, ac not present	ACPRES = Low, V_{CC} = SRN = 18 V		15	22	µA

logic interface dc characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage (ACPRES, ALARM)	I_{OL} = 1 mA			0.4	V
V_{IL}	Low–level input voltage (ACSEL, ENABLE)				0.8	V
V_{IH}	High-level input voltage (ACSEL, ENABLE)		1.8			V
I_{SINK1}	Sink current (ACPRES)	V_{OL} = 0.4	2	5	8	mA
I_{SINK2}	Sink current (ALARM)	V_{OL} = 0.4	0.75	1.5	3.5	mA

pwm oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{OSC(PWM)}$	Oscillator frequency	0°C ≤ T_A ≤ 85°C	260	300	340	kHz
		–40°C ≤ T_A ≤ 0°C	240	300	340	
	Maximum duty cycle		100%			
	Input voltage for maximum dc (COMP)		3.8			V
	Minimum duty cycle				0%	
	Input voltage for minimum dc (COMP)				0.8	V
V_{RAMP}	Oscillator ramp voltage (peak-to-peak)	0°C ≤ T_A ≤ 85°C	1.85	2.15	2.30	
		–40°C ≤ T_A ≤ 0°C	1.60	2.15	2.30	
$V_{IK(COMP)}$	Internal input clamp voltage (tracks COMP voltage for maximum dc)			3.8	4.5	
$I_{S(COMP)}$	Internal source current (COMP)	Error amplifier = OFF, V_{COMP} = 1 V	70	110	140	µA

leakage current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{L\_\overline{ACDET}}$	Leakage current, $\overline{ACDET}$				1	µA
I_{L_SRSET}	Leakage current, SRSET				1	µA
I_{L_ACSET}	Leakage current, ACSET				1	µA
I_{L_BATDEP}	Leakage current, BATDEP				1	µA
I_{L_VS}	Leakage current, VS				1	µA

electrical characteristics ($T_A = T_{OPR}$, 7.0 Vdc V_{CC} 20.0 Vdc, all voltages relative to V_{SS}) (unless otherwise specified) (continued)

battery current-sense amplifier

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
g_m	Transconductance gain		90	150	210	mA/V
CMRR	Common-mode rejection ratio	See Note 1		90		dB
V_{ICR}	Common-mode input (SRP) voltage range	VCC = SRN + 2 V	5		18.2	V
I_{SINK}	Sink current (COMP)	COMP = 1 V, (SRP – SRN) = 10 mV	0.5	1.5	2.5	mA
I_{IB}	Input bias current (SRP)	VSRP = 16 V, SRSET = 0 V, VCC = 20		6	10	μA
	Input bias current (SRN)	VSRP = 16 V, SRSET = 0 V, VCC = 20		200	300	
V_{SET}	Battery current programming voltage (SRSET)		0		2.5	V
A_V	Battery current set gain	0.65 V ≤ SRSET ≤ 2.5 V, 8 V ≤ SRN ≤ 16 V, –40°C ≤ T_A ≤ 85°C, See Note 2	24	25	26	V/V
	Total battery current-sense mid-scale accuracy	SRSET = 1.25 V, T_A = 25°C, See Note 3	–5%		5%	
		SRSET = 1.25 V, –40°C ≤ T_A ≤ 85°C, See Note 3	–6%		6%	
	Total battery current-sense full-scale accuracy	SRSET = 2.5 V, T_A = 25°C, See Note 3	–3%		3%	
		SRSET = 2.5 V, –40°C ≤ T_A ≤ 85°C, See Note 3	–4%		4%	

NOTES: 1. Ensured by design. Not production tested.

2. $I_{BAT} = \frac{SRSET}{R_{SENSE}} \times \frac{1}{A_V}$

3. Total battery-current set is based on the measured value of (SRP–SRN) = Δm, and the calculated value of (SRP–SRN) = ΔC, using the measured gain, A_V. $\Delta C = \frac{SRSET}{A_V}$, Total accuracy in % $= \frac{(\Delta m - \Delta c)}{\Delta c} \times 100$

electrical characteristics ($T_A = T_{OPR}$, 7.0 Vdc V_{CC} 20.0 Vdc, all voltages relative to V_{SS}) (unless otherwise specified) (continued)

adapter current-sense amplifier

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
g_m	Transconductance gain		90	150	210	mA/V
CMRR	Common-mode rejection ratio	See Note 1		90		dB
V_{ICR}	Common-mode input voltage range (ACP)		7.0		V_{CC}+0.2	V
I_{SINK}	Sink current (COMP)	COMP = 1 V, (ACP – ACN) = 10 mV	0.5	1.5	2.5	mA
I_{IB}	Input bias current (ACP, ACN)	ACP = ACN = 20 V, SRSET = 0 V, VCC = 20 V, ACSET = 1.25 V	15	25	35	µA
	Input bias current accuracy ratio (ACP, ACN)	ACP = ACN = 20 V, VCC = 20 V, ACSET = 1.25 V	0.95	1.00	1.05	
V_{SET}	AC current programming voltage (ACSET)		0		2.5	V
A_V	AC current set gain	0.65 V ≤ ACSET ≤ 2.5 V, 12 V ≤ ACP ≤ 20 V, –40°C ≤ T_A ≤ 85°C, See Note 4	24.5	25.5	26.5	V/V
	Total ac current-sense mid-scale accuracy	ACSET = 1.25 V, T_A = 25°C, See Note 5	–5%		5%	
		ACSET = 1.25 V, –40°C ≤ T_A ≤ 85°C, See Note 5	–6%		6%	
	Total ac current-sense full-scale accuracy	ACSET = 2.5 V, T_A = 25°C, See Note 5	–3.5%		3.5%	
		ACSET = 2.5 V, –40°C ≤ T_A ≤ 85°C, See Note 5	–4%		4%	

battery voltage error amplifier

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
g_m	Transconductance gain		75	135	195	mA/V
CMRR	Common-mode rejection ratio	See Note 1		90		dB
V_{ICR}	BATSET common-mode input voltage range		1		2.5	V
V_{IT}	Internal reference override input threshold voltage		0.20	0.25	0.30	V
I_{SINK}	Sink current COMP	COMP = 1 V, (BATP – BATSET) = 10 mV, BATSET = 1.25 V	0.5	1.5	2.5	mA
V_{FB}	Error-amplifier precision reference voltage	T_A = 25°C	1.241	1.246	1.251	V
		0°C ≤ T_A ≤ 70°C	1.239	1.246	1.252	
		–40°C ≤ T_A ≤ 85°C	1.234	1.246	1.254	

NOTES: 1. Ensured by design. Not production tested.

2. $I_{BAT} = \frac{SRSET}{R_{SENSE}} \times \frac{1}{A_V}$

3. Total battery-current set is based on the measured value of (SRP–SRN) = Δm, and the calculated value of (SRP–SRN) = ΔC, using the measured gain, A_V. $\Delta c = \frac{SRSET}{A_V}$, Total accuracy in % $= \frac{(\Delta m - \Delta c)}{\Delta c} \times 100$

4. Calculation of the AC current: $I_{AC} = \frac{ACSET}{R_{SENSE}} \times \frac{1}{A_V}$

5. Total ac-current set accuracy is based on the measured value of (ACP–ACN) = Δc, using the measured gain, A_V. $\Delta c = \frac{ACSET}{A_V}$, Total accuracy in % $= \frac{(\Delta m - \Delta c)}{\Delta c} \times 100$

electrical characteristics ($T_A = T_{OPR}$, 7.0 Vdc V_{CC} 20.0 Vdc, all voltages relative to V_{SS}) (unless otherwise specified) (continued)

battery current output amplifier

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{TR}	Transfer gain	(SRP – SRN) = 50 mV, See Note 6	5		18.2	V
V_{IBAT}	Battery current readback output voltage (IBAT)	(SRP – SRN) = 50 mV, SRP = 12 V, VCC = 18 V, T_A = 25°C	0.97	1.00	1.03	V
	Line rejection voltage	T_A = 25°C		10		mV/V
CM	Common-mode input range (SRP)		5		18.2	V
$V_{O(IBAT)}$	Battery current output voltage range (IBAT)		0		2.5	V
$I_{S(O)}$	Output source current (IBAT)	(SRP – SRN) = 100 mV	150	600	1200	µA
	Total battery current readback mid-scale accuracy	(SRP – SRN) = 50 mV, T_A = 25°C, See Note 7	–4%		4%	
		(SRP – SRN) = 50 mV, –40°C ≤ T_A ≤ 85°C, See Note 7	–6%		6%	
	Total battery current readback full-scale accuracy	(SRP – SRN) = 100 mV, T_A = 25°C, See Note 7	–6%		6%	
		(SRP – SRN) = 100 mV, –40°C ≤ T_A ≤ 85°C, See Note 7	–8%		8%	

5-V voltage reference

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Output voltage (VREF)	0°C ≤ T_A ≤ 70°C	5.000	5.030	5.060	V
		–40°C ≤ T_A ≤ 85°C	4.960	5.030	5.070	V
	Line regulation			0.15	0.37	mV/V
	Load regulation	1 mA ≤ I_{LOAD} ≤ 5 mA		1.0	2.5	mV/mA
	Short circuit current		8	18	30	mA

half supply regulator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HSP(on)}$	VCC up-threshold for half supply regulation		14.5	15.5	16.5	V
	VCC hysteresis for half supply regulation		–7.2%	–6.5%	–6%	
VHSP/V_{CC}	Voltage regulation	VCC ≥ $V_{HSP(on)}$, 16.5 V ≤ VCC ≤ 20 V	0.45	0.50	0.55	
VHSP		VCC < $V_{HSP(on)}$, 7 V ≤ VCC ≤ 14.5 V			2.0	V

NOTES: 6. Battery readback transfer gain $G_{TR} = \frac{V_{IBAT}}{(SRP - SRN)}$

7. Total battery current readback accuracy is based on the measured value of VIBAT, VIBATm, and the calculated value of VIBAT, VIBATc, using the measured value of the transfer gain, GTR.

$$V_{IBATc} = (SRP - SRN) \times GTR \quad \text{Total Accuracy in \%} = \frac{V_{IBATm} - V_{IBATc}}{V_{IBATm}} \times 100$$

electrical characteristics ($T_A = T_{OPR}$, 7.0 Vdc V_{CC} 20.0 Vdc, all voltages relative to V_{SS}) (unless otherwise specified) (continued)

MOSFET gate drive

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	AC driver $R_{DS(on)}$ high	V_{CC} = 18 V		150	250	Ω
	AC driver $R_{DS(on)}$ low	V_{CC} = 18 V		60	120	Ω
	Battery driver $R_{DS(on)}$ high	V_{CC} = 18 V		200	370	Ω
	Battery driver $R_{DS(on)}$ low	V_{CC} = 18 V		100	170	Ω
t_{Da}	Time delay from ac driver off to battery driver on	ACSEL 2.4 V ⇓ 0.2 V		0.5	1.5	µs
t_{Db}	Time delay from battery driver off to ac driver on	ACSEL 0.2 V ⇑ 2.4 V		1.0	2.0	µs
V_{OH}	PWM driver high-level output voltage	I_{OUT} = –10 mA, VCC = 18 V	–0.12	–0.07		V
		I_{OUT} = –100 mA, VCC = 18 V	–1.2	–0.7		
	PWM driver $R_{DS(on)}$ high			7	14	Ω
V_{OL}	PWM driver low-level output voltage	I_{OUT} = 10 mA, VCC = 18 V		V_{HSP}+0.04	V_{HSP}+0.1	V
		I_{OUT} = 100 mA, VCC = 18 V		V_{HSP}+0.5	V_{HSP}+0.9	
	PWM driver $R_{DS(on)}$ low			4	8	Ω

selector

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ACPRES}	AC presence detect voltage	See Note 9	1.165	1.220	1.275	V
$V_{IT(ACPRES)}$	AC presence hysteresis		40	80	120	mV
$t_{d(ALMON)}$	ACSEL high to alarm set high in ac fault time delay	ACSEL 0.2 V ⇑ 2.4 V		5	10	µs
$t_{d(ALMOFF)}$	ACSEL low to alarm reset low in ac fault time delay	SRN = SRP = 8 V, ACSEL 2.4 V ⇓ 0.2 V		2	10	µs
V_{BATDEP}	Battery depletion ALARM trip voltage	See Note 8	1.165	1.220	1.275	V
V_{NOBAT}	No battery detect, switch to ACDRV	See Note 8	0.87	0.98	1.07	V
t_{BATSEL}	Battery select time (ACSEL low to BATDRV low)	VS < BATP, ACSEL 2.4 V ⇓ 0.2 V	0.2		3.0	µs
t_{ACSEL}	AC select time (ACSEL high to ACDRV low)	ACSEL 0.2 V ⇑ 2.4 V	0.2		3.0	µs
V_{VS}	VS voltage to enable BATDRV	BATP = 1 V	0.96		1.02	V
$V_{IT(VS)}$	VS voltage hysteresis	VS > BATP	30		110	mV

NOTES: 8. Refer to Table 1 to determine the logic operation of the bq24700 and the bq24701.

9. Maximum ac adapter voltage (VCC) and AC presence detect voltage are 18 V.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ACDET	1	I	AC or adapter power detection
$\overline{\text{ACDRV}}$	24	O	AC or adapter power source selection output
ACN	11	I	Negative differential input
ACP	12	I	Positive differential input
ACPRES	2	O	AC power indicator
ACSEL	3	I	AC adapter power select
ACSET	6	I	Adapter current programming voltage
ALARM	19	O	Depleted battery alarm output
BATDEP	4	I	Depleted battery level
$\overline{\text{BATDRV}}$	23	O	Battery power source select output
BATP	13	I	Battery charge regulation voltage measurement input to the battery-voltage g_m amplifier
BATSET	9	I	External override to an internal 0.5% precision reference
COMP	10	O	Inverting input to the PWM comparator
ENABLE	8	I	Charge enable
GND	17	O	Supply return and ground reference
IBAT	14	O	Battery current differential amplifier output
$\overline{\text{PWM}}$	21	O	Gate drive output
SRN	15	I	Negative differential battery current sense amplifier input
SRP	16	I	Positive differential battery current sense amplifier input
SRSET	5	I	Battery charge current programming voltage
VCC	22	I	Operational supply voltage
VHSP	20	O	Voltage source to drive gates of the external MOSFETs
VREF	7	O	Precision voltage 5-V, ±0.6% reference
VS	18	I	System (load) voltage input pin

pin assignments

ACDET: AC or adapter power detection. This input pin is used to determine the presence of the ac adapter. When the voltage level on the ACDET pin is less than 1.20 V, the bq24700/bq24701 is in sleep mode, the PWM control is disabled, the $\overline{\text{BATDRV}}$ is driven low and the $\overline{\text{ACDRV}}$ is driven high. This feature can be used to automatically select battery as the system's power source.

$\overline{\text{ACDRV}}$: AC or adapter power source select output. This pin drives an external P-channel MOSFET used to switch to the ac wall-adapter as the system's power source. When the ACSEL pin is high while the voltage on the ACDET pin is greater than 1.20 V, the output $\overline{\text{ACDRV}}$ pin is driven low (V_{HSP}). This pin is driven high (V_{CC}) when the ACDET is less than 1.20 V.

ACN, ACP: Negative and positive differential inputs, respectively for ac-to-dc adapter current sense resistor.

ACPRES: This open-drain output pin is used to indicate the presence of ac power. A logic high indicates there is a valid ac input. A low indicates the loss of ac power. ACPRES is high when the voltage level on the ACDET pin is greater than 1.20 V.

ACSEL: AC adapter power select. This input selects either the ac adapter or the battery as the power source. A logic high selects ac power, while a logic low selects the battery.

pin assignments (continued)

ACSET: Adapter current programming voltage. This input sets the system current level at which dynamic power management occurs. Adapter currents above this programmed level activate the dynamic power management and proportionally reduce the available power to the battery.

ALARM: Depleted battery alarm output. This open-drain pin indicates that a depleted battery condition exists. A pullup on ALARM goes high when the voltage on the BATDEP pin is below 1.20 V. On the bq24700, the ALARM output also activates when the selector inputs do not match the selector state.

BATDEP: Depleted battery level. A voltage divider network from the battery to BATDEP pin is used to set the battery voltage level at which depletion is indicated by the ALARM pin. See ALARM pin for more details. A battery depletion is detected when BATDEP is less than 1.2 V. A no-battery condition is detected when the battery voltage is < 80% of the depleted threshold. In a no-battery condition, the bq24700 automatically selects ac as the input source. If ENABLE = 1, the PWM remains enabled.

$\overline{\text{BATDRV}}$: Battery power source select output. This pin drives an external P-channel MOSFET used to switch the battery as the system's power source. When the voltage level on the ACDET pin is less than 1.2 V, the output of the $\overline{\text{BATDRV}}$ pin is driven low, GND. This pin is driven high (V_{CC}) when ACSEL is high and ACDET > 1.2 V.

BATP: Battery charge regulation voltage measurement input to the battery-voltage g_m amplifier. The voltage on this pin is typically derived from a voltage divider network connected across the battery. In a voltage loop, BATP is regulated to the 1.25 V, ±0.5% precision reference of the battery voltage g_m amplifier.

BATSET: An external override to an internal precision 0.5% reference. When BATSET is > 0.25 V, the voltage level on the BATSET pin sets the voltage charge level. When BATSET ≤ 0.25 V, an internal 1.25-V, ±0.5% reference is connected to the inverting input of the battery error amplifier. To ensure proper battery voltage regulation with BATSET, BATSET must be > 1.0 V. Simply ground BATSET to use the internal reference.

COMP: The inverting input to the PWM comparator and output of the g_m amplifiers. A type II compensation network between COMP and GND is recommended.

ENABLE: Charge enable. A high on this input pin allows PWM control operation to enable charging while a low on this pin disables and forces the PWM output to a high state. Battery charging is initiated by asserting a logic 1 on the ENABLE pin.

> **NOTE:** The ENABLE pin should be asserted high only after ACDET has been asserted high and V_{REF} has been established. When ac is lost, and the bq24700/bq24701 drives ACPRES low, the host must assert the ENABLE low.

GND: Supply return and ground reference

IBAT: Battery current differential amplifier output. The output of this pin produces a voltage proportional to the battery charge current. This voltage is suitable for driving an ADC input.

$\overline{\text{PWM}}$: Gate drive output pin drives the P-channel MOSFET for PWM control. The PWM control is active when ACPRES, ACSEL, and ENABLE are high. $\overline{\text{PWM}}$ is driven low to V_{HSP} and high to V_{CC}.

SRN, SRP: Differential amplifier inputs for battery current sense. These pins feed back the battery charge current for PWM control. SRN is tied to the battery terminal. Care must be taken to keep SRN and SRP below their absolute maximum rating, especially when the battery is removed. Refer to the application section, under ACDET operation, for further detail outlining the various connection configurations which help keep SRN and SRP within safe operating regions.

SRSET: Battery charge current programmed voltage. The level on this pin sets the battery charge current limit.

VCC: Operational supply voltage.

pin assignments (continued)

VHSP: The VHSP pin is connected to a 10-µF capacitor (close to the pin) to provide a stable voltage source to drive the gates of the external MOSFETs. VHSP is equal to (0.5 × VCC) for VCC ≥ 15 V and 0 V for VCC < 15 V (refer to Figure 12). An 18-V Zener diode should be placed between VCC and VHSP for VCC > 20 V to prevent MOSFET overstress during start-up.

VREF: Bypassed precision voltage 5-V, ±0.6% output. It can be used to set fixed levels on the inverting inputs of any one of the three error amplifiers if desired. The tight tolerance is suitable for charging lithium-ion batteries. A 3.3-µF (or higher) capacitor should be placed close to the pin.

VS: System (Load) voltage input pin. The voltage on this pin indicates the system voltage in order to insure a break before make transition when changing from ac power to battery power. The battery is protected from an over-voltage condition by disabling the P-channel MOSFET connected to the $\overline{\text{BATDRV}}$ pin if the voltage at VS is greater than BATP. This function can be eliminated by grounding the VS pin.

APPLICATION INFORMATION

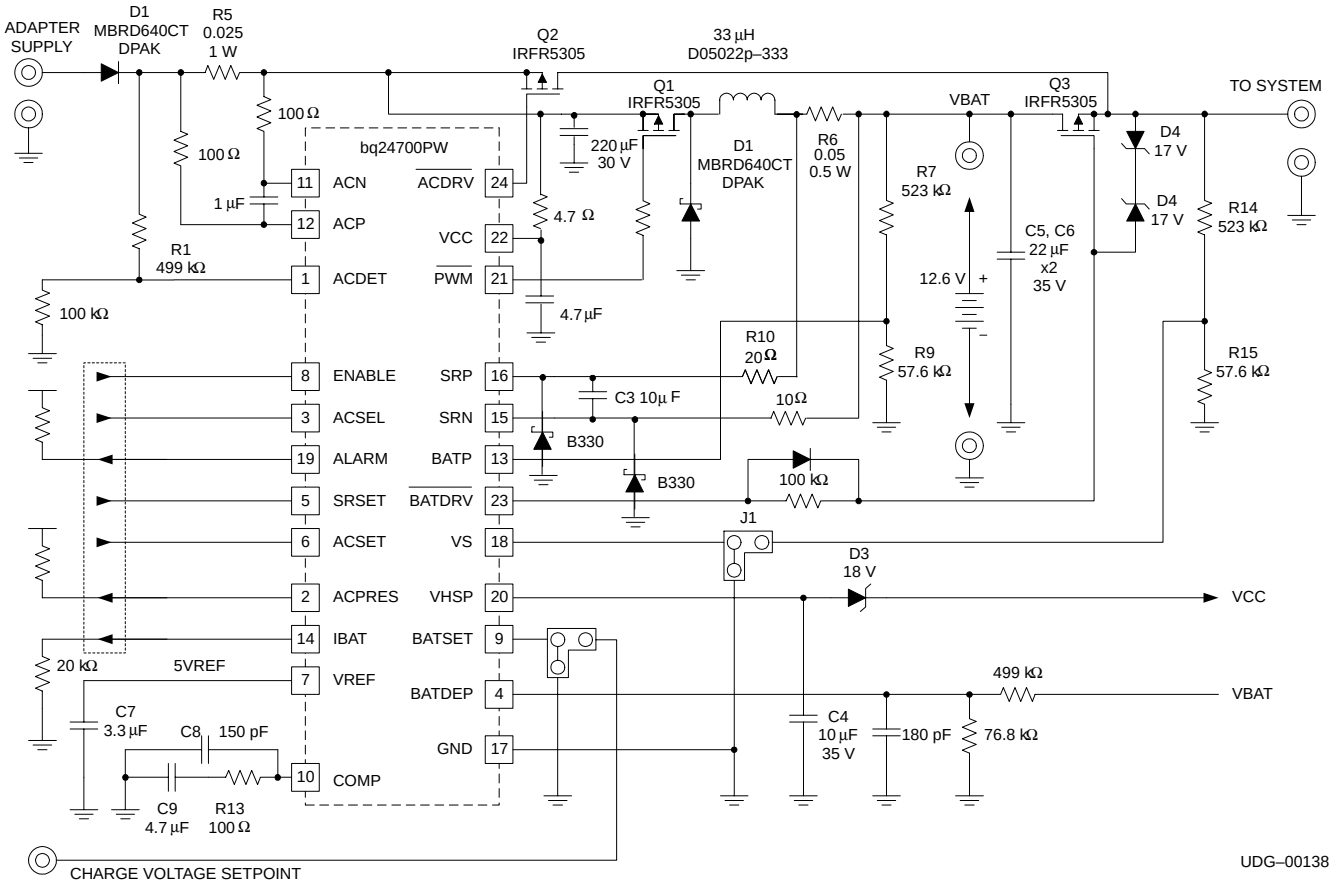


Figure 1. Typical Notebook Charge Management Application

APPLICATION INFORMATION

dynamic power management

The dynamic power management (DPM) feature allows a cost effective choice of an ac wall-adapter that accommodates 90% of the system's operating-current requirements. It minimizes battery charge time by allocating available power to charge the battery (i.e. $I_{BAT} = I_{ADPT} - I_{SYS}$). If the system plus battery charge current exceeds the adapter current limit, as shown in Figure 2, the DPM feature reduces the battery charge current to maintain an overall input current consumption within user defined power capability of the wall-adapter. As the system's current requirements decrease, additional current can be directed to the battery, thereby increasing battery charge current and minimizing battery charge time.

The DPM feature is inherently designed into the PWM controller by inclusion of the three control loops, battery-charge regulation voltage, battery-charge current, and adapter-charge current, refer to Figure 3. If any of the three user programmed limits are reached, the corresponding control loop commands the PWM controller to reduce duty cycle, thereby reducing the battery charge current.

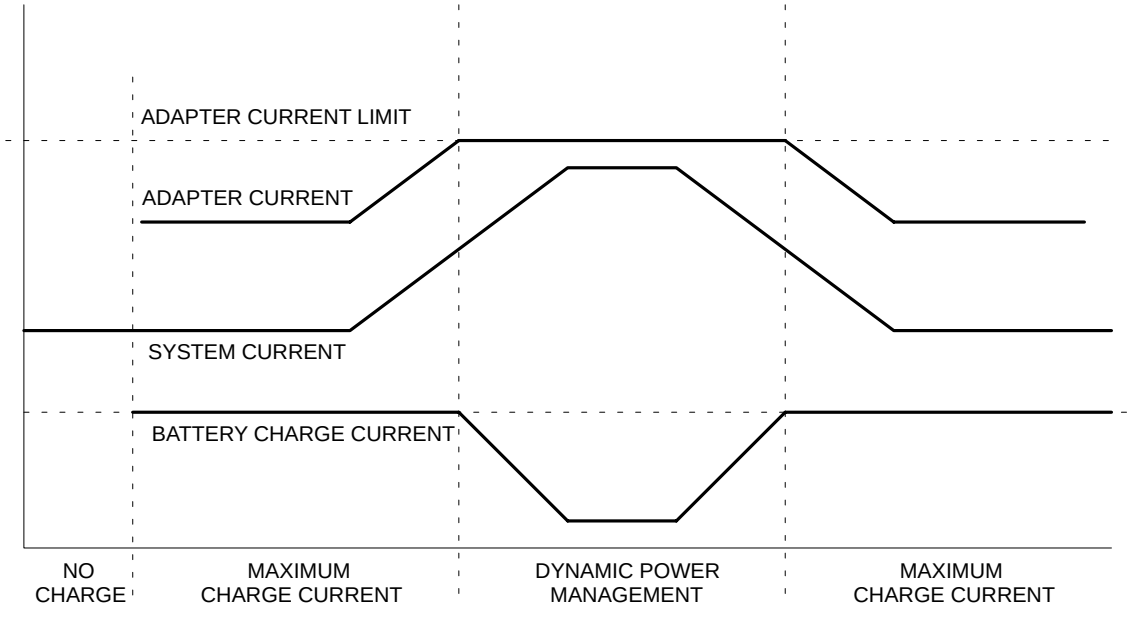


Figure 2. Dynamic Power Management

ACDET operation

The ACDET function senses the loss of adequate adapter power. If the voltage on ACDET drops below the internal 1.2 V reference voltage, a loss of ADAPTER power is declared and the bq24700/bq24701 switches to battery power as the main system power. In addition, the bq24700/bq24701 shuts down its 5-V VREF and enters a low power sleep mode. Under normal operation with a battery present, the low impedance battery node absorbs excess energy stored in the system capacitors (from the higher V_{ADPT} voltage) and quickly bring the system voltage down to the battery voltage level. However, in conditions where the battery has been removed or appears high impedance due to battery protector operation, the residual system energy stored in the load capacitors due to the higher V_{ADPT} level is directly coupled to the SRN and SRP terminals when the battery switch-over occurs. This presents a problem for V_{ADPT} voltages greater than the absolute maximum voltage rating of the SRN and SRP pins.

APPLICATION INFORMATION

ACDET sense point

The ACDET function senses adapter voltage via a resistor divider (refer to the Application Circuit). The location of the ACDET sense node depends on the maximum adapter voltage capability. For operation with V_{ADPT} < 18 V, the ACDET sense node can be at the anode of the input blocking diode. Since the V_{ADPT} voltage does not exceed the absolute maximum rating of the SRN pin, SRN stays within safe operating range. For operation with $V_{ADPT} \geq 18$ V, the ACDET sense node should be at the cathode of the input blocking diode. Moving the ACDET sense point to the cathode of the input diode ensures that the bq24700/bq24701 remains active after adapter power is lost until the load capacitors have discharged to a safe level to protect the SRN and SRP pins. In either case, it is assumed that the ACDET level is set for V_{ADPT} < 17 V.

alternative method

Alternatively, the battery select MOSFET and its associated gate drive protection circuitry could be replaced with a Schottky. The Schottky allows the ACDET sense point to be moved to the anode side of the input diode, for $V_{ADPT} \geq 18$ V, since it blocks the system voltage from the SRN and SRP pins. The bq24700/bq24701 would retain all functionality with fewer components at the expense of lower battery efficiency and a higher drop-out voltage.

battery charger operation

The bq24700/bq24701 fixed-frequency, PWM controller is designed to provide closed-loop control of battery charge-current (I_{CH}) based on three parameters, battery-float voltage (V_{BAT}), battery-charge current, and adapter charge current (I_{ADPT}). The bq24700/bq24701 is designed primarily for control of a buck converter using a high side P-channel MOSFET device (SW, refer to Figure 3).

The three control parameters are voltage programmable through resistor dividers from the bq24700/bq24701 precision 5-V reference, an external or internal precision reference, or directly via a DAC interface from a keyboard controller.

Adapter and battery-charge current information is sensed and fed back to two transconductance (g_m) amplifiers via low-value-sense resistors in series with the adapter and battery respectively. Battery voltage information is sensed through an external resistor divider and fed back from the battery to a third g_m amplifier.

NOTE: The ENABLE pin should be asserted high only after ACDET has been asserted high and V_{REF} has been established. When ac is lost, and the bq24700/bq24701 drives ACPRES low, the host must assert the ENABLE low.

APPLICATION INFORMATION

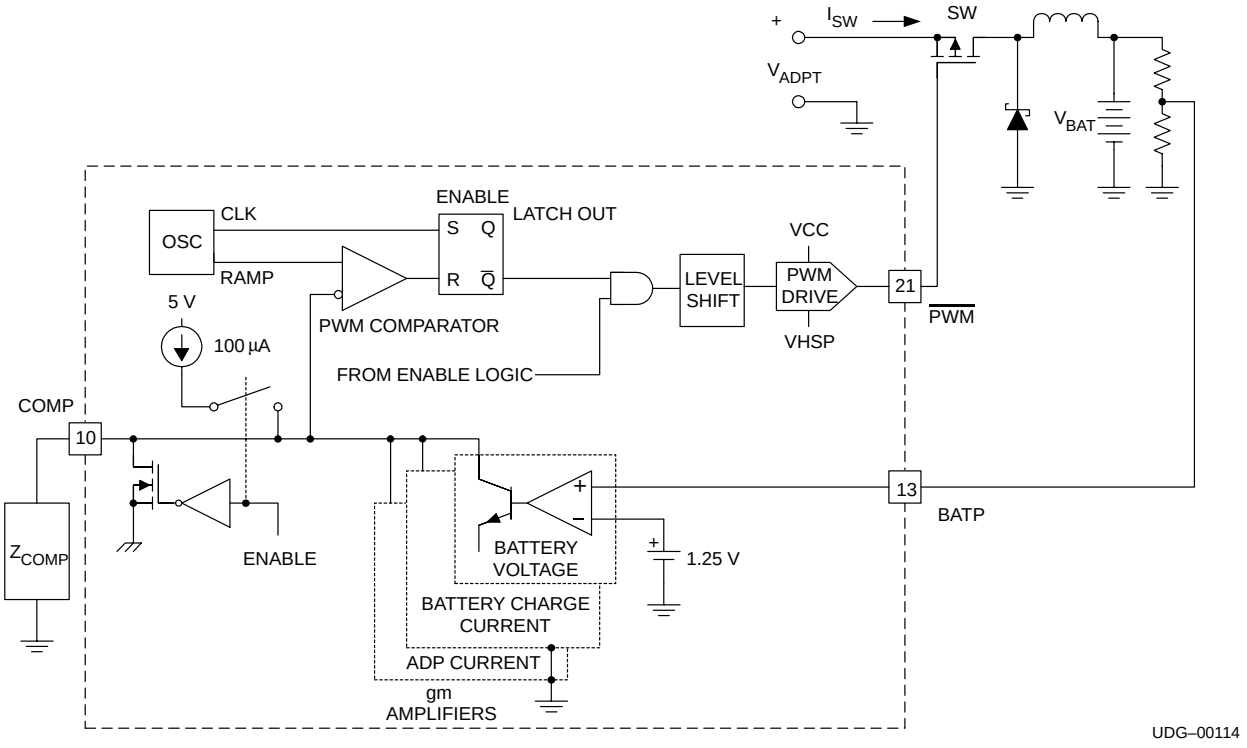


Figure 3. PWM Controller Block Diagram

PWM operation

The three open collector g_m amplifiers are tied to the COMP pin (refer to Figure 3), which is internally biased up by a 100-µA constant current source. The voltage on the COMP pin is the control voltage (V_C) for the PWM comparator. The PWM comparator compares V_C to the sawtooth ramp of the internally fixed 300-kHz oscillator to provide duty cycle information for the PWM drive. The PWM drive is level-shifted to provide adequate gate voltage levels for the external P-channel MOSFET. Refer to *PWM selector switch gate drive* section for gate drive voltage levels.

softstart

Softstart is provided to ensure an orderly start-up when the PWM is enabled. When the PWM controller is disabled (ENABLE = Low), the 100-µA current source pullup is disabled and the COMP pin is actively pulled down to GND. Disabling the 100-µA pullup reduces current drain when the PWM is disabled. When the bq24700/bq24701 $\overline{\text{PWM}}$ is enabled (ENABLE = High), the COMP pin is released and the 100-µA pullup is enabled (refer to Figure 3). The voltage on the COMP pin increases as the pullup charges the external compensation network connected to the COMP pin. As the voltage on the COMP pin increases the PWM duty cycle increases linearly as shown in Figure 4.

> **NOTE:** The ENABLE pin should be asserted high only after ACDET has been asserted high and V_{REF} has been established. When ac is lost, and the bq24700/bq24701 drives ACPRES low, the host must assert the ENABLE low.

APPLICATION INFORMATION

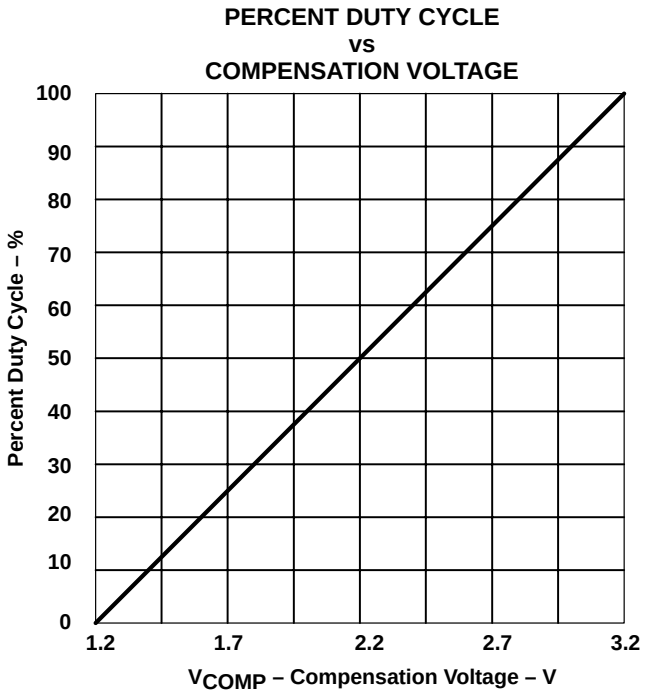


Figure 4

As any one of the three controlling loops approaches the programmed limit, the g_m amplifier begins to shunt current away from the COMP pin. The rate of voltage rise on the COMP pin slows due to the decrease in total current out of the pin, decreasing the rate of duty cycle increase. When the loop has reached the programmed limit the g_m amplifier shunts the entire bias current (100 μA) and the duty cycle remains fixed. If any of the control parameters tries to exceed the programmed limit, the g_m amplifier shunts additional current from the COMP pin, further reducing the PWM duty cycle until the offending parameter is brought into check.

APPLICATION INFORMATION

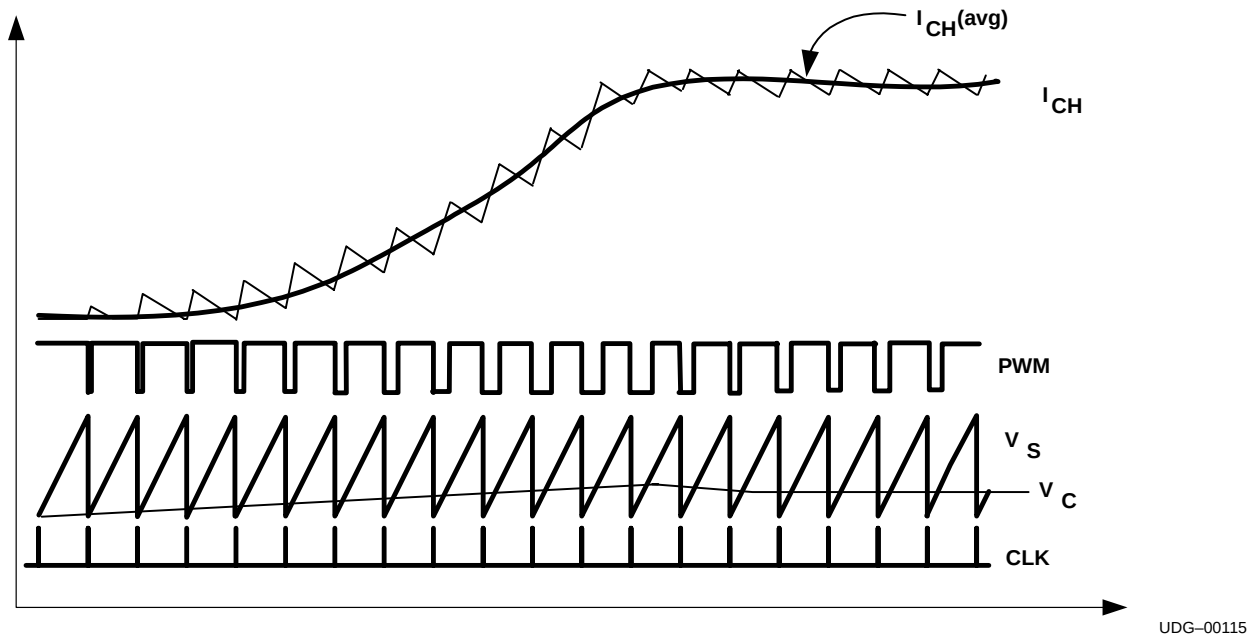


Figure 5. Typical PWM Waveforms in a Buck Converter (Including Startup)

setting the battery charge regulation voltage

The battery charge regulation voltage is programmed through the BATSET pin, if the internal 1.25-V precision reference is not used. The BATSET input is a high-impedance input that is driven by either a keyboard controller DAC or via a resistor divider from a precision reference (see Figure 6).

The battery voltage is fed back to the g_m amplifier through a resistor divider network. The battery charge regulation voltage can be defined as:

$$V_{BATTERY} = \frac{(R1 + R2) \times V_{BATSET}}{R2} \ V \quad (1)$$

The overall accuracy of the battery charge regulation voltage is a function of the bypassed 5-V reference voltage tolerance as well as the tolerances on R1 and R2. The precision voltage reference has a 0.5% tolerance making it suitable for the tight battery voltage requirements of Li-ion batteries. Tolerance resistors of 0.1% are recommended for R1 and R2 as well as any resistors used to set BATSET.

The bq24700/bq24701 provides the capability of using an internal precision voltage reference (1.25 Vdc) through the use of a multiplexing scheme, refer to Figure 6, on the BATSET pin. When BATSET voltage is less than 0.25 V, an internal 1.25-V, 0.5% reference is switched in and the BATSET pin is switched out from the g_m amplifier input. When the BATSET voltage is greater than 0.25 V, the BATSET pin voltage is switched in to the input of the g_m amplifier and the 1.25 V voltage reference is switched out.

NOTE: The minumum recommended BATSET is 1.0 V, if BATSET is used to set the voltage loop.

APPLICATION INFORMATION

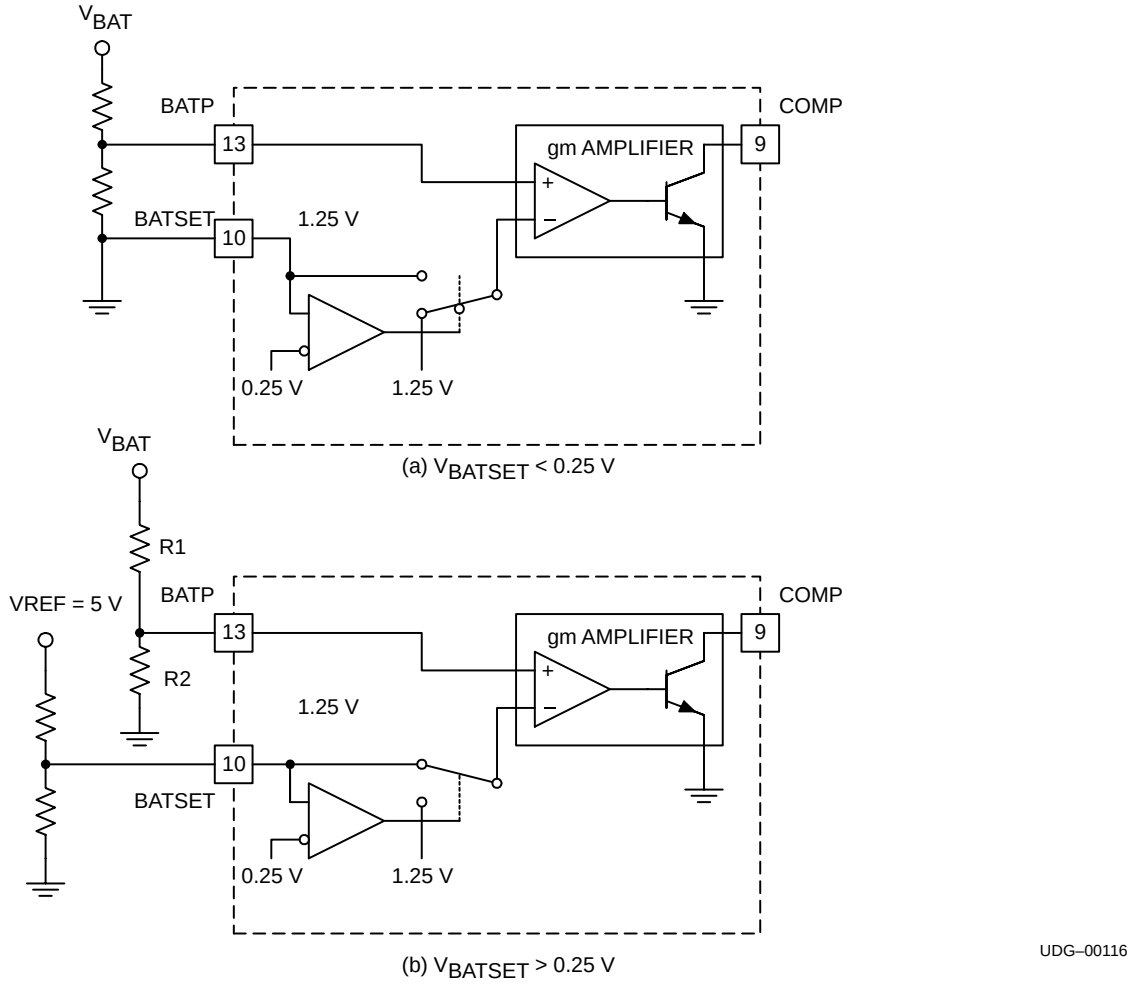


Figure 6. Battery Error Amplifier Input Multiplexing Scheme

programming the battery charge current

The battery charge current is programmed via a voltage on the SRSET pin. This voltage can be derived from a resistor divider from the 5-V VREF or by means of an DAC. The voltage is converted to a current source that is used to develop a voltage drop across an internal offset resistor at one input of the SR g_m amplifier. The charge current is then a function of this voltage drop and the sense resistor (R_S), refer to Figure 7.

APPLICATION INFORMATION

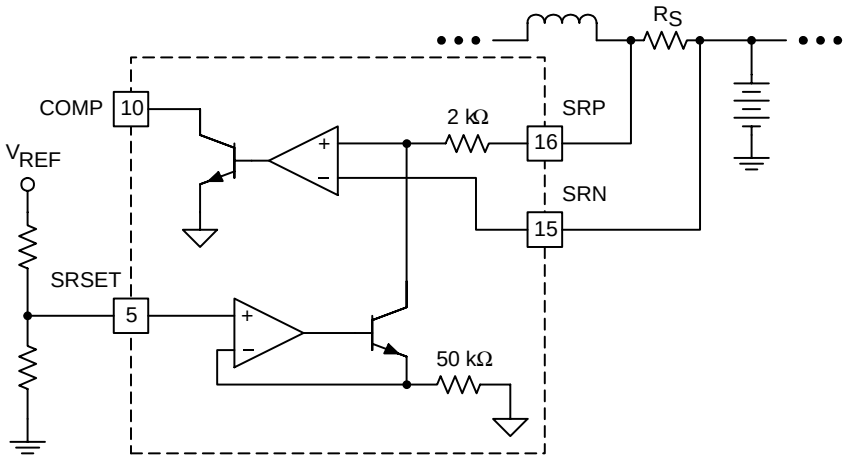


Figure 7. Battery Charge Current Input Threshold Function

The battery charge current can be defined as:

$$I_{BAT} = \frac{V_{SRSET}}{25 \times R_S} \quad (2)$$

where V_{SRSET} is the programming voltage on the SRSET pin. V_{SRSET} maximum is 2.5 V.

programming the adapter current

Like the battery charge current described previously, the adapter current is programmed via a voltage on the ACSET pin. That voltage can either be from an external resistor divider from the 5-V VREF or from an external DAC. The adapter current is defined as:

$$I_{ADPT} = \frac{V_{ACSET}}{25 \times R_{S2}} \quad (3)$$

component selection

MOSFET selection

MOSFET selection depends on several factors, namely, gate-source voltage, input voltage and input current. The MOSFET must be a P-channel device capable of handling at least 20-V gate-to-source with a drain-source breakdown of VBV~ VIN+1V. The average input current can be approximated by:

$$I_{IN}(avg) \cong \frac{\left(V_O \times I_O\right) \times 1.2}{V_{IN}} \text{ A} \quad (4)$$

APPLICATION INFORMATION

The RMS current through the MOSFET is defined as:

$$I_{IN}(RMS) = I_{IN}(avg) \times \sqrt{\frac{1}{D}} \ A_{RMS} \quad (5)$$

Schottky rectifier (freewheeling)

The freewheeling Schottky rectifier must also be selected to withstand the input voltage, V_{IN}. The average current can be approximated from:

$$I_{D1}(avg) = I_O \times (1 - D) \ A \quad (6)$$

choosing an inductance

Low inductance values result in a steep current ramp or slope. Steeper current slopes result in the converter operating in the discontinuous mode at a higher power level. Steeper current slopes also result in higher output ripple current, which may require a higher number, or more expensive capacitors to filter the higher ripple current.

In addition, the higher ripple current results in an error in the sensed battery current particularly at lower charging currents. It is recommended that the ripple current not exceed 20% to 30% of full scale dc current.

$$L = \frac{\left(V_{IN} - V_{BAT}\right) \times V_{BAT}}{fs \times 0.2 \times I_{FS} \times V_{IN}} \quad (7)$$

Too large an inductor value results in the current waveform of Q1 and D1 in Figure 8 approximating a squarewave with an almost flat current slope on the step. In this case, the inductor is usually much larger than necessary, which may result in an efficiency loss (higher DCR) and an area penalty.

selecting an output capacitor

For this application the output capacitor is used primarily to shunt the output ripple current away from the battery. The output capacitor should be sized to handle the full output ripple current as defined as:

$$I_C(RMS) = \frac{\left(V_{IN} - V_{BAT}\right) \times D}{fs \times L \times \sqrt{12}} \quad (8)$$

selecting an input capacitor

The input capacitor is used to shunt the converter ripple current on the input lines. The capacitor(s) must have a ripple curent (RMS) rating of:

$$I_{RMS} = I_{IN(avg)} \times \frac{V_{IN}}{V_O} \sqrt{\frac{V_{IN}}{V_O}\left(1 - \frac{V_{IN}}{V_O}\right)} \ A_{RMS} \quad (9)$$

APPLICATION INFORMATION

compensating the loop

For the bq24700/bq24701 used as a buck converter, the best method of compensation is to use a Type II compensation network from the output of the transconductance amplifiers (COMP pin) to ground (GND) as shown in Figure 8. A Type II compensation adds a pole-zero pair and an addition pole at dc.

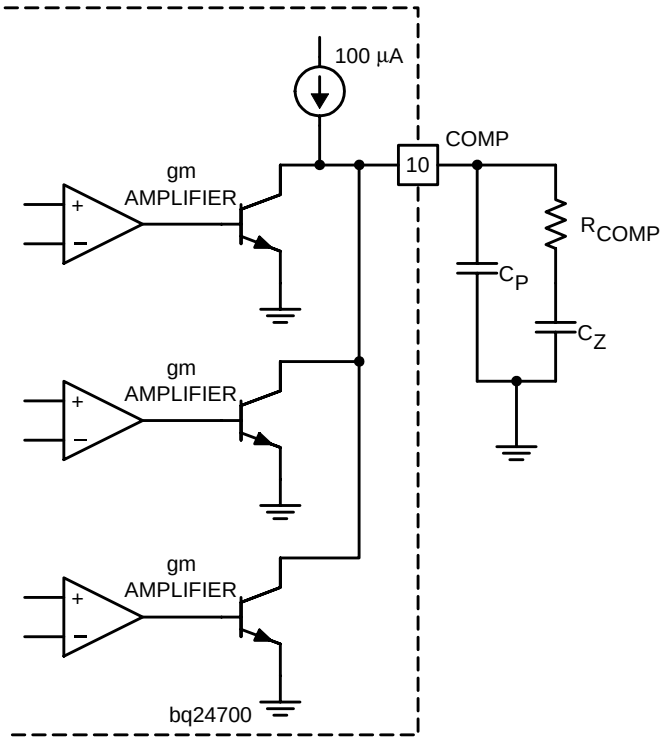


Figure 8. Type II Compensation Network

The Type II compensation network places a zero at

$$F_Z = \frac{1}{2} \times \pi \times R_{COMP} \times C_Z \text{ Hz} \quad (10)$$

and a pole at

$$F_P = \frac{1}{2} \times \pi \times R_{COMP} \times C_P \text{ Hz} \quad (11)$$

For this battery charger application the following component values: C_Z = 4.7 µF, C_P = 150 pF, and R_{COMP} = 100Ω, provides a closed loop response with more than sufficient phase margin.

APPLICATION INFORMATION

selector operation

The bq24700/bq24701 allows the host controller to manually select the battery as the system's main power source, without having to remove adapter power. This allows battery conditioning through smart battery learn cycles. In addition, the bq24700/bq24701 supports autonomous supply selection during fault conditions on either supply. The selector function uses low $R_{DS(on)}$ P-channel MOSFETs for reduced voltage drops and longer battery run times. *Note: Selection of battery power whether manual or automatic results in the suspension of battery charging.*

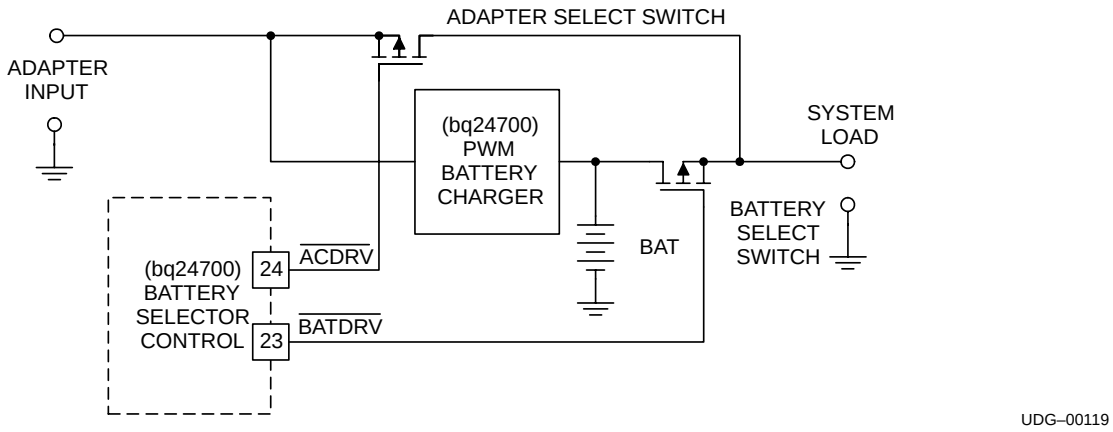


Figure 9. Selector Control Switches

autonomous selection operation

Adapter voltage information is sensed at the ACDET pin via a resistor divider from the adapter input (refer to ACDET operation section). The voltage on the ACDET pin is compared to an internally fixed threshold. An ACDET voltage less than the set threshold is considered as a loss of adapter power regardless of the actual voltage at the adapter input. Information concerning the status of adapter power is fed back to the host controller through ACPRES. The presence of adapter power is indicated by ACPRES being set high. A loss of adapter power is indicated by ACPRES going low regardless of which power source is powering the system. During a loss of adapter power, the bq24700/bq24701 obtains operating power from the battery through the body diode of the P-channel battery select MOSFET. Under a loss of adapter power, ACPRES (normally high) goes low, if adapter power is selected to power the system, the bq24700/bq24701 automatically switches over to battery power by commanding $\overline{\text{ACDRV}}$ high and $\overline{\text{BATDRV}}$ low and ALARM goes high. During the switch transition period, battery power is supplied to the load via the body diode of the battery select P-channel MOSFET. When adapter power is restored, the bq24700/bq24701 configures the selector switches according to the state of signals; ACSEL, and ACPRES. If the ACSEL pin is left high when ac power is restored, the bq24700/bq24701 automatically switches back to ac power and the ALARM pin goes low. To remain on battery power after ac power is restored, the ACSEL pin must be brought low.

Conversely**,** if the battery is removed while the system is running on battery power and adapter power is present, the bq24700/bq24701 automatically switches over to adapter power by commanding $\overline{\text{BATDRV}}$ high and $\overline{\text{ACDRV}}$ low. *Note: For the bq24700 any fault condition that results in the selector MOSFET switches not matching their programmed states is indicated by the ALARM pin going high. Please refer to Battery Depletion Detection Section for more information on the ALARM discrete.*

APPLICATION INFORMATION

smart learn cycles when adapter power is present

Smart learn cycles can be conducted when adapter power is present by asserting and maintaining the ACSEL pin low. The adapter power can be reselected at the end of the learn cycle by a setting ACSEL to a logic high, provided that adapter power is present. Battery charging is suspended while selected as the system power source.

When selecting the battery as the system primary power source, the adapter power select MOSFET turns off, in a *break-before-make* fashion, before the battery select MOSFET turns on. To ensure that this happens under all load conditions, the system voltage (load voltage) can be monitored through a resistor divider on the VS pin. This function provides protection against switching over to battery power if the adapter selector switch were shorted and adapter power present. This function can be eliminated by grounding the VS pin. During the transition period from battery to adapter or adapter to battery, power is supplied to the system through the body diode of the battery select switch.

battery depletion detection

The bq24700/bq24701 provides the host controller with a battery depletion discrete, the ALARM pin, to alert the host when a depleted battery condition occurs. The battery depletion level is set by the voltage applied to the BATDEP pin through a voltage divider network. The ALARM output asserts high and remains high as long as the battery deplete condition exists regardless of the power source selected.

For the bq24700, the host controller must take appropriate action during a battery deplete condition to select the proper power source. The bq24700 remains on the selected power source. The bq24700, however, automatically reverts over to adapter power, provided the adapter is present, during a deep discharge state. The battery is considered as being in a deep discharge state when the battery voltage is less than (0.8 × depleted level).

The bq24701 automatically switches back to adapter power if a battery deplete condition exists, provided that the adapter is present. Feature sets for the bq24700 and bq24701 are detailed in Table 1.

Table 1. Available Options

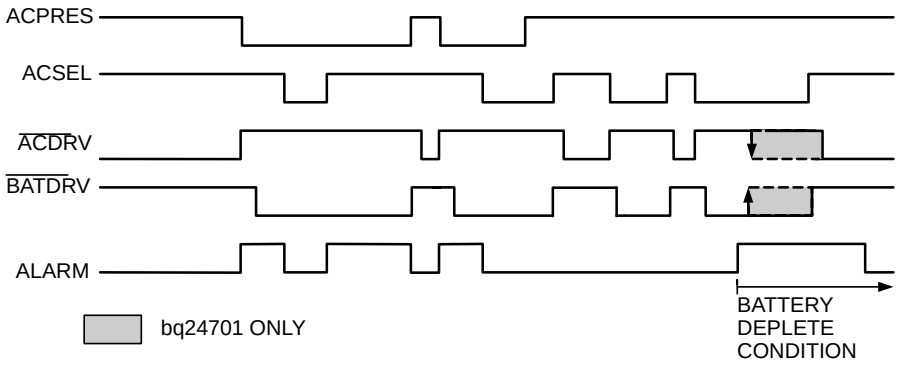
Condition –40 C T_A 85 C	Selector Operation	
	bq24700PW	**bq24701PW**
Battery as Power Source		
Battery removal	Automatically selects ac	Automatically selects ac
Battery reinserted	Selection based on selector inputs	Battery is selected when ac is removed
ac as Power Source		
AC removal	Automatically selects battery	Automatically selects battery
AC reinserted	Selection based on selector inputs	Selection based on selector inputs
Depleted Battery Condition		
Battery as power source	Sends ALARM signal	**Automatically selects ac** Sends ALARM signal
AC as power source	Sends ALARM signal	Sends ALARM signal
ALARM Signal Active		
	Depleted battery condition	Depleted battery condition
	Selector inputs do not match selector outputs	

APPLICATION INFORMATION

selector/ALARM timing example

The selector and ALARM timing example in Figure 10 illustrates the battery conditioning support.

NOTE: For manual selection of wall power as the main power source, both the ACPRES and ACSEL signals must be a logic high.



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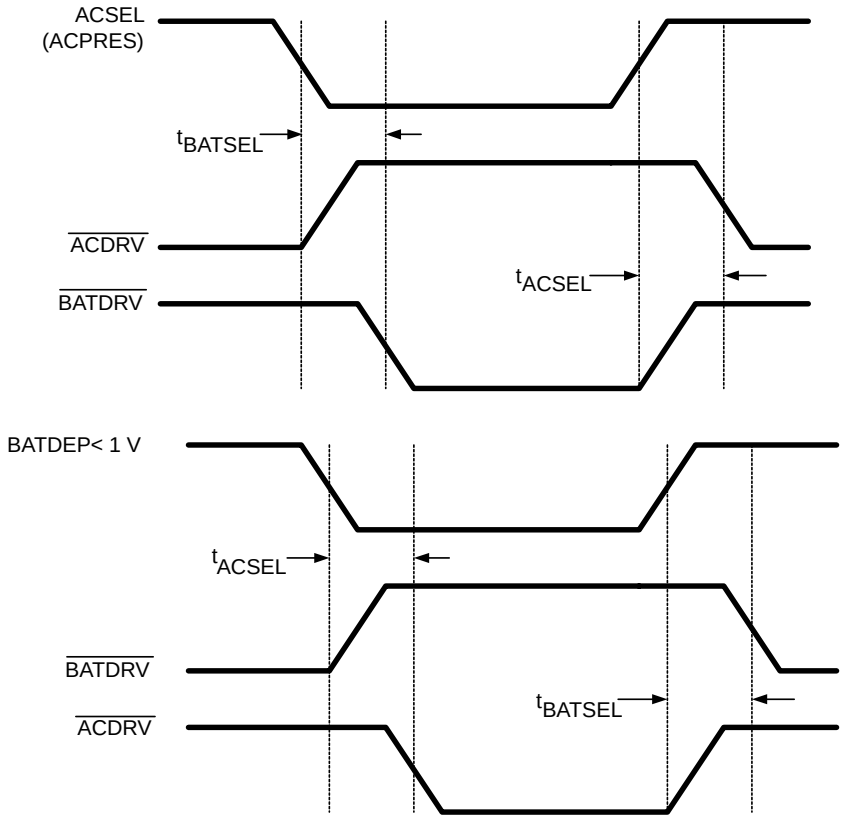


UDG–00120

Figure 10. Battery Selector and ALARM Timing Diagram

APPLICATION INFORMATION

PWM selector switch gate drive

Because the external P-channel MOSFETs (as well as the internal MOSFETs) have a maximum gate-source voltage limitation of 20 V, the input voltage, VCC, cannot be used directly to drive the MOSFET gate under all input conditions. To provide safe MOSFET-gate-drive at input voltages of less than 20 V, an intermediate gate drive voltage rail was established (VSHP). As shown in Figure 11, VSHP has a stepped profile. For VCC voltages of less than 15 V, VSHP = 0 and the full VCC voltage is used to drive the MOSFET gate. At input voltages of greater than 15 V, VSHP steps to approximately one-half the VCC voltage. This ensures adequate enhancement voltage across all operating conditions.

The gate drive voltage, Vgs, vs VCC for the PWM, and ac selector P-channel MOSFETs are shown in Figure 11.

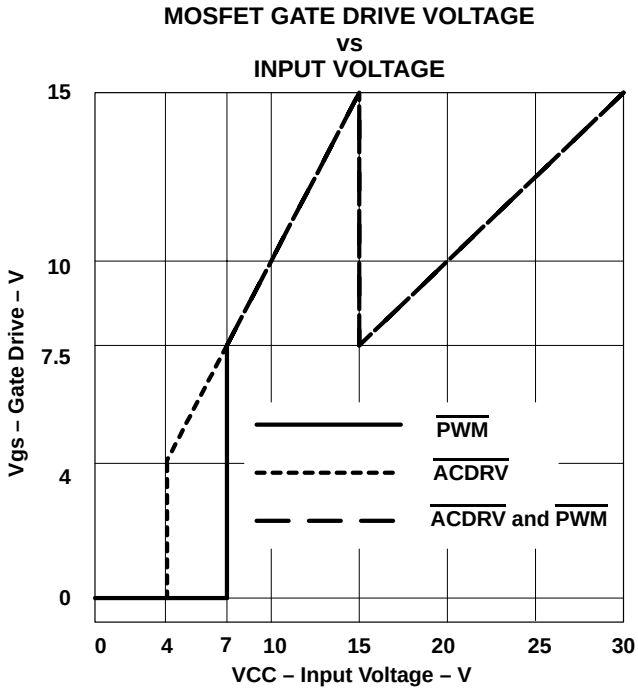


Figure 11

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER REFERENCE vs JUNCTION TEMPERATURE

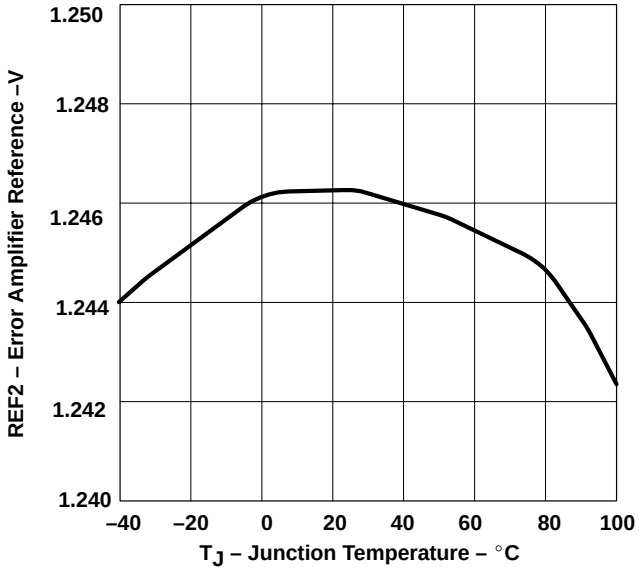


Figure 12

BYPASSED 5-V REFERENCE vs JUNCTION TEMPERATURE

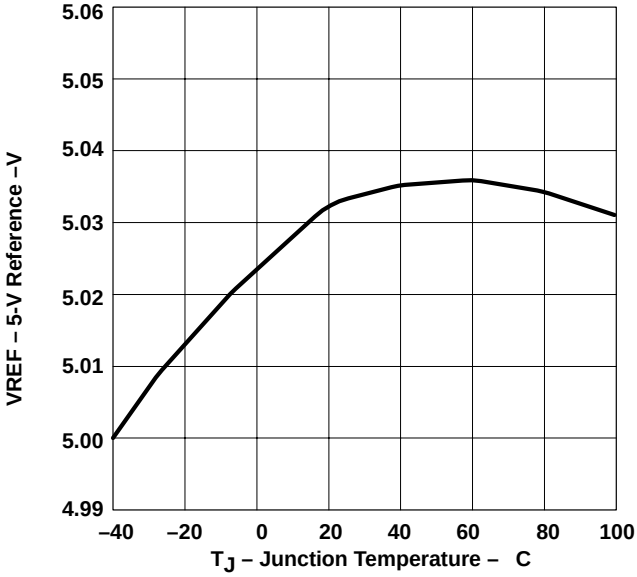


Figure 13

TOTAL SLEEP CURRENT vs JUNCTION TEMPERATURE

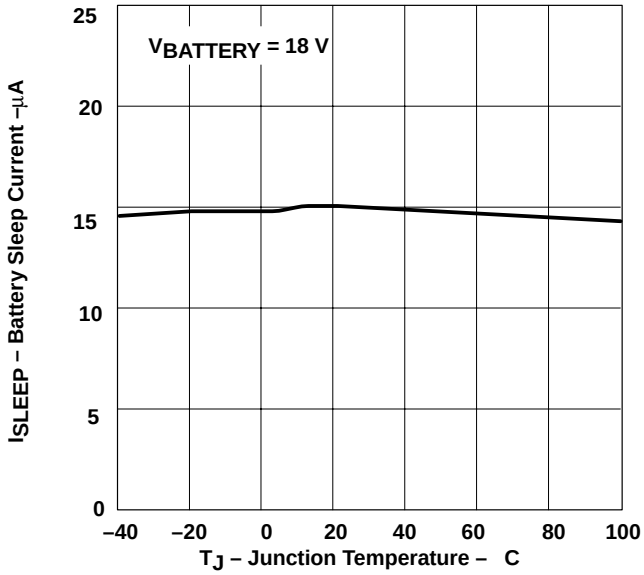


Figure 14

OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

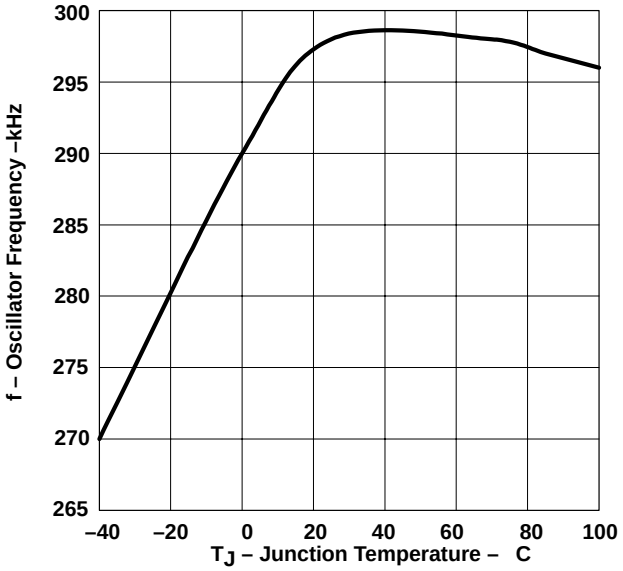


Figure 15

TYPICAL CHARACTERISTICS

BATTERY CURRENT SET ACCURACY vs BATTERY CURRENT SET VOLTAGE

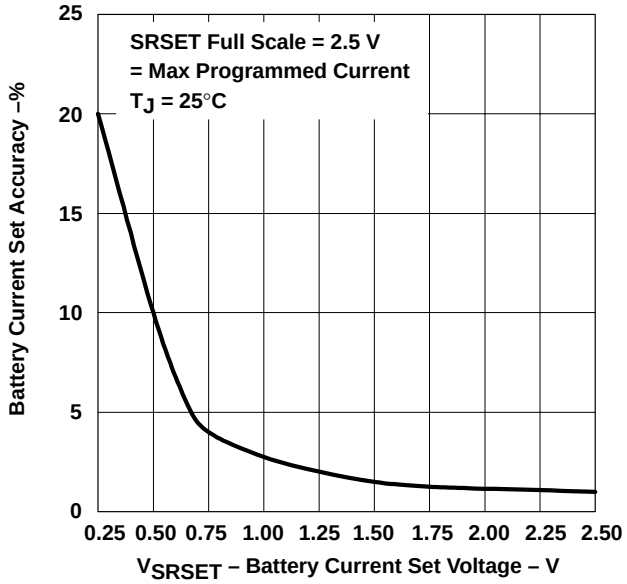


Figure 16

AC CURRENT SET ACCURACY vs AC CURRENT SET VOLTAGE

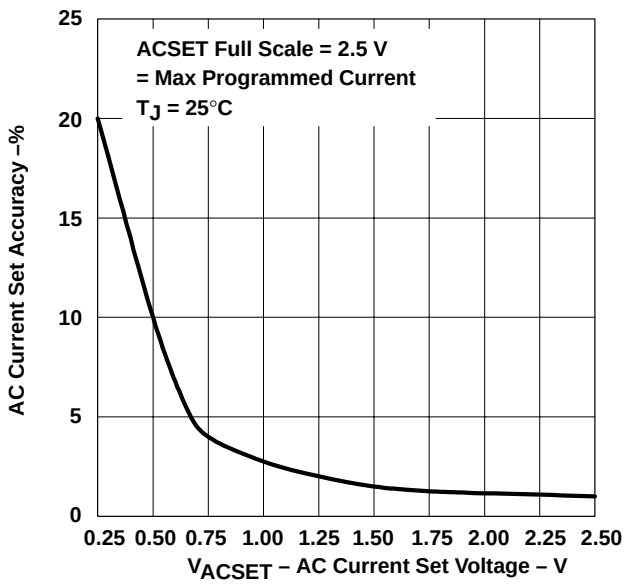


Figure 17

BATTERY I_{BAT} READBACK vs (SRP–SRN) VOLTAGE

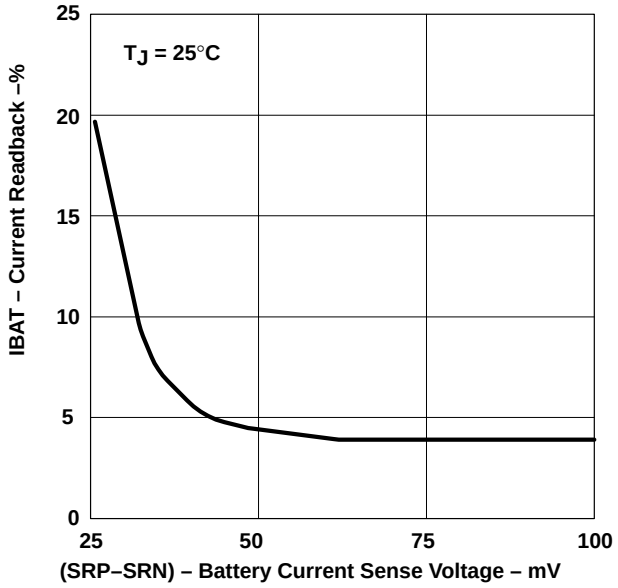


Figure 18

HALF SUPPLY REGULATOR VOLTAGE vs INPUT VOLTAGE

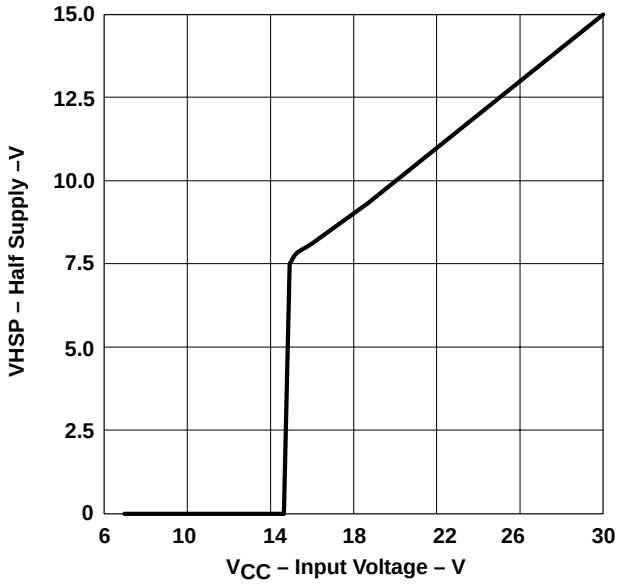


Figure 19

PARAMETER MEASUREMENT INFORMATION

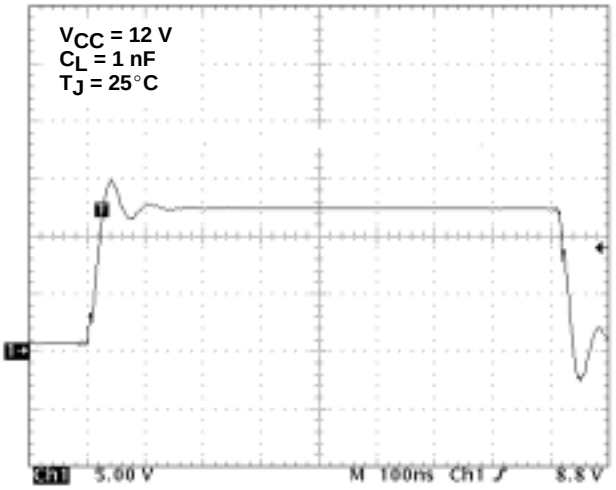


Figure 20. PWMB Rise and Fall Times

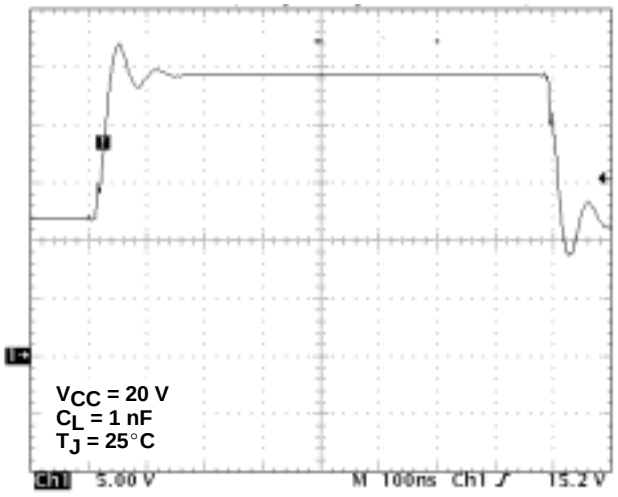


Figure 21. PWMB Rise and Fall Times

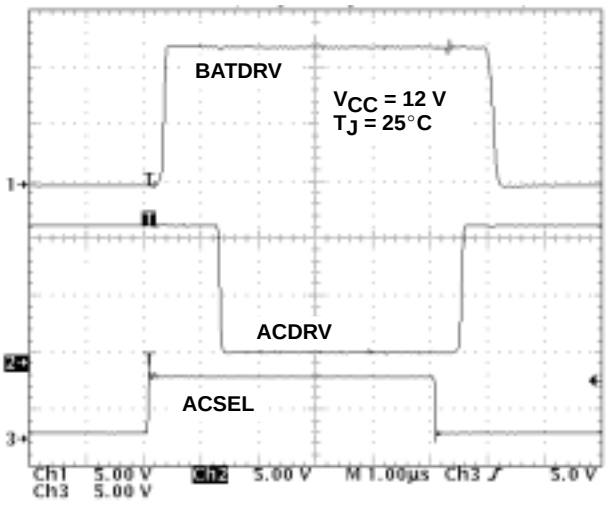


Figure 22. Power Source Select Output Break Before Make

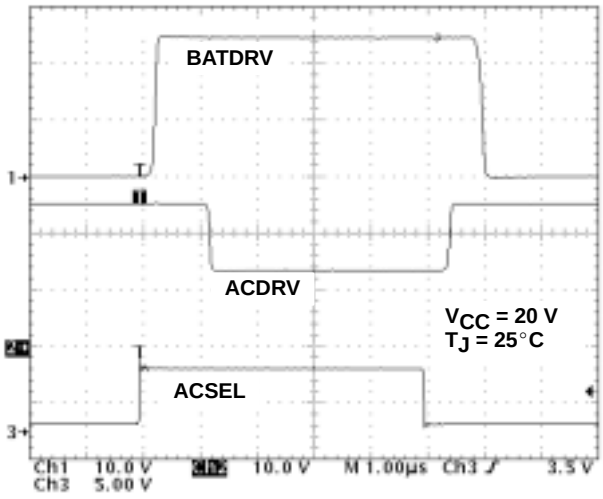


Figure 23. Power Source Select Output Break Before Make

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
BQ24700PW	NRND	TSSOP	PW	24		TBD	Call TI	Call TI
BQ24700PWR	NRND	TSSOP	PW	24		TBD	Call TI	Call TI
BQ24700PWRG4	NRND	TSSOP	PW	24		TBD	Call TI	Call TI
BQ24701PW	NRND	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24701PWG4	NRND	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24701PWR	NRND	TSSOP	PW	24		TBD	Call TI	Call TI
BQ24701PWRG4	NRND	TSSOP	PW	24		TBD	Call TI	Call TI

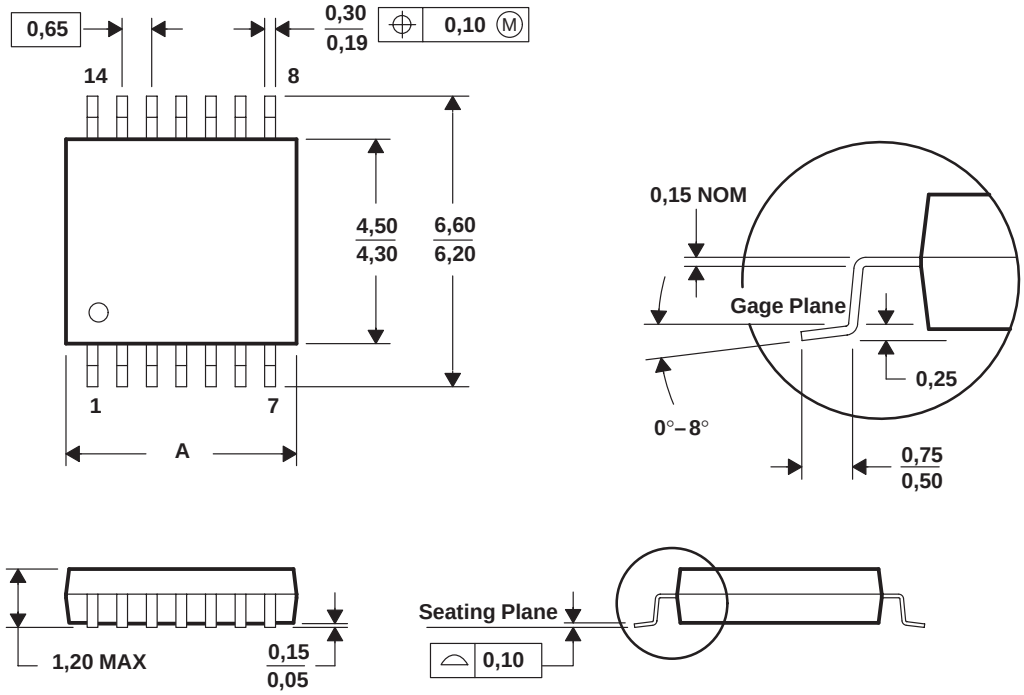
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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