Freescale Semiconductor
Data Sheet: Technical Data

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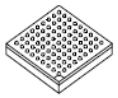
MPC8569E

MPC8569E PowerQUICC III Integrated Processor Hardware Specifications



- High-performance, 32-bit e500 core, scaling up to 1.33 GHz, that implements the Power Architecture® technology
  - 2799 MIPS at 1.33 GHz (estimated Dhrystone 2.1)
  - 36-bit physical addressing
  - Double-precision embedded floating point APU using 64-bit operands
  - Embedded vector and scalar single-precision floating-point APUs using 32- or 64-bit operands
  - Memory management unit (MMU)
- Integrated L1/L2 cache
  - L1 cache—32-Kbyte data and 32-Kbyte instruction
  - L2 cache—512-Kbyte (8-way set associative)
- Two DDR2/DDR3 SDRAM memory controllers with full ECC support
  - One 64-bit or two 32-bit data bus configuration
  - Up to 400 MHz clock (800 MHz data rate)
  - Supporting up to 16 Gbytes of main memory
  - Using ECC, detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble
  - Invoke a level of system power management by asserting MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode
  - Both hardware and software options to support battery-backed main memory
  - Initialization bypass feature that allow system designers to prevent re-initialization of main memory during system power on following abnormal shutdown
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPsec, IKE, SSL/TLS, iSCSI, SRTP, IEEE Std 802.11i™, IEEE Std 802.16™ (WiMAX), IEEE 802.1ae™ (MACSec), 3GPP, A5/3 for GSM and EDGE, and GEA3 for GPRS.
  - XOR engine for parity checking in RAID storage applications
  - Four crypto-channels, each supporting multi-command descriptor chains
  - Cryptographic execution units for PKEU, DEU, AESU, AFEU, MDEU, KEU, CRCU, RNG and SEU- SNOW
- QUICC Engine technology
  - Four 32-bit RISC cores
  - Supports Ethernet, ATM, POS, and T1/E1 along with associated interworking
    - Four Gigabit Ethernet interfaces (up to two with SGMII)
    - Up to eight 10/100-Mbps Ethernet interfaces
    - Up to 16 T1/E1 TDM links (512 × 64 channels)
    - Multi-PHY UTOPIA/POS-PHY L2 interface (16-bit)
  - IEEE Std 1588™ v2 support
  - SPI and Ethernet PHY management interface
  - One full-/low-speed USB interface supporting USB 2.0
  - General-purpose I/O signals
- High-speed interfaces (multiplexed) supporting:
  - Two 1× Serial RapidIO interfaces (with message unit) or one 4x interface
  - ×4/×2/×1 PCI Express interface
  - Two SGMII interfaces
- On-chip network switch fabric
- 133 MHz, 16-bit, 3.3 V I/O, enhanced local bus (eLBC) with memory controller
- Enhanced secured digital host controller (eSDHC) used for SD/MMC card interface
- Integrated four-channel DMA controller
- Dual I^2C and dual universal asynchronous receiver/transmitter (DUART) support
- Programmable interrupt controller (PIC)
- IEEE Std 1149.1™ JTAG test access port
- 1.0-V and 1.1-V core voltages with 3.3-V, 2.5-V, 1.8-V, 1.5-V and 1.0-V I/O
- 783-pin FC-PBGA package, 29 mm × 29 mm

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NOTE

The MPC8569E is also available without a security engine in a configuration known as the MPC8569. All specifications other than those relating to security apply to the MPC8569 exactly as described in this document.

The following figure shows the major functional units within the MPC8569E.

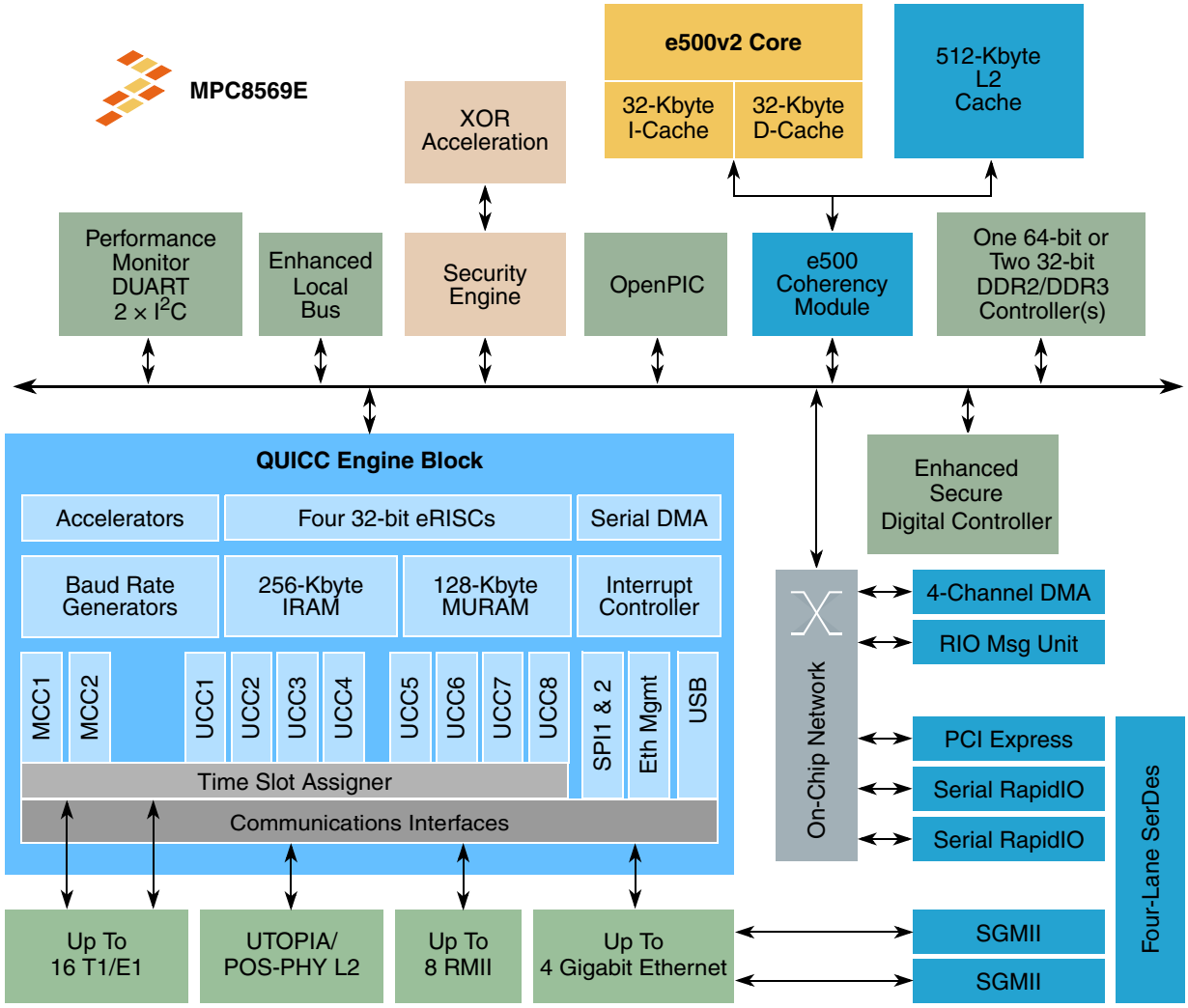


Figure 1. MPC8569E Block Diagram

1 Pin Assignments and Reset States

1.1 Ball Layout Diagrams

The following figure shows the top view of the MPC8569E 783-pin BGA ball map diagram.

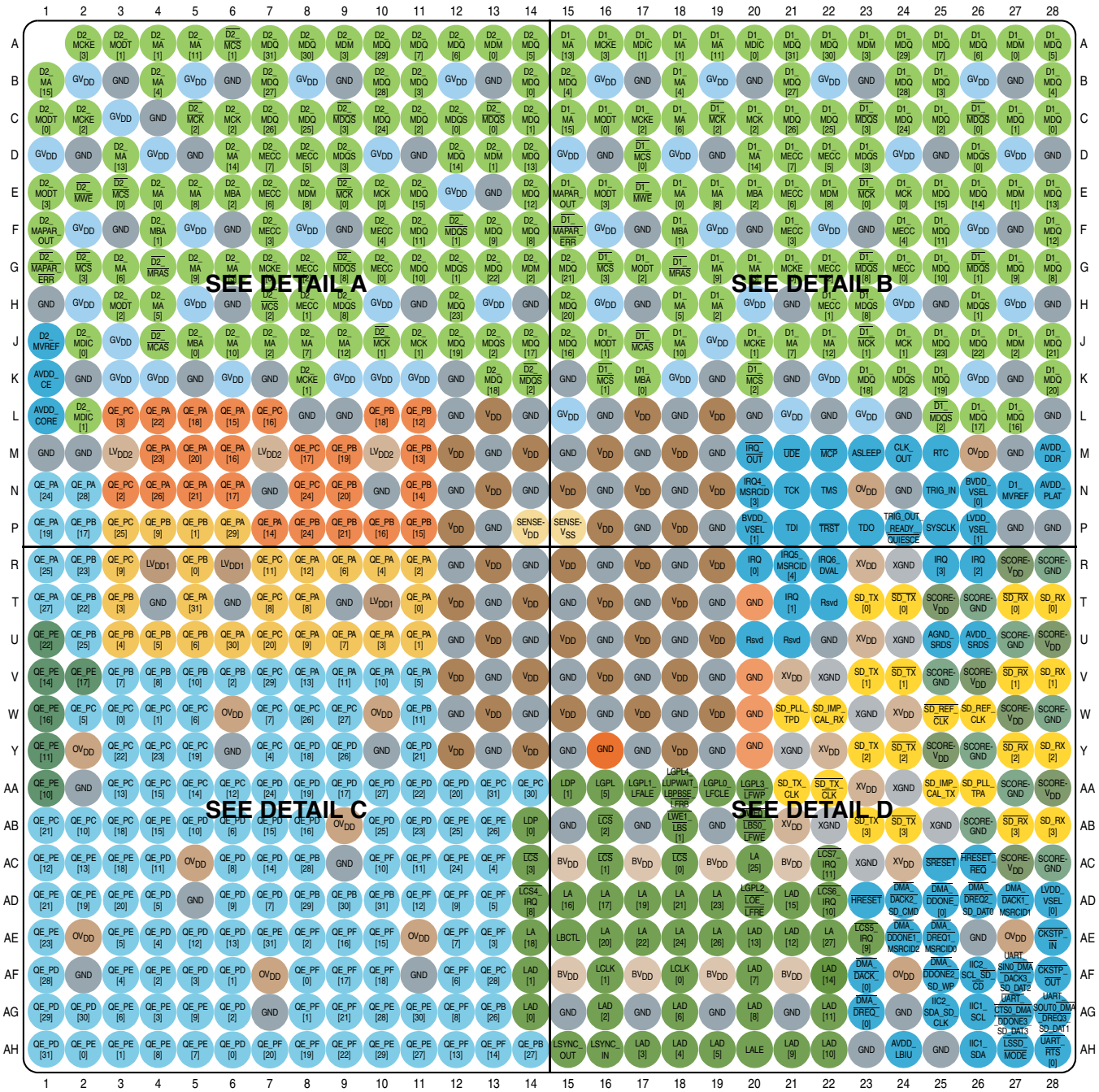
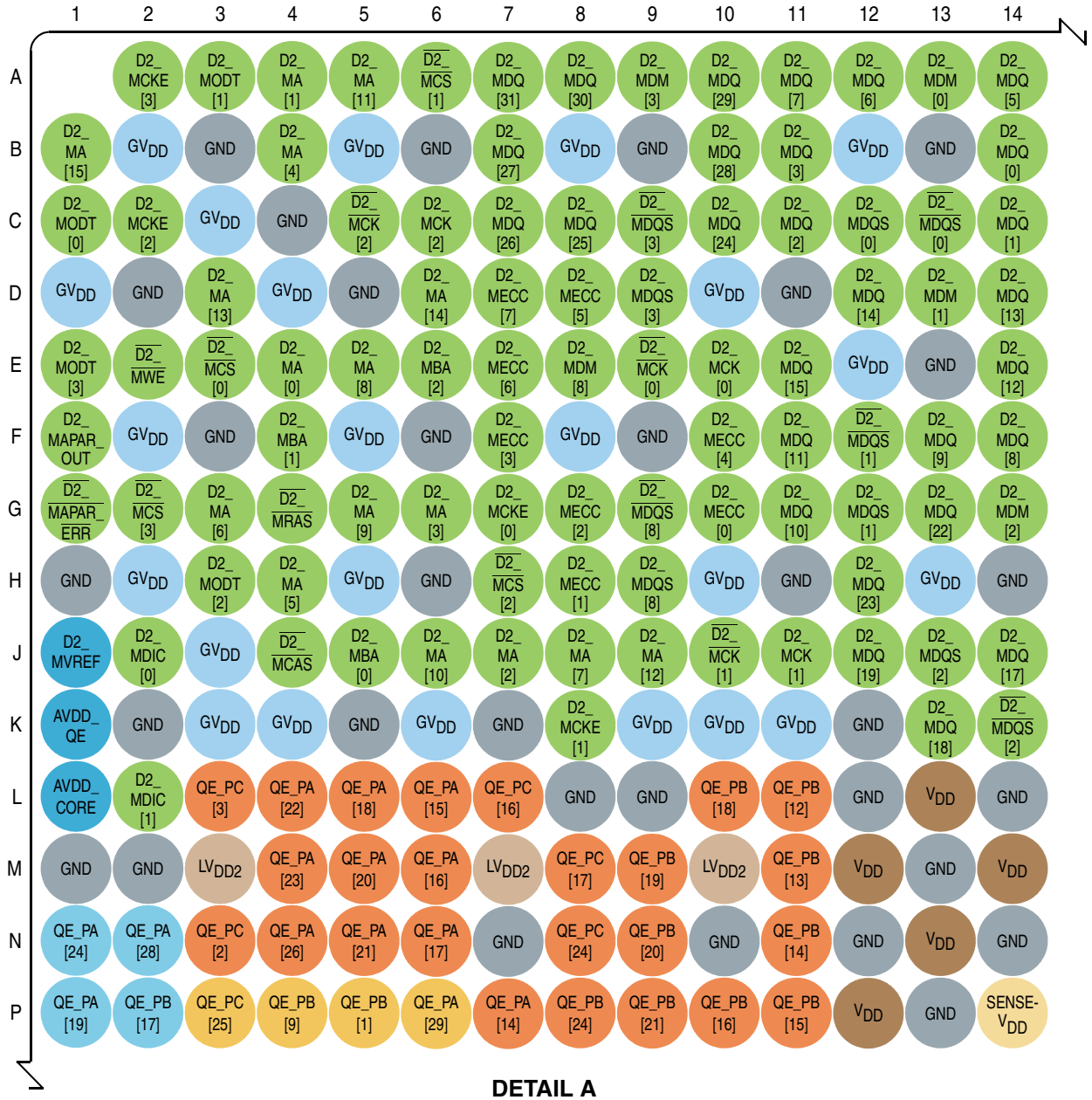


Figure 2. MPC8569E Top View Ballmap

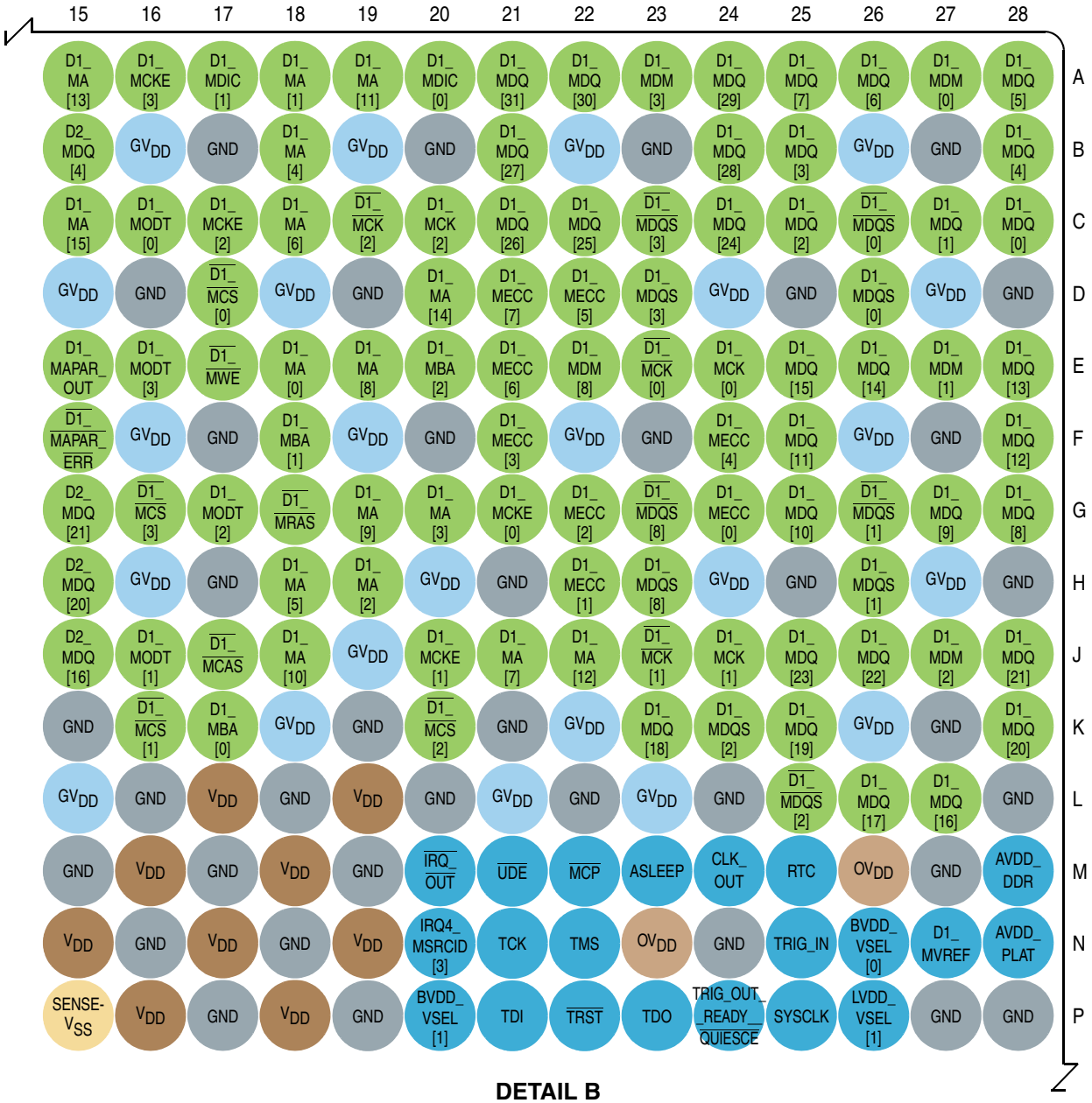
The following figure provides detailed view A of the MPC8569E 783-pin BGA ball map diagram.



DETAIL A

Figure 3. MPC8569E Detail A Ball Map

The following figure provides detailed view B of the MPC8569E 783-pin BGA ball map diagram.



DETAIL B

Figure 4. MPC8569E Detail B Ball Map

The following figure provides detailed view C of the MPC8569E 783-pin BGA ball map diagram.

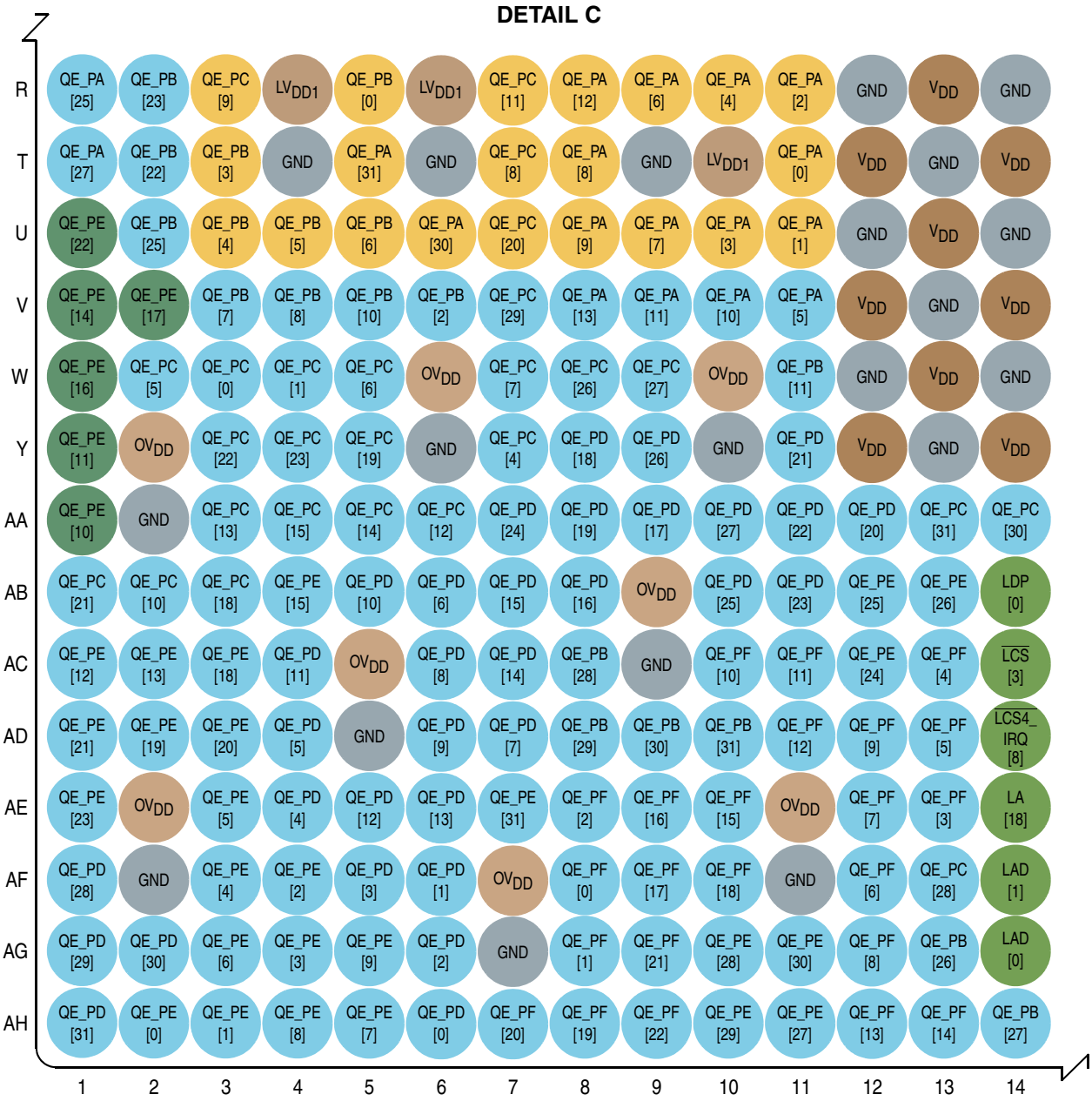


Figure 5. MPC8569E Detail C Ball Map

The following figure provides detailed view D of the MPC8569E 783-pin BGA ball map diagram.

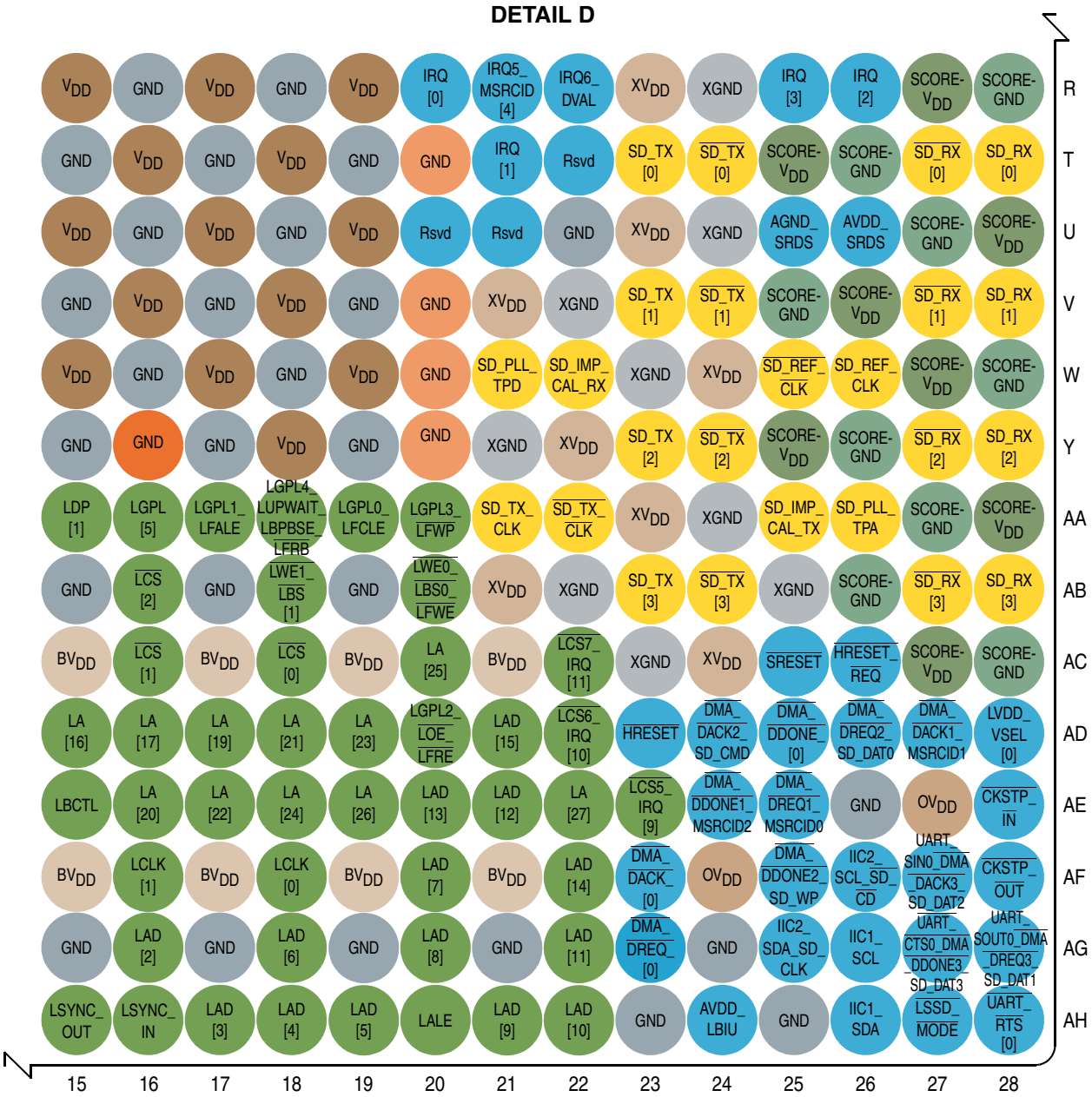


Figure 6. MPC8569E Detail D Ball Map

1.2 Pinout List

The following table provides the pinout listing for the MPC8569E 783 FC-PBGA package.

Table 1. MPC8569E Pinout Listing

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
Clocks				
RTC	M25	I	OV_{DD}	—
SYSCLK	P25	I	OV_{DD}	—
DDR SDRAM Memory Interface				
D1_MA0	E18	O	GV_{DD}	—
D1_MA1	A18	O	GV_{DD}	—
D1_MA2	H19	O	GV_{DD}	—
D1_MA3	G20	O	GV_{DD}	—
D1_MA4	B18	O	GV_{DD}	—
D1_MA5	H18	O	GV_{DD}	—
D1_MA6	C18	O	GV_{DD}	—
D1_MA7	J21	O	GV_{DD}	—
D1_MA8	E19	O	GV_{DD}	—
D1_MA9	G19	O	GV_{DD}	—
D1_MA10	J18	O	GV_{DD}	—
D1_MA11	A19	O	GV_{DD}	—
D1_MA12	J22	O	GV_{DD}	—
D1_MA13	A15	O	GV_{DD}	—
D1_MA14	D20	O	GV_{DD}	—
D1_MA15	C15	O	GV_{DD}	—
D1_MBA0	K17	O	GV_{DD}	—
D1_MBA1	F18	O	GV_{DD}	—
D1_MBA2	E20	O	GV_{DD}	—
$\overline{\text{D1\_MCAS}}$	J17	O	GV_{DD}	—
D1_MCK0	E24	O	GV_{DD}	—
$\overline{\text{D1\_MCK0}}$	E23	O	GV_{DD}	—
D1_MCK1	J24	O	GV_{DD}	—
$\overline{\text{D1\_MCK1}}$	J23	O	GV_{DD}	—
D1_MCK2	C20	O	GV_{DD}	—
$\overline{\text{D1\_MCK2}}$	C19	O	GV_{DD}	—
D1_MCKE0	G21	O	GV_{DD}	—
D1_MCKE1	J20	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D1_MCKE2	C17	O	GV_{DD}	—
D1_MCKE3	A16	O	GV_{DD}	—
$\overline{\text{D1\_MCS0}}$	D17	O	GV_{DD}	—
$\overline{\text{D1\_MCS1}}$	K16	O	GV_{DD}	—
$\overline{\text{D1\_MCS2}}$	K20	O	GV_{DD}	—
$\overline{\text{D1\_MCS3}}$	G16	O	GV_{DD}	—
D1_MDIC0	A20	I/O	GV_{DD}	27
D1_MDIC1	A17	I/O	GV_{DD}	27
D1_MDM0	A27	I/O	GV_{DD}	—
D1_MDM1	E27	I/O	GV_{DD}	—
D1_MDM2	J27	I/O	GV_{DD}	—
D1_MDM3	A23	I/O	GV_{DD}	—
D1_MDM8	E22	I/O	GV_{DD}	—
D1_MDQ0	C28	I/O	GV_{DD}	—
D1_MDQ1	C27	I/O	GV_{DD}	—
D1_MDQ2	C25	I/O	GV_{DD}	—
D1_MDQ3	B25	I/O	GV_{DD}	—
D1_MDQ4	B28	I/O	GV_{DD}	—
D1_MDQ5	A28	I/O	GV_{DD}	—
D1_MDQ6	A26	I/O	GV_{DD}	—
D1_MDQ7	A25	I/O	GV_{DD}	—
D1_MDQ8	G28	I/O	GV_{DD}	—
D1_MDQ9	G27	I/O	GV_{DD}	—
D1_MDQ10	G25	I/O	GV_{DD}	—
D1_MDQ11	F25	I/O	GV_{DD}	—
D1_MDQ12	F28	I/O	GV_{DD}	—
D1_MDQ13	E28	I/O	GV_{DD}	—
D1_MDQ14	E26	I/O	GV_{DD}	—
D1_MDQ15	E25	I/O	GV_{DD}	—
D1_MDQ16	L27	I/O	GV_{DD}	—
D1_MDQ17	L26	I/O	GV_{DD}	—
D1_MDQ18	K23	I/O	GV_{DD}	—
D1_MDQ19	K25	I/O	GV_{DD}	—
D1_MDQ20	K28	I/O	GV_{DD}	—
D1_MDQ21	J28	I/O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D1_MDQ22	J26	I/O	GV_{DD}	—
D1_MDQ23	J25	I/O	GV_{DD}	—
D1_MDQ24	C24	I/O	GV_{DD}	—
D1_MDQ25	C22	I/O	GV_{DD}	—
D1_MDQ26	C21	I/O	GV_{DD}	—
D1_MDQ27	B21	I/O	GV_{DD}	—
D1_MDQ28	B24	I/O	GV_{DD}	—
D1_MDQ29	A24	I/O	GV_{DD}	—
D1_MDQ30	A22	I/O	GV_{DD}	—
D1_MDQ31	A21	I/O	GV_{DD}	—
D1_MDQS0	D26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS0}}$	C26	I/O	GV_{DD}	—
D1_MDQS1	H26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS1}}$	G26	I/O	GV_{DD}	—
D1_MDQS2	K24	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS2}}$	L25	I/O	GV_{DD}	—
D1_MDQS3	D23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS3}}$	C23	I/O	GV_{DD}	—
D1_MDQS8	H23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS8}}$	G23	I/O	GV_{DD}	—
D1_MECC0	G24	I/O	GV_{DD}	—
D1_MECC1	H22	I/O	GV_{DD}	—
D1_MECC2	G22	I/O	GV_{DD}	—
D1_MECC3	F21	I/O	GV_{DD}	—
D1_MECC4	F24	I/O	GV_{DD}	—
D1_MECC5	D22	I/O	GV_{DD}	—
D1_MECC6	E21	I/O	GV_{DD}	—
D1_MECC7	D21	I/O	GV_{DD}	—
D1_MODT0	C16	O	GV_{DD}	—
D1_MODT1	J16	O	GV_{DD}	—
D1_MODT2	G17	O	GV_{DD}	—
D1_MODT3	E16	O	GV_{DD}	—
D1_MAPAR_OUT	E15	O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	F15	I	GV_{DD}	—
$\overline{\text{D1\_MRAS}}$	G18	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{D1\_MWE}}$	E17	O	GV_{DD}	—
D2_MA0	E4	O	GV_{DD}	—
D2_MA1	A4	O	GV_{DD}	—
D2_MA2	J7	O	GV_{DD}	—
D2_MA3	G6	O	GV_{DD}	—
D2_MA4	B4	O	GV_{DD}	—
D2_MA5	H4	O	GV_{DD}	—
D2_MA6	G3	O	GV_{DD}	—
D2_MA7	J8	O	GV_{DD}	—
D2_MA8	E5	O	GV_{DD}	—
D2_MA9	G5	O	GV_{DD}	—
D2_MA10	J6	O	GV_{DD}	—
D2_MA11	A5	O	GV_{DD}	—
D2_MA12	J9	O	GV_{DD}	—
D2_MA13	D3	O	GV_{DD}	—
D2_MA14	D6	O	GV_{DD}	—
D2_MA15	B1	O	GV_{DD}	—
D2_MBA0	J5	O	GV_{DD}	—
D2_MBA1	F4	O	GV_{DD}	—
D2_MBA2	E6	O	GV_{DD}	—
$\overline{\text{D2\_MCAS}}$	J4	O	GV_{DD}	—
D2_MCK0	E10	O	GV_{DD}	—
$\overline{\text{D2\_MCK0}}$	E9	O	GV_{DD}	—
D2_MCK1	J11	O	GV_{DD}	—
$\overline{\text{D2\_MCK1}}$	J10	O	GV_{DD}	—
D2_MCK2	C6	O	GV_{DD}	—
$\overline{\text{D2\_MCK2}}$	C5	O	GV_{DD}	—
D2_MCKE0	G7	O	GV_{DD}	—
D2_MCKE1	K8	O	GV_{DD}	—
D2_MCKE2	C2	O	GV_{DD}	—
D2_MCKE3	A2	O	GV_{DD}	—
$\overline{\text{D2\_MCS0}}$	E3	O	GV_{DD}	—
$\overline{\text{D2\_MCS1}}$	A6	O	GV_{DD}	—
$\overline{\text{D2\_MCS2}}$	H7	O	GV_{DD}	—
$\overline{\text{D2\_MCS3}}$	G2	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D2_MDIC0	J2	I/O	GV_{DD}	27
D2_MDIC1	L2	I/O	GV_{DD}	27
D2_MDM0/D1_MDM4	A13	I/O	GV_{DD}	—
D2_MDM1/D1_MDM5	D13	I/O	GV_{DD}	—
D2_MDM2/D1_MDM6	G14	I/O	GV_{DD}	—
D2_MDM3/D1_MDM7	A9	I/O	GV_{DD}	—
D2_MDM8	E8	I/O	GV_{DD}	—
D2_MDQ0/D1_MDQ32	B14	I/O	GV_{DD}	—
D2_MDQ1/D1_MDQ33	C14	I/O	GV_{DD}	—
D2_MDQ2/D1_MDQ34	C11	I/O	GV_{DD}	—
D2_MDQ3/D1_MDQ35	B11	I/O	GV_{DD}	—
D2_MDQ4/D1_MDQ36	B15	I/O	GV_{DD}	—
D2_MDQ5/D1_MDQ37	A14	I/O	GV_{DD}	—
D2_MDQ6/D1_MDQ38	A12	I/O	GV_{DD}	—
D2_MDQ7/D1_MDQ39	A11	I/O	GV_{DD}	—
D2_MDQ8/D1_MDQ40	F14	I/O	GV_{DD}	—
D2_MDQ9/D1_MDQ41	F13	I/O	GV_{DD}	—
D2_MDQ10/D1_MDQ42	G11	I/O	GV_{DD}	—
D2_MDQ11/D1_MDQ43	F11	I/O	GV_{DD}	—
D2_MDQ12/D1_MDQ44	E14	I/O	GV_{DD}	—
D2_MDQ13/D1_MDQ45	D14	I/O	GV_{DD}	—
D2_MDQ14/D1_MDQ46	D12	I/O	GV_{DD}	—
D2_MDQ15/D1_MDQ47	E11	I/O	GV_{DD}	—
D2_MDQ16/D1_MDQ48	J15	I/O	GV_{DD}	—
D2_MDQ17/D1_MDQ49	J14	I/O	GV_{DD}	—
D2_MDQ18/D1_MDQ50	K13	I/O	GV_{DD}	—
D2_MDQ19/D1_MDQ51	J12	I/O	GV_{DD}	—
D2_MDQ20/D1_MDQ52	H15	I/O	GV_{DD}	—
D2_MDQ21/D1_MDQ53	G15	I/O	GV_{DD}	—
D2_MDQ22/D1_MDQ54	G13	I/O	GV_{DD}	—
D2_MDQ23/D1_MDQ55	H12	I/O	GV_{DD}	—
D2_MDQ24/D1_MDQ56	C10	I/O	GV_{DD}	—
D2_MDQ25/D1_MDQ57	C8	I/O	GV_{DD}	—
D2_MDQ26/D1_MDQ58	C7	I/O	GV_{DD}	—
D2_MDQ27/D1_MDQ59	B7	I/O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D2_MDQ28/D1_MDQ60	B10	I/O	GV_{DD}	—
D2_MDQ29/D1_MDQ61	A10	I/O	GV_{DD}	—
D2_MDQ30/D1_MDQ62	A8	I/O	GV_{DD}	—
D2_MDQ31/D1_MDQ63	A7	I/O	GV_{DD}	—
D2_MDQS0/D1_MDQS4	C12	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS0}}$/$\overline{\text{D1\_MDQS4}}$	C13	I/O	GV_{DD}	—
D2_MDQS1/D1_MDQS5	G12	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS1}}$/$\overline{\text{D1\_MDQS5}}$	F12	I/O	GV_{DD}	—
D2_MDQS2/D1_MDQS6	J13	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS2}}$/$\overline{\text{D1\_MDQS6}}$	K14	I/O	GV_{DD}	—
D2_MDQS3/D1_MDQS7	D9	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS3}}$/$\overline{\text{D1\_MDQS7}}$	C9	I/O	GV_{DD}	—
D2_MDQS8	H9	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS8}}$	G9	I/O	GV_{DD}	—
D2_MECC0	G10	I/O	GV_{DD}	—
D2_MECC1	H8	I/O	GV_{DD}	—
D2_MECC2	G8	I/O	GV_{DD}	—
D2_MECC3	F7	I/O	GV_{DD}	—
D2_MECC4	F10	I/O	GV_{DD}	—
D2_MECC5	D8	I/O	GV_{DD}	—
D2_MECC6	E7	I/O	GV_{DD}	—
D2_MECC7	D7	I/O	GV_{DD}	—
D2_MODT0	C1	O	GV_{DD}	—
D2_MODT1	A3	O	GV_{DD}	—
D2_MODT2	H3	O	GV_{DD}	—
D2_MODT3	E1	O	GV_{DD}	—
D2_MAPAR_OUT	F1	O	GV_{DD}	—
$\overline{\text{D2\_MAPAR\_ERR}}$	G1	I	GV_{DD}	—
$\overline{\text{D2\_MRAS}}$	G4	O	GV_{DD}	—
$\overline{\text{D2\_MWE}}$	E2	O	GV_{DD}	—
DMA				
$\overline{\text{DMA\_DACK0}}$	AF23	O	OV_{DD}	2
$\overline{\text{DMA\_DACK1}}$/MSRCID1	AD27	O	OV_{DD}	11
$\overline{\text{DMA\_DACK2}}$/SD_CMD	AD24	O	OV_{DD}	—
$\overline{\text{DMA\_DDONE0}}$	AD25	O	OV_{DD}	2

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
DMA_DDONE1/MSRCID2	AE24	O	OV_{DD}	2
DMA_DDONE2/SD_WP	AF25	O	OV_{DD}	—
DMA_DREQ0	AG23	I	OV_{DD}	—
DMA_DREQ1/MSRCID0	AE25	I	OV_{DD}	—
DMA_DREQ2/SD_DAT0	AD26	I	OV_{DD}	—
DUART				
UART_SOUT0/DMA_DREQ3/SD_DAT1	AG28	O	OV_{DD}	2
UART_SIN0/DMA_DACK3/SD_DAT2	AF27	I	OV_{DD}	—
UART_CTS0/DMA_DDONE3/SD_DAT3	AG27	I	OV_{DD}	—
UART_RTS0	AH28	O	OV_{DD}	—
Enhanced Local Bus Controller Interface				
LA16	AD15	O	BV_{DD}	2
LA17	AD16	O	BV_{DD}	2
LA18	AE14	O	BV_{DD}	2
LA19	AD17	O	BV_{DD}	2
LA20	AE16	O	BV_{DD}	2
LA21	AD18	O	BV_{DD}	2
LA22	AE17	O	BV_{DD}	11
LA23	AD19	O	BV_{DD}	2
LA24	AE18	O	BV_{DD}	18
LA25	AC20	O	BV_{DD}	18
LA26	AE19	O	BV_{DD}	18
LA27	AE22	O	BV_{DD}	18
LAD0	AG14	I/O	BV_{DD}	23
LAD1	AF14	I/O	BV_{DD}	23
LAD2	AG16	I/O	BV_{DD}	23
LAD3	AH17	I/O	BV_{DD}	23
LAD4	AH18	I/O	BV_{DD}	23
LAD5	AH19	I/O	BV_{DD}	23
LAD6	AG18	I/O	BV_{DD}	23
LAD7	AF20	I/O	BV_{DD}	23
LAD8	AG20	I/O	BV_{DD}	23
LAD9	AH21	I/O	BV_{DD}	23
LAD10	AH22	I/O	BV_{DD}	23
LAD11	AG22	I/O	BV_{DD}	23

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
LAD12	AE21	I/O	BV_{DD}	23
LAD13	AE20	I/O	BV_{DD}	23
LAD14	AF22	I/O	BV_{DD}	23
LAD15	AD21	I/O	BV_{DD}	23
LALE	AH20	O	BV_{DD}	20
LBCTL	AE15	O	BV_{DD}	20
LCLK0	AF18	O	BV_{DD}	11
LCLK1	AF16	O	BV_{DD}	11
$\overline{\text{LCS0}}$	AC18	O	BV_{DD}	2
$\overline{\text{LCS1}}$	AC16	O	BV_{DD}	2
$\overline{\text{LCS2}}$	AB16	O	BV_{DD}	2
$\overline{\text{LCS3}}$	AC14	O	BV_{DD}	21
$\overline{\text{LCS4}}$/IRQ8	AD14	I/O	BV_{DD}	21
$\overline{\text{LCS5}}$/IRQ9	AE23	I/O	BV_{DD}	21
$\overline{\text{LCS6}}$/IRQ10	AD22	I/O	BV_{DD}	21
$\overline{\text{LCS7}}$/IRQ11	AC22	I/O	BV_{DD}	21
LDP0	AB14	I/O	BV_{DD}	—
LDP1	AA15	I/O	BV_{DD}	—
LGPL0/LFCLE	AA19	O	BV_{DD}	2
LGPL1/LFALE	AA17	O	BV_{DD}	2
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	AD20	O	BV_{DD}	20
LGPL3/$\overline{\text{LFWP}}$	AA20	O	BV_{DD}	2
LGPL4/LUPWAIT/LBPBSE/$\overline{\text{LFRB}}$	AA18	I/O	BV_{DD}	29
LGPL5	AA16	O	BV_{DD}	2
LSYNC_IN	AH16	I	BV_{DD}	—
LSYNC_OUT	AH15	O	BV_{DD}	—
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$LFWE	AB20	O	BV_{DD}	11
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$	AB18	O	BV_{DD}	24
I^2C				
IIC1_SDA	AH26	I/O	OV_{DD}	5, 28
IIC1_SCL	AG26	I/O	OV_{DD}	5, 28
IIC2_SDA/SD_CLK	AG25	I/O	OV_{DD}	3
IIC2_SCL/$\overline{\text{SD\_CD}}$	AF26	I/O	OV_{DD}	3
JTAG				
TCK	N21	I	OV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
TDI	P21	I	OV_{DD}	26
TDO	P23	O	OV_{DD}	25
TMS	N22	I	OV_{DD}	26
$\overline{\text{TRST}}$	P22	I	OV_{DD}	26
Programmable Interrupt Controller				
IRQ0	R20	I	OV_{DD}	—
IRQ1	T21	I	OV_{DD}	—
IRQ2	R26	I	OV_{DD}	—
IRQ3	R25	I	OV_{DD}	—
IRQ4/MSRCID3	N20	I	OV_{DD}	—
IRQ5/MSRCID4	R21	I	OV_{DD}	—
IRQ6/MDVAL	R22	I	OV_{DD}	—
$\overline{\text{IRQ\_OUT}}$	M20	O	OV_{DD}	5, 6, 11
$\overline{\text{MCP}}$	M22	I	OV_{DD}	6
$\overline{\text{UDE}}$	M21	I	OV_{DD}	6
QUICC Engine Block				
QE_PA0	T11	I/O	$LV_{DD}1$	—
QE_PA1	U11	I/O	$LV_{DD}1$	—
QE_PA2	R11	I/O	$LV_{DD}1$	—
QE_PA3	U10	I/O	$LV_{DD}1$	—
QE_PA4	R10	I/O	$LV_{DD}1$	—
QE_PA5	V11	I/O	OV_{DD}	—
QE_PA6	R9	I/O	$LV_{DD}1$	—
QE_PA7	U9	I/O	$LV_{DD}1$	—
QE_PA8	T8	I/O	$LV_{DD}1$	—
QE_PA9	U8	I/O	$LV_{DD}1$	—
QE_PA10	V10	I/O	OV_{DD}	—
QE_PA11	V9	I/O	OV_{DD}	—
QE_PA12	R8	I/O	$LV_{DD}1$	—
QE_PA13	V8	I/O	OV_{DD}	—
QE_PA14	P7	I/O	$LV_{DD}2$	—
QE_PA15	L6	I/O	$LV_{DD}2$	—
QE_PA16	M6	I/O	$LV_{DD}2$	—
QE_PA17	N6	I/O	$LV_{DD}2$	—
QE_PA18	L5	I/O	$LV_{DD}2$	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PA19	P1	I/O	OV_{DD}	—
QE_PA20	M5	I/O	$LV_{DD}2$	—
QE_PA21	N5	I/O	$LV_{DD}2$	—
QE_PA22	L4	I/O	$LV_{DD}2$	—
QE_PA23	M4	I/O	$LV_{DD}2$	—
QE_PA24	N1	I/O	OV_{DD}	—
QE_PA25	R1	I/O	OV_{DD}	—
QE_PA26	N4	I/O	$LV_{DD}2$	—
QE_PA27	T1	I/O	OV_{DD}	—
QE_PA28	N2	I/O	OV_{DD}	—
QE_PA29	P6	I/O	$LV_{DD}1$	—
QE_PA30	U6	I/O	$LV_{DD}1$	—
QE_PA31	T5	I/O	$LV_{DD}1$	—
QE_PB0	R5	I/O	$LV_{DD}1$	—
QE_PB1	P5	I/O	$LV_{DD}1$	—
QE_PB2	V6	I/O	OV_{DD}	—
QE_PB3	T3	I/O	$LV_{DD}1$	—
QE_PB4	U3	I/O	$LV_{DD}1$	—
QE_PB5	U4	I/O	$LV_{DD}1$	—
QE_PB6	U5	I/O	$LV_{DD}1$	—
QE_PB7	V3	I/O	OV_{DD}	11
QE_PB8	V4	I/O	OV_{DD}	—
QE_PB9	P4	I/O	$LV_{DD}1$	—
QE_PB10	V5	I/O	OV_{DD}	—
QE_PB11	W11	I/O	OV_{DD}	—
QE_PB12	L11	I/O	$LV_{DD}2$	—
QE_PB13	M11	I/O	$LV_{DD}2$	—
QE_PB14	N11	I/O	$LV_{DD}2$	—
QE_PB15	P11	I/O	$LV_{DD}2$	—
QE_PB16	P10	I/O	$LV_{DD}2$	—
QE_PB17	P2	I/O	OV_{DD}	—
QE_PB18	L10	I/O	$LV_{DD}2$	—
QE_PB19	M9	I/O	$LV_{DD}2$	—
QE_PB20	N9	I/O	$LV_{DD}2$	—
QE_PB21	P9	I/O	$LV_{DD}2$	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PB22	T2	I/O	OV_{DD}	—
QE_PB23	R2	I/O	OV_{DD}	—
QE_PB24	P8	I/O	$LV_{DD}2$	—
QE_PB25	U2	I/O	OV_{DD}	—
QE_PB26	AG13	I/O	OV_{DD}	11
QE_PB27	AH14	I/O	OV_{DD}	22
QE_PB28	AC8	I/O	OV_{DD}	22
QE_PB29	AD8	I/O	OV_{DD}	—
QE_PB30	AD9	I/O	OV_{DD}	—
QE_PB31	AD10	I/O	OV_{DD}	11
QE_PC0	W3	I/O	OV_{DD}	—
QE_PC1	W4	I/O	OV_{DD}	—
QE_PC2	N3	I/O	$LV_{DD}2$	—
QE_PC3	L3	I/O	$LV_{DD}2$	—
QE_PC4	Y7	I/O	OV_{DD}	22
QE_PC5	W2	I/O	OV_{DD}	—
QE_PC6	W5	I/O	OV_{DD}	—
QE_PC7	W7	I/O	OV_{DD}	—
QE_PC8	T7	I/O	$LV_{DD}1$	—
QE_PC9	R3	I/O	$LV_{DD}1$	—
QE_PC10	AB2	I/O	OV_{DD}	—
QE_PC11	R7	I/O	$LV_{DD}1$	—
QE_PC12	AA6	I/O	OV_{DD}	—
QE_PC13	AA3	I/O	OV_{DD}	—
QE_PC14	AA5	I/O	OV_{DD}	—
QE_PC15	AA4	I/O	OV_{DD}	—
QE_PC16	L7	I/O	$LV_{DD}2$	—
QE_PC17	M8	I/O	$LV_{DD}2$	—
QE_PC18	AB3	I/O	OV_{DD}	—
QE_PC19	Y5	I/O	OV_{DD}	—
QE_PC20	U7	I/O	$LV_{DD}1$	—
QE_PC21	AB1	I/O	OV_{DD}	—
QE_PC22	Y3	I/O	OV_{DD}	—
QE_PC23	Y4	I/O	OV_{DD}	—
QE_PC24	N8	I/O	$LV_{DD}2$	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PC25	P3	I/O	$LV_{DD}1$	—
QE_PC26	W8	I/O	OV_{DD}	—
QE_PC27	W9	I/O	OV_{DD}	—
QE_PC28	AF13	I/O	OV_{DD}	—
QE_PC29	V7	I/O	OV_{DD}	—
QE_PC30	AA14	I/O	OV_{DD}	—
QE_PC31	AA13	I/O	OV_{DD}	—
QE_PD0	AH6	I/O	OV_{DD}	11
QE_PD1	AF6	I/O	OV_{DD}	—
QE_PD2	AG6	I/O	OV_{DD}	—
QE_PD3	AF5	I/O	OV_{DD}	—
QE_PD4	AE4	I/O	OV_{DD}	22
QE_PD5	AD4	I/O	OV_{DD}	—
QE_PD6	AB6	I/O	OV_{DD}	—
QE_PD7	AD7	I/O	OV_{DD}	—
QE_PD8	AC6	I/O	OV_{DD}	—
QE_PD9	AD6	I/O	OV_{DD}	—
QE_PD10	AB5	I/O	OV_{DD}	—
QE_PD11	AC4	I/O	OV_{DD}	—
QE_PD12	AE5	I/O	OV_{DD}	—
QE_PD13	AE6	I/O	OV_{DD}	—
QE_PD14	AC7	I/O	OV_{DD}	—
QE_PD15	AB7	I/O	OV_{DD}	—
QE_PD16	AB8	I/O	OV_{DD}	—
QE_PD17	AA9	I/O	OV_{DD}	—
QE_PD18	Y8	I/O	OV_{DD}	—
QE_PD19	AA8	I/O	OV_{DD}	—
QE_PD20	AA12	I/O	OV_{DD}	—
QE_PD21	Y11	I/O	OV_{DD}	—
QE_PD22	AA11	I/O	OV_{DD}	—
QE_PD23	AB11	I/O	OV_{DD}	—
QE_PD24	AA7	I/O	OV_{DD}	—
QE_PD25	AB10	I/O	OV_{DD}	—
QE_PD26	Y9	I/O	OV_{DD}	—
QE_PD27	AA10	I/O	OV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PD28	AF1	I/O	OV_{DD}	—
QE_PD29	AG1	I/O	OV_{DD}	—
QE_PD30	AG2	I/O	OV_{DD}	—
QE_PD31	AH1	I/O	OV_{DD}	—
QE_PE0	AH2	I/O	OV_{DD}	—
QE_PE1	AH3	I/O	OV_{DD}	—
QE_PE2	AF4	I/O	OV_{DD}	—
QE_PE3	AG4	I/O	OV_{DD}	—
QE_PE4	AF3	I/O	OV_{DD}	—
QE_PE5	AE3	I/O	OV_{DD}	—
QE_PE6	AG3	I/O	OV_{DD}	—
QE_PE7	AH5	I/O	OV_{DD}	—
QE_PE8	AH4	I/O	OV_{DD}	—
QE_PE9	AG5	I/O	OV_{DD}	—
QE_PE10	AA1	I/O	OV_{DD}	—
QE_PE11	Y1	I/O	OV_{DD}	—
QE_PE12	AC1	I/O	OV_{DD}	—
QE_PE13	AC2	I/O	OV_{DD}	—
QE_PE14	V1	I/O	OV_{DD}	—
QE_PE15	AB4	I/O	OV_{DD}	—
QE_PE16	W1	I/O	OV_{DD}	—
QE_PE17	V2	I/O	OV_{DD}	—
QE_PE18	AC3	I/O	OV_{DD}	—
QE_PE19	AD2	I/O	OV_{DD}	—
QE_PE20	AD3	I/O	OV_{DD}	—
QE_PE21	AD1	I/O	OV_{DD}	—
QE_PE22	U1	I/O	OV_{DD}	—
QE_PE23	AE1	I/O	OV_{DD}	—
QE_PE24	AC12	I/O	OV_{DD}	11
QE_PE25	AB12	I/O	OV_{DD}	2
QE_PE26	AB13	I/O	OV_{DD}	11
QE_PE27	AH11	I/O	OV_{DD}	19
QE_PE28	AG10	I/O	OV_{DD}	19

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PE29	AH10	I/O	OV_{DD}	19
QE_PE30	AG11	I/O	OV_{DD}	—
QE_PE31	AE7	I/O	OV_{DD}	—
QE_PF0	AF8	I/O	OV_{DD}	—
QE_PF1	AG8	I/O	OV_{DD}	—
QE_PF2	AE8	I/O	OV_{DD}	—
QE_PF3	AE13	I/O	OV_{DD}	—
QE_PF4	AC13	I/O	OV_{DD}	—
QE_PF5	AD13	I/O	OV_{DD}	—
QE_PF6	AF12	I/O	OV_{DD}	—
QE_PF7	AE12	I/O	OV_{DD}	—
QE_PF8	AG12	I/O	OV_{DD}	—
QE_PF9	AD12	I/O	OV_{DD}	2
QE_PF10	AC10	I/O	OV_{DD}	2
QE_PF11	AC11	I/O	OV_{DD}	2
QE_PF12	AD11	I/O	OV_{DD}	—
QE_PF13	AH12	I/O	OV_{DD}	11
QE_PF14	AH13	I/O	OV_{DD}	2
QE_PF15	AE10	I/O	OV_{DD}	—
QE_PF16	AE9	I/O	OV_{DD}	—
QE_PF17	AF9	I/O	OV_{DD}	—
QE_PF18	AF10	I/O	OV_{DD}	—
QE_PF19	AH8	I/O	OV_{DD}	—
QE_PF20	AH7	I/O	OV_{DD}	—
QE_PF21	AG9	I/O	OV_{DD}	—
QE_PF22	AH9	I/O	OV_{DD}	—
SerDes				
SD_IMP_CAL_RX	W22	I	—	7
SD_IMP_CAL_TX	AA25	I	—	17
SD_PLL_TPA	AA26	O	AV_{DD}_SRDS	8
SD_PLL_TPD	W21	O	XV_{DD}	8
SD_REF_CLK	W26	I	ScoreVDD	—
$\overline{\text{SD\_REF\_CLK}}$	W25	I	ScoreVDD	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
SD_RX0	T28	I	ScoreVDD	30
$\overline{\text{SD\_RX0}}$	T27	I	ScoreVDD	30
SD_RX1	V28	I	ScoreVDD	30
$\overline{\text{SD\_RX1}}$	V27	I	ScoreVDD	30
SD_RX2	Y28	I	ScoreVDD	30
$\overline{\text{SD\_RX2}}$	Y27	I	ScoreVDD	30
SD_RX3	AB28	I	ScoreVDD	30
$\overline{\text{SD\_RX3}}$	AB27	I	ScoreVDD	30
SD_TX0	T23	O	XV_{DD}	31
$\overline{\text{SD\_TX0}}$	T24	O	XV_{DD}	31
SD_TX1	V23	O	XV_{DD}	31
$\overline{\text{SD\_TX1}}$	V24	O	XV_{DD}	31
SD_TX2	Y23	O	XV_{DD}	31
$\overline{\text{SD\_TX2}}$	Y24	O	XV_{DD}	31
SD_TX3	AB23	O	XV_{DD}	31
$\overline{\text{SD\_TX3}}$	AB24	O	XV_{DD}	31
SD_TX_CLK	AA21	O	XV_{DD}	8
$\overline{\text{SD\_TX\_CLK}}$	AA22	O	XV_{DD}	8
System Control				
$\overline{\text{CKSTP\_IN}}$	AE28	I	OV_{DD}	4
$\overline{\text{CKSTP\_OUT}}$	AF28	O	OV_{DD}	5, 6, 11
$\overline{\text{HRESET}}$	AD23	I	OV_{DD}	4
$\overline{\text{HRESET\_REQ}}$	AC26	O	OV_{DD}	11
$\overline{\text{SRESET}}$	AC25	I	OV_{DD}	4
Debug				
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	P24	O	OV_{DD}	11
CLK_OUT	M24	O	OV_{DD}	—
TRIG_IN	N25	I	OV_{DD}	—
Voltage Control				
LVDD_VSEL0	AD28	I	OV_{DD}	15
LVDD_VSEL1	P26	I	OV_{DD}	16
BVDD_VSEL0	N26	I	OV_{DD}	14
BVDD_VSEL1	P20	I	OV_{DD}	14
Design for Test				
$\overline{\text{LSSD\_MODE}}$	AH27	I	OV_{DD}	10

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
Power Management				
ASLEEP	M23	O	OV_{DD}	11
Thermal Management				
THERM0	U21	—	Internal temperature diode cathode	32
THERM1	U20	—	Internal temperature diode anode	32
Reserved	T22	—	—	9
Analog				
D1_MVREF	N27	Reference voltage for DDR	MV_{REF}	—
D2_MVREF	J1			—
Power and Ground				
V_{DD}	L13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	L17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	L19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	P12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	P16	1.0-V/1.1-V core power supply	V_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
V_{DD}	P18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	R19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	T18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	U19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	V18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	W19	1.0-V/1.1-V core power supply	V_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
V_{DD}	Y12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	Y14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	Y18	1.0-V/1.1-V core power supply	V_{DD}	—
BV_{DD}	AC15	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AC17	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AC19	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AC21	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF15	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF17	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF19	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
BV_{DD}	AF21	3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply	BV_{DD}	—
GV_{DD}	B12	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B16	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B19	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B2	1.8-/1.5-V DDR power supply	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GV_{DD}	B22	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B26	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B5	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	B8	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	C3	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D1	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D10	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D15	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D18	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D24	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D27	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	D4	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	E12	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F16	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F19	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F2	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F22	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F26	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F5	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	F8	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H10	1.8-/1.5-V DDR power supply	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GV_{DD}	H13	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H16	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H2	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H20	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H24	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H27	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H5	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	J19	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	J3	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K10	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K11	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K18	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K22	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K26	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K3	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K4	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K6	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K9	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L15	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L21	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L23	1.8-/1.5-V DDR power supply	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
$LV_{DD}1$	R4	3.3-/2.5-V Ethernet power supply	$LV_{DD}1$	—
$LV_{DD}1$	R6	3.3-/2.5-V Ethernet power supply	$LV_{DD}1$	—
$LV_{DD}1$	T10	3.3-/2.5-V Ethernet power supply	$LV_{DD}1$	—
$LV_{DD}2$	M10	3.3-/2.5-V Ethernet power supply	$LV_{DD}2$	—
$LV_{DD}2$	M3	3.3-/2.5-V Ethernet power supply	$LV_{DD}2$	—
$LV_{DD}2$	M7	3.3-/2.5-V Ethernet power supply	$LV_{DD}2$	—
OV_{DD}	AB9	3.3-V power supply	OV_{DD}	—
OV_{DD}	AC5	3.3-V power supply	OV_{DD}	—
OV_{DD}	AE11	3.3-V power supply	OV_{DD}	—
OV_{DD}	AE2	3.3-V power supply	OV_{DD}	—
OV_{DD}	AE27	3.3-V power supply	OV_{DD}	—
OV_{DD}	AF24	3.3-V power supply	OV_{DD}	—
OV_{DD}	AF7	3.3-V power supply	OV_{DD}	—
OV_{DD}	M26	3.3-V power supply	OV_{DD}	—
OV_{DD}	N23	3.3-V power supply	OV_{DD}	—
OV_{DD}	W10	3.3-V power supply	OV_{DD}	—
OV_{DD}	W6	3.3-V power supply	OV_{DD}	—
OV_{DD}	Y2	3.3-V power supply	OV_{DD}	—
ScoreVDD	AA28	1.0-V/1.1-V SerDes power supply	ScoreVDD	—
ScoreVDD	AC27	1.0-V/1.1-V SerDes power supply	ScoreVDD	—
ScoreVDD	R27	1.0-V/1.1-V SerDes power supply	ScoreVDD	—
ScoreVDD	T25	1.0-V/1.1-V SerDes power supply	ScoreVDD	—
ScoreVDD	U28	1.0-V/1.1-V SerDes power supply	ScoreVDD	—
ScoreVDD	V26	1.0-V/1.1-V SerDes power supply	ScoreVDD	—
ScoreVDD	W27	1.0-V/1.1-V SerDes power supply	ScoreVDD	—
ScoreVDD	Y25	1.0-V/1.1-V SerDes power supply	ScoreVDD	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
SENSEVDD	P14	Core supply sense	V_{DD}	13
XV_{DD}	AA23	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	AB21	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	AC24	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	R23	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	U23	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	V21	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	W24	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
XV_{DD}	Y22	1.0-V/1.1-V SerDes I/O power supply	XV_{DD}	—
AV_{DD}_CORE	L1	1.0-V/1.1-V AV_{DD} supply for the core PLL	—	12
AV_{DD}_DDR	M28	1.0-V/1.1-V AV_{DD} supply for the DDR PLL	—	12
AV_{DD}_LBIU	AH24	1.0-V/1.1-V AV_{DD} supply for the eLBC PLL	—	12
AV_{DD}_PLAT	N28	1.0-V/1.1-V AV_{DD} supply for the platform PLL	—	12
AV_{DD}_QE	K1	1.0-V/1.1-V AV_{DD} supply for the QUICC Engine block PLL	—	12
AV_{DD}_SRDS	U26	1.0-V/1.1-V AV_{DD} supply for the SerDes PLL	—	12
GND	AA2	—	—	—
GND	AB15	—	—	—
GND	AB17	—	—	—
GND	AB19	—	—	—
GND	AC9	—	—	—
GND	AD5	—	—	—
GND	AE26	—	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	AF11	—	—	—
GND	AF2	—	—	—
GND	AG15	—	—	—
GND	AG17	—	—	—
GND	AG19	—	—	—
GND	AG21	—	—	—
GND	AG24	—	—	—
GND	AG7	—	—	—
GND	AH23	—	—	—
GND	AH25	—	—	—
GND	B13	—	—	—
GND	B17	—	—	—
GND	B20	—	—	—
GND	B23	—	—	—
GND	B27	—	—	—
GND	B3	—	—	—
GND	B6	—	—	—
GND	B9	—	—	—
GND	C4	—	—	—
GND	D11	—	—	—
GND	D16	—	—	—
GND	D19	—	—	—
GND	D2	—	—	—
GND	D25	—	—	—
GND	D28	—	—	—
GND	D5	—	—	—
GND	E13	—	—	—
GND	F17	—	—	—
GND	F20	—	—	—
GND	F23	—	—	—
GND	F27	—	—	—
GND	F3	—	—	—
GND	F6	—	—	—
GND	F9	—	—	—
GND	H1	—	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	H11	—	—	—
GND	H14	—	—	—
GND	H17	—	—	—
GND	H21	—	—	—
GND	H25	—	—	—
GND	H28	—	—	—
GND	H6	—	—	—
GND	K12	—	—	—
GND	K15	—	—	—
GND	K19	—	—	—
GND	K2	—	—	—
GND	K21	—	—	—
GND	K27	—	—	—
GND	K5	—	—	—
GND	K7	—	—	—
GND	L12	—	—	—
GND	L14	—	—	—
GND	L16	—	—	—
GND	L18	—	—	—
GND	L20	—	—	—
GND	L22	—	—	—
GND	L24	—	—	—
GND	L28	—	—	—
GND	L8	—	—	—
GND	L9	—	—	—
GND	M1	—	—	—
GND	M13	—	—	—
GND	M15	—	—	—
GND	M17	—	—	—
GND	M19	—	—	—
GND	M2	—	—	—
GND	M27	—	—	—
GND	N10	—	—	—
GND	N12	—	—	—
GND	N14	—	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	N16	—	—	—
GND	N18	—	—	—
GND	N24	—	—	—
GND	N7	—	—	—
GND	P13	—	—	—
GND	P17	—	—	—
GND	P19	—	—	—
GND	P27	—	—	—
GND	P28	—	—	—
GND	R12	—	—	—
GND	R14	—	—	—
GND	R16	—	—	—
GND	R18	—	—	—
GND	T13	—	—	—
GND	T15	—	—	—
GND	T17	—	—	—
GND	T19	—	—	—
GND	T4	—	—	—
GND	T6	—	—	—
GND	T9	—	—	—
GND	U12	—	—	—
GND	U14	—	—	—
GND	U16	—	—	—
GND	U18	—	—	—
GND	U22	—	—	—
GND	V13	—	—	—
GND	V15	—	—	—
GND	V17	—	—	—
GND	V19	—	—	—
GND	W12	—	—	—
GND	W14	—	—	—
GND	W16	—	—	—
GND	W18	—	—	—
GND	Y6	—	—	—
GND	Y10	—	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	Y13	—	—	—
GND	Y15	—	—	—
GND	Y16	—	—	—
GND	Y17	—	—	—
GND	Y19	—	—	—
GND	V20	—	—	—
GND	T20	—	—	—
GND	W20	—	—	—
GND	Y20	—	—	—
SENSEVSS	P15	Ground sense	—	13
SCOREGND	AA27	SerDes Core Logic GND	—	—
SCOREGND	AB26	SerDes Core Logic GND	—	—
SCOREGND	AC28	SerDes Core Logic GND	—	—
SCOREGND	R28	SerDes Core Logic GND	—	—
SCOREGND	T26	SerDes Core Logic GND	—	—
SCOREGND	U27	SerDes Core Logic GND	—	—
SCOREGND	V25	SerDes Core Logic GND	—	—
SCOREGND	W28	SerDes Core Logic GND	—	—
SCOREGND	Y26	SerDes Core Logic GND	—	—
XGND	AA24	SerDes Transceiver Pad GND	—	—
XGND	AB22	SerDes Transceiver Pad GND	—	—
XGND	AB25	SerDes Transceiver Pad GND	—	—
XGND	AC23	SerDes Transceiver Pad GND	—	—
XGND	R24	SerDes Transceiver Pad GND	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
XGND	U24	SerDes Transceiver Pad GND	—	—
XGND	V22	SerDes Transceiver Pad GND	—	—
XGND	W23	SerDes Transceiver Pad GND	—	—
XGND	Y21	SerDes Transceiver Pad GND	—	—
AGND_SRDS	U25	SerDes PLL GND	—	—

Notes:

1. All multiplexed signals are listed only once and do not reoccur.
2. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull-up or active driver is needed.
3. When configured as I2C, this pin is an open drain signal and recommend a pull-up resistor (1 kΩ) be placed on this pin to OV_{DD}. When configured as SD, this pin is not open drain and does not require a pull-up.
4. This pin has a weak internal pull-up resistor (~20 kΩ).
5. This pin is an open drain signal.
6. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
7. This pin requires a 200-Ω pull-down to ground.
8. Do not connect.
9. Recommend a weak pull-down resistor (2–10 kΩ) be placed on this pin to GND.
10. These are test signals for factory use only and must be pulled up (100 Ω–1 kΩ) to OV_{DD} for normal machine operation.
11. These pins must not be pulled down during power-on reset.
12. See *AN4232 MPC8569E PowerQUICC III Design Checklist* for the required PLL filters to be attached to the AV_{DD} pin.
13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. This pin selects the voltage of eLBC interface (BV_{DD}). This pin has internal weak pull down.
15. This pin selects the voltage of UCC1 and UCC3 interfaces ($LV_{DD}1$). This pin has internal weak pull down.
16. This pin selects the voltage of UCC2 and UCC4 interfaces ($LV_{DD}2$). This pin has internal weak pull down.
17. This pin requires a 100-Ω pull down to ground.
18. The value of LA[24:27] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See *AN4232 MPC8569E PowerQUICC III Design Checklist* for more details.
19. The value of QE_PE[27:29] during reset sets the DDR clock PLL settings. These pins require 4.7-kΩ pull up or pull down resistors. See *AN4232 MPC8569E PowerQUICC III Design Checklist* for more details.
20. The value of LALE, LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$ and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the *AN4232 MPC8569E PowerQUICC III Design Checklist* for more details.
21. The value of $\overline{\text{LCS}}$[3:7] at reset sets the QE PLL settings. These pins require 4.7-kΩ pull up or pull down resistors. See *AN4232 MPC8569E PowerQUICC III Design Checklist* for more details.
22. The value of QE_PB[27:28], QE_PC4 and QE_PD4 at reset sets the Boot ROM location. These pins require 4.7-kΩ pull up or pull down resistors. See the *MPC8569E PowerQUICC III Integrated Host Processor Family Reference Manual* for details
23. These pins are sampled at reset for general-purpose configuration use by software. The value of LAD[0:15] at reset sets the upper 16 bits of the GPPORCR
24. These pins must not be pulled up during power-on reset.
25. This output is actively driven during reset rather than being three-stated during reset.

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note

26. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
27. When operating in DDR2 mode, connect Dn_MDIC[0] to ground through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to GV_{DD} through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect Dn_MDIC[0] to ground through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to GV_{DD} through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
28. Recommend a pull-up resistor (1 kΩ) to be placed on this pin to OV_{DD}.
29. For systems which boot from local bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull up on LGPL4 is required.
30. If unused, these pins must be connected to GND.
31. If unused, these pins must be left unconnected.
32. These pins may be connected to a temperature diode monitoring device such as the On Semiconductor, NCT1008™. If a temperature diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8569E. This device is currently targeted to these specifications, some of which are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the DC ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic	Symbol	Range	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage	AV_{DD}_CORE AV_{DD}_DDR, AV_{DD}_LBIU, AV_{DD}_PLAT, AV_{DD}_QE, AV_{DD}_SRDS	–0.3 to 1.21	V	—
Core power supply for SerDes transceiver	ScoreVDD	–0.3 to 1.21	V	—
Pad power supply for SerDes transceiver	XV_{DD}	–0.3 to 1.21	V	—
DDR2 and DDR3 DRAM I/O voltage	GV_{DD}	–0.3 to 1.98 –0.3 to 1.65	V	2
QUICC Engine block Ethernet interface I/O voltage	$LV_{DD}1$	–0.3 to 3.63 –0.3 to 2.75	V	—

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Range	Unit	Notes
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}2$	–0.3 to 3.63 –0.3 to 2.75	V	—
Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Enhanced local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR2/DDR3 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 3
	DDR2/DDR3 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	—
	Ethernet signals	LV_{IN}	–0.3 to ($LV_{DD}n$ + 0.3)	V	3
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	3
	Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
	SerDes signals	XV_{IN}	–0.3 to (XV_{DD} + 0.3)	V	—
Storage junction temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. The –0.3 to 1.98 V range is for DDR2, and the –0.3 to 1.65 V range is for DDR3.
3. **Caution:** (B,M,L,O,X)V_{IN} must not exceed (B,G,L,O,X)V_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

2.1.1.1 Recommended Operating Conditions

The following table provides the recommended operating conditions for this device. Proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

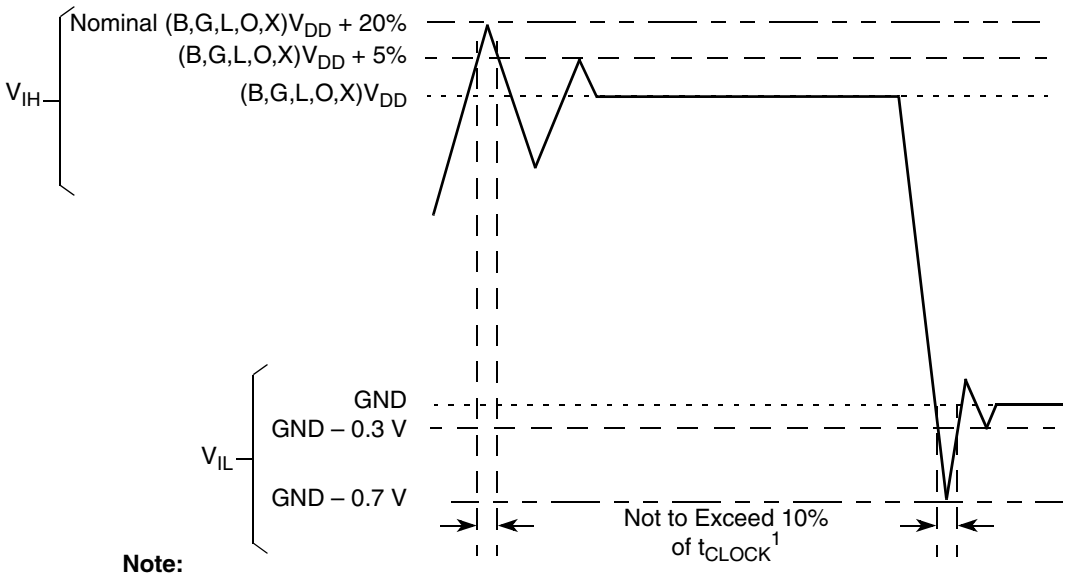
Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
PLL supply voltage	AV_{DD}_CORE, AV_{DD}_DDR, AV_{DD}_LBIU, AV_{DD}_PLAT, AV_{DD}_QE, AV_{DD}_SRDS	1.0 V ± 30 mV 1.1 V ± 33 mV	V	2

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Core power supply for SerDes transceiver		ScoreVDD	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
Pad power supply for SerDes transceiver		XV_{DD}	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
DDR2 and DDR3 DRAM I/O voltage		GV_{DD}	1.8 V ± 90 mV 1.5 V ± 75 mV	V	4
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}1$	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}2$	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Enhanced local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2 and DDR3 DRAM signals	MV_{IN}	GND to GV_{DD}	V	3
	DDR2 DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 2%	V	3
	DDR3 DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 1%	V	3
	Ethernet signals	LV_{IN}	GND to $LV_{DD}n$	V	3
	Enhanced local bus signals	BV_{IN}	GND to BV_{DD}	V	3
	Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage	OV_{IN}	GND to OV_{DD}	V	3
	SerDes signals	XV_{IN}	GND to XV_{DD}	V	—
Operating Temperature range	Commercial	T_A, T_J	T_A = 0 (min) to T_J = 105 (max)	°C	—

Notes:
1. A nominal voltage of 1.1 V is recommended for CPU speeds of 1.33 GHz and QUICC Engine block speeds of 667 MHz.
2. This voltage is the input to the filter and not the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
3. **Caution:** (B,M,L,O,X)V_{IN} must not exceed (B,G,L,O,X)V_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. The 1.8 V ± 90 mV range is for DDR2, and the 1.5 V ± 75 mV range is for DDR3.

The following figure shows the undershoot and overshoot voltages at the interfaces of the MPC8569E.



Note:

1. Note that t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references Dn_MCK.
   For eLBC, t_{CLOCK} references LCLKn
   For eLBC, t_{CLOCK} references LCLKn
   For SerDes XV_{DD}, t_{CLOCK} references SD_REF_CLK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/XV_{DD}$

The core voltage must always be provided at nominal 1.0 or 1.1 V. See Table 3 for actual recommended core voltage. Voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. $(B,M,L,O)V_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied D*n*_MVREF signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.1.2 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Enhanced local bus interface utilities signals	45 45 45	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	—
DDR2 signal	18 (full strength mode) 35 (half strength mode)	GV_{DD} = 1.8 V	1
DDR3 signal	20 (full strength mode) 40 (half strength mode)	GV_{DD} = 1.5 V	1
DUART, EPIC, I^2C, JTAG, system control	45	OV_{DD} = 3.3 V	—

Note:

1. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at T_J = 105°C and at GV_{DD} (min). Refer to the MPC8569 reference manual for the DDR impedance programming procedure through the DDR control driver register 1 (DDRCDR_1).

2.1.2 Power Sequencing

The MPC8569E requires its power rails to be applied in a specific sequence to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD}_n, BV_{DD}, $LV_{DD}n$, OV_{DD}, ScoreVDD, XV_{DD}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

NOTE

While V_{DD} is ramping, current may be supplied from V_{DD} through the MPC8569E to GV_{DD}. Nevertheless, GV_{DD} from an external supply should follow the sequencing described above.

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power up, and extra current may be drawn by the device.

2.1.3 RESET Initialization

This section describes the AC electrical specifications for the RESET timing requirements of the MPC8569E. The following table describes the specifications for the RESET initialization timing.

Table 5. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	10	—	SYSCLK	1, 2
Minimum assertion time of $\overline{\text{TRESET}}$ simultaneous to HRESET assertion	25	—	ns	3

Table 5. RESET Initialization Timing Specifications (continued)

Parameter	Min	Max	Unit	Notes
Maximum rise/fall time of $\overline{\text{HRESET}}$	—	1	SYSCLK	5
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLK	4
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	2	—	SYSCLK	—
Input setup time for POR configurations (other than PLL configuration) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLK	4
Input hold time for all POR configurations (including PLL configuration) with respect to negation of $\overline{\text{HRESET}}$	8	—	SYSCLK	4
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLK	4

Note:

1. There may be some extra current leakage when driving signals high during this time.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. For guidance on how this requirement can be met, refer to the JTAG signal termination guidelines in *AN4232 MPC8569E PowerQUICC III Design Checklist*.
4. SYSCLK is the primary clock input for the MPC8569E.
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following table provides the PLL lock times.

Table 6. PLL Lock Times

Parameter	Min	Max	Unit
Core PLL lock time	—	100	µs
Platform PLL lock time	—	100	µs
QUICC Engine block PLL lock time	—	100	µs
DDR PLL lock times	—	100	µs

2.1.4 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum Power-On Ramp Rate is required to avoid falsely triggering the ESD circuitry. The following table provides the power supply ramp rate specifications.

Table 7. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OVDD/CVDD/GVDD/BVDD/SVDD/LVDD, All VDD supplies, MVREF and all AVDD supplies.)	—	36000	V/s	1, 2

Note:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range may falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

2.2 Power Characteristics

The following table shows the power dissipations of the V_{DD} supply for various operating core complex bus clock (CCB_clk) frequencies versus the core, DDR data rate, and QUICC Engine block frequencies. Note that these numbers are based on design estimates only and are preliminary. More accurate power numbers are available after the measurement on the silicon is complete.

Table 8. MPC8569E Power Dissipation

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	DDR Data Rate Frequency (MHz)	QUICC Engine Block Frequency (MHz)	V_{DD} Core (V)	Junction Temperature (°C)	Power[5]	Notes
Typical	800	400	600	400	1.0	65	3.4 W	1, 2
Thermal						105	4.9 W	1, 3
Maximum							5.4 W	1, 4
Typical	1067	533	667	533	1.0	65	3.9 W	1, 2
Thermal						105	5.4 W	1, 3
Maximum							6.0 W	1, 4

Table 8. MPC8569E Power Dissipation (continued)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	DDR Data Rate Frequency (MHz)	QUICC Engine Block Frequency (MHz)	V_{DD} Core (V)	Junction Temperature (°C)	Power[5]	Notes
Typical	1333	533	800	667	1.1	65	5.7 W	1, 2
Thermal						105	7.9 W	1, 3
Maximum							8.6 W	1, 4

Note:

1. These values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured while running the Dhrystone benchmark, using the *nominal* process and *recommended* core voltage (V_{DD}) at 65 °C junction temperature (see Table 3).
3. Thermal power is the maximum power measured while running the Dhrystone benchmark, using the *worst case* process and *recommended* core voltage (V_{DD}) at maximum operating junction temperature (see Table 3).
4. Maximum power is the maximum power measured while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions that keeps the execution unit maximally busy and a typical workload on platform interfaces, using the *worst case* process and *nominal* core voltage (V_{DD}) at maximum operating junction temperature (see Table 3).
5. This table includes power numbers for the V_{DD}, AV_{DD}_n, and ScoreVDD rails.

2.3 Input Clocks

The following table provides the system clock (SYSCLK) DC specifications.

Table 9. SYSCLK DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	10.5	11.5	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DD})	I_{IN}	—	—	±50	μA	2

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

The following table provides the system clock (SYSCLK) AC timing specifications.

Table 10. SYSCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	66	—	133	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	15.15	ns	1, 2
SYSCLK duty cycle	t_{KHK}/ $t_{SYSCLK/DDRCLK}$	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at –56 dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.3.1 Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in below table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the MPC8569E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the MPC8569E is compatible with spread spectrum sources if the recommendations listed in the following table are observed.

Table 11. Spread Spectrum Clock Source Recommendations

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Notes:

1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 10.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION

The processor's minimum and maximum SYSCLK and core frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

2.3.2 Real Time Clock Timing

The real time clock timing (RTC) input is sampled by the core complex bus clock (CCB_clk). The output of the sampling latch is then used as an input to the counters of the PIC and the time base unit of the e500; there is no need for jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB_clk. That is, minimum clock high time is $2 \times t_{CCB\_clk}$, and minimum clock low time is $2 \times t_{CCB\_clk}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.3.3 Gigabit Ethernet Reference Clock Timing

The following table provides the gigabit Ethernet reference clock (TX_CLK) AC timing specifications.

Table 12. TX_CLK[3,4] AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 V ± 125 mV / 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
TX_CLK frequency	t_{G125}	—	125	—	MHz	—
TX_CLK cycle time	t_{G125}	—	8	—	ns	—
TX_CLK rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1, 5
TX_CLK duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2, 5
TX_CLK jitter	—	—	—	± 150	ps	2, 5

Notes:

1. Rise and fall times for TX_CLK are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V, and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. TX_CLK is used to generate the GTX clock for the UEC transmitter with 2% degradation. The TX_CLK duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the UEC GTX_CLK. See Section 2.6.3.7, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. Gigabit transmit 125-MHz source. This signal must be generated externally with a crystal or oscillator, or is sometimes provided by the PHY. TX_CLK is a 125-MHz input into the UCC Ethernet Controller and is used to generate all 125-MHz related signals and clocks in the following modes: GMII, TBI, RTBI, RGMII.
4. For GMII and TBI modes, TX_CLK is provided to UCC1 through QE_PC[8:11,14,15] (CLK9-12,15,16) and to UCC2 through QE_PC[2,3,6,7,15:17](CLK3,4,7,8,16:18). For RGMII and RTBI modes, TX_CLK is provided to UCC1 and UCC3 through QE_PC11(CLK12) and to UCC2 and UCC4 through QE_PC16 (CLK17).
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

2.3.4 Other Input Clocks

A description of the overall clocking of this device is available in the *MPC8569E PowerQUICC III Integrated Host Processor Family Reference Manual* in the form of a clock subsystem block diagram. For information about the input clock requirements of other functional blocks such as SerDes, Ethernet Management, eSDHC, and Enhanced Local Bus see the specific interface section.

2.4 DDR2 and DDR3 SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR2 and DDR3 SDRAM controller interface of the MPC8569E. Note that the required GV_{DD}(typ) is 1.8 V for DDR2 SDRAM and GV_{DD}(typ) is 1.5 V for DDR3 SDRAM.

2.4.1 DDR2 and DDR3 SDRAM Interface DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR2 SDRAM.

Table 13. DDR2 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.8 V[1]

Parameter	Symbol	Min	Max	Unit	Notes
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.125	—	V	5
Input low voltage	V_{IL}	—	MVREF*n* – 0.125	V	5
Output high current (V_{OUT} = 1.320 V)	I_{OH}	—	–13.4	mA	6, 7
Output low current (V_{OUT} = 0.380 V)	I_{OL}	13.4	—	mA	6, 7
I/O leakage current	I_{OZ}	–50	50	μA	8

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed the MVREF*n* DC level by more than ±2% of GV_{DD} (that is, ± 36 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must meet the specifications stated in Table 16.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. I_{OH} and I_{OL} are measured at GV_{DD} = 1.7 V.
7. Refer to the IBIS model for the complete output IV curve characteristics.
8. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

The following table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 14. DDR3 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.5 V[1]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4

Table 14. DDR3 SDRAM Interface DC Electrical Characteristics (continued)

At recommended operating condition with GV_{DD} = 1.5 V[1]

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	MVREF*n* + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed the MVREF*n* DC level by more than ±1% of GV_{DD} (that is, ± 15 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must meet the specifications stated in Table 16.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

The following table provides the DDR controller interface capacitance for DDR2 and DDR3.

Table 15. DDR2 and DDR3 SDRAM Capacitance

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3

Parameter	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1, 2

Note:

1. This parameter is sampled. GVDD = 1.8 V ± 0.1 V (for DDR2), f = 1 MHz, T_A = 25 °C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.
2. This parameter is sampled. GVDD = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25 °C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.175 V.

The following table provides the current draw characteristics for MVREF*n*.

Table 16. Current Draw Characteristics for MVREFn

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Current draw for DDR2 SDRAM for MVREF*n*	I_{MVREFn}	—	300	μA	—
Current draw for DDR3 SDRAM for MVREF*n*	I_{MVREFn}	—	250	μA	—

2.4.2 DDR2 and DDR3 SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that the required GV_{DD}(typ) voltage is 1.8 V or 1.5 V when interfacing to DDR2 or DDR3 SDRAM respectively.

2.4.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

The following table provides the input AC timing specifications for the DDR controller when interfacing to DDR2 SDRAM.

Table 17. DDR2 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	> 533 MHz data rate	V_{ILAC}	—	MVREF*n* – 0.20	V	—
	≤ 533 MHz data rate		—	MVREF*n* – 0.25		
AC input high voltage	> 533 MHz data rate	V_{IHAC}	MVREF*n* + 0.20	—	V	—
	≤ 533 MHz data rate		MVREF*n* + 0.25	—		

The following table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 18. DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	—	MVREF*n* – 0.175	V	—
AC input high voltage	V_{IHAC}	MVREF*n* + 0.175	—	V	—

The following table provides the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 19. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications[3]

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1
800 MHz data rate		–200	200		1
667 MHz data rate		–240	240		1
533 MHz data rate		–300	300		1
400 MHz data rate		–365	365		1

Table 19. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications[3] (continued)

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3

Parameter	Symbol	Min	Max	Unit	Note
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}	—	—	ps	2
800 MHz data rate		–425	425		2
667 MHz data rate		–510	510		2
533 MHz data rate		–635	635		2
400 MHz data rate		–885	885		2

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.
3. Parameters tested in DDR2 mode are to 400, 533, 667, and 800 MHz data rates and in DDR3 mode to 667 and 800 MHz data rates.

The following figure shows the DDR2 and DDR3 SDRAM interface input timing diagram.

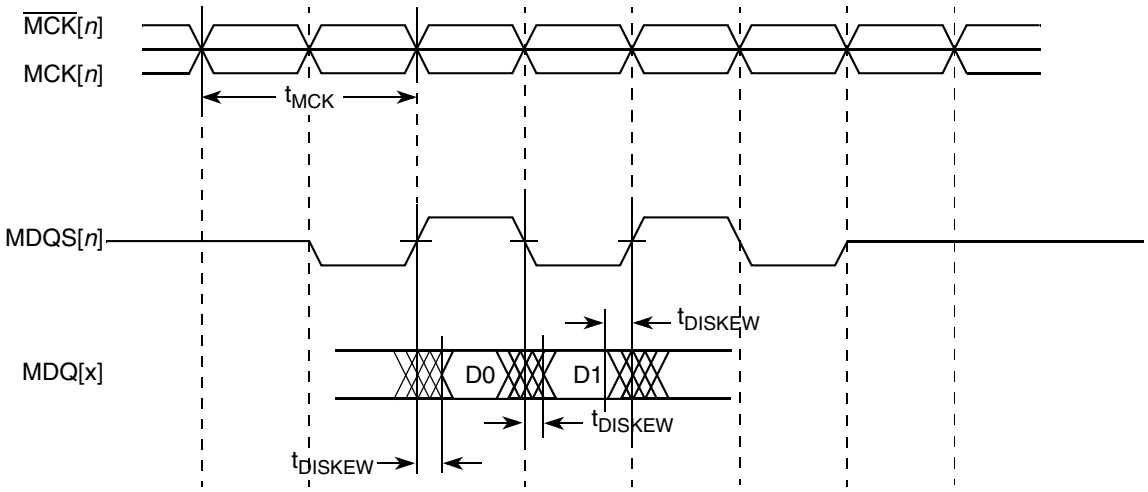


Figure 8. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

2.4.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

The following table contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 20. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications[6]

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[*n*] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
800 MHz		0.917[7] 0.88[8]	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
800 MHz		0.917[7] 0.88[8]	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
$\overline{\text{MCS}}$[*n*] output setup with respect to MCK	t_{DDKHCS}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
$\overline{\text{MCS}}$[*n*] output hold with respect to MCK	t_{DDKHCX}			ns	3
800 MHz		0.917	—		
667 MHz		1.10	—		
533 MHz		1.48	—		
400 MHz		1.95	—		
MCK to MDQS skew	t_{DDKHMH}			ns	4
800 MHz		–0.375	0.375		
≤ 667 MHz		–0.6	0.6		

Table 20. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications[6]

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
800 MHz		280[7] 320[8]	—		
667 MHz		400[7] 450[8]	—		
533 MHz		538	—		
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
800 MHz		280[7] 320[8]	—		
667 MHz		400[7] 450[8]	—		
533 MHz		538	—		
400 MHz		700	—		

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This will typically be set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8569E PowerQUICC III Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
6. Parameters tested in DDR2 mode are to 400, 533, 667, and 800 MHz data rate and in DDR3 mode to 667 and 800 MHz data rate.
7. DDR3 only
8. DDR2 only

NOTE

For the ADDR/CMD setup and hold specifications in Table 20, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

The following figure shows the DDR2 and DDR3 SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

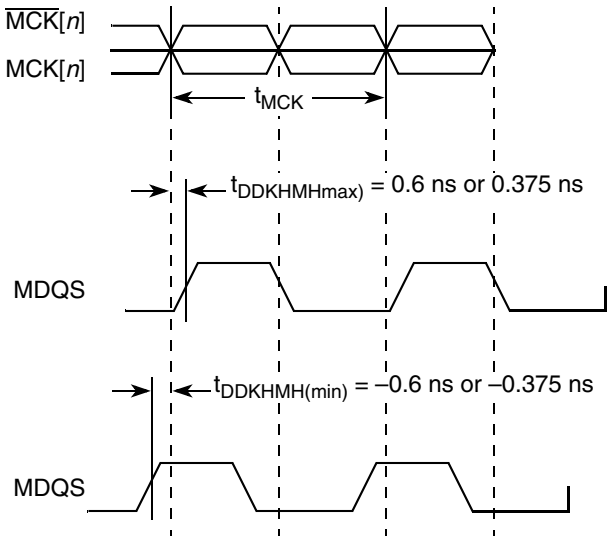


Figure 9. Timing Diagram for t_{DDKHMH}

The following figure shows the DDR2 and DDR3 SDRAM output timing diagram.

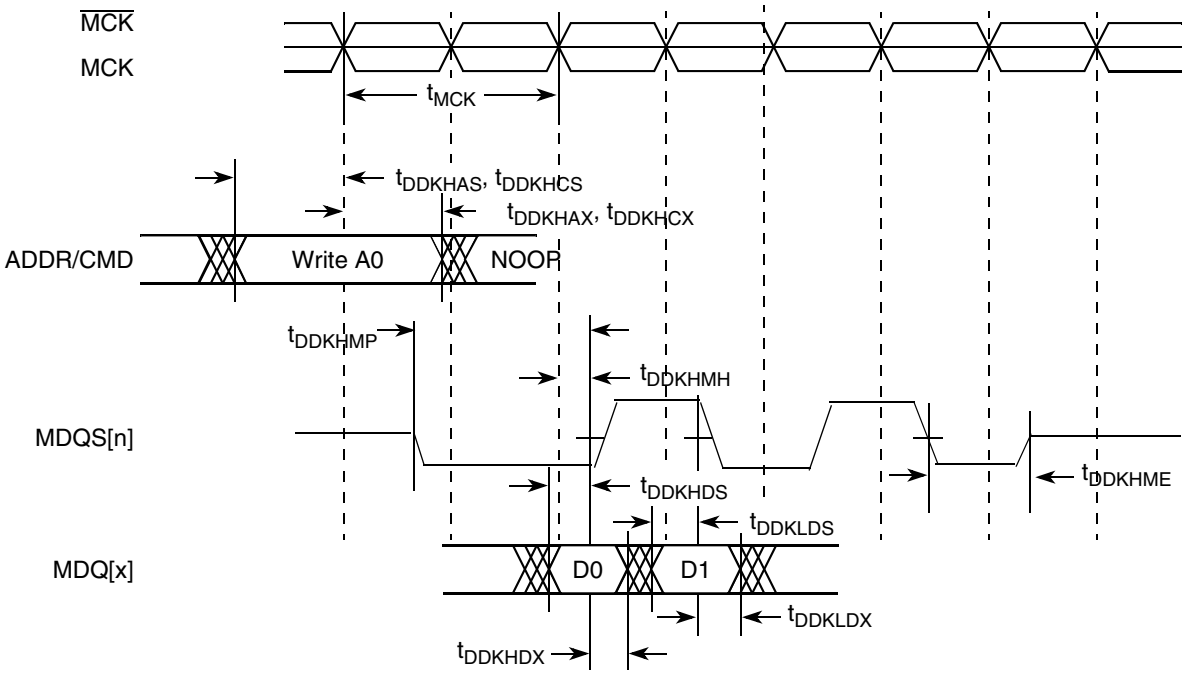


Figure 10. DDR2 and DDR3 Output Timing Diagram

The following figure provides the AC test load for the DDR2 and DDR3 controller bus.

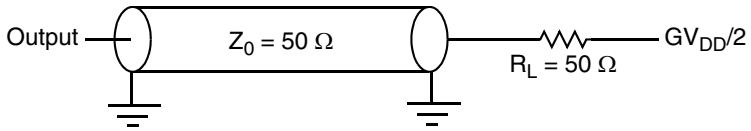


Figure 11. DDR2 and DDR3 Controller Bus AC Test Load

2.5 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8569E.

2.5.1 DUART DC Electrical Characteristics

The following table provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.5.2 DUART AC Electrical Specifications

The following table provides the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB}/1,048,576	baud	1
Maximum baud rate	f_{CCB}/16	baud	1, 2
Oversample rate	16	—	3

Notes:

1. f_{CCB} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

2.6 Ethernet Interface

This section provides the AC and DC electrical characteristics for the Ethernet interfaces inside the QUICC Engine block.

2.6.1 GMII/SGMII/MII/SMII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), serial gigabit media independent interface (SGMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces are defined for 3.3 V. The GMII, MII, and TBI interface timing is compatible with IEEE Std 802.3™. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000)*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2 (3/20/1998)*. The electrical characteristics for the SGMII is specified in Section 2.6.4, "SGMII Interface Electrical Characteristics." The electrical characteristics for MDIO and MDC are specified in Section 2.7, "Ethernet Management Interface."

2.6.2 GMII, MII, RMII, SMII, TBI, RGMII and RTBI DC Electrical Characteristics

The following table shows the GMII, MII, RMII, SMII, and TBI DC electrical characteristics when operating from a 3.3 V supply.

Table 23. GMII, MII, RMII, SMII, and TBI DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	40	μA	2
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –4.0 mA)	V_{OH}	2.1	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

The following table shows the RGMII, and RTBI DC electrical characteristics when operating from a 2.5 V supply.

Table 24. RGMII and RTBI DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	10	μA	1

Table 24. RGMII and RTBI DC Electrical Characteristics (continued)

At recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	1, 2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.
2. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.

2.6.3 GMII, MII, RMII, SMII, TBI, RGMII, and RTBI AC Timing Specifications

This section describes the AC timing specifications for GMII, MII, RMII, SMII, TBI, RGMII, and RTBI.

2.6.3.1 GMII Timing Specifications

This section describe the GMII transmit and receive AC timing specifications.

2.6.3.1.1 GMII Transmit AC Timing Specifications

The following table provides the GMII transmit AC timing specifications.

Table 25. GMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
GTX_CLK clock period	t_{GTX}	7.5	—	8.5	ns	—
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	—	ns	—
GTX_CLK data clock rise time (20%–80%)	t_{GTXR}	—	1.0	—	ns	—
GTX_CLK data clock fall time (80%–20%)	t_{GTXF}	—	1.0	—	ns	—

The following figure shows the GMII transmit AC timing diagram.

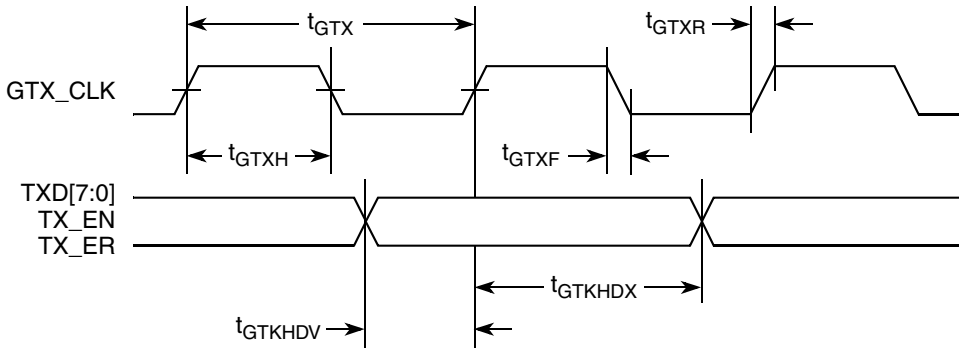


Figure 12. GMII Transmit AC Timing Diagram

2.6.3.1.2 GMII Receive AC Timing Specifications

The following table provides the GMII receive AC timing specifications.

Table 26. GMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period	t_{GRX}	7.5	—	—	ns	1
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	65	%	2
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.2	—	—	ns	—
RX_CLK clock rise time (20%–80%)	t_{GRXR}	—	—	1.0	ns	2
RX_CLK clock fall time (80%–20%)	t_{GRXF}	—	—	1.0	ns	2

Note:
1. The frequency of RX_CLK should not exceed frequency of gigabit Ethernet reference clock by more than 300 ppm
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

The following figure provides the GMII AC test load.

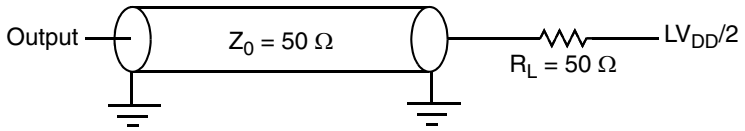


Figure 13. GMII AC Test Load

The following figure shows the GMII receive AC timing diagram.

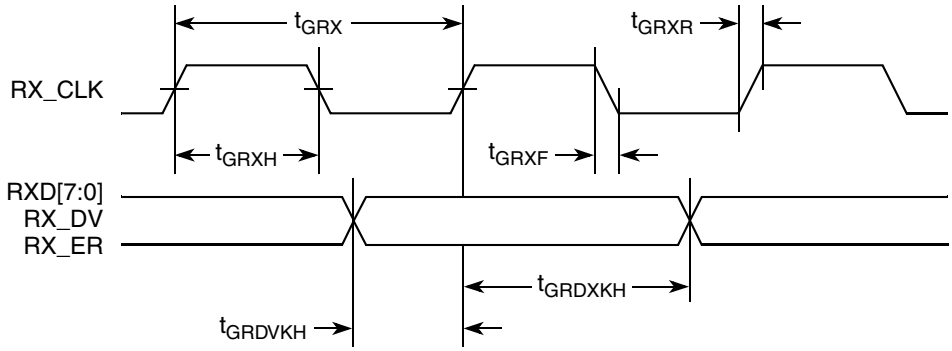


Figure 14. GMII Receive AC Timing Diagram

2.6.3.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

2.6.3.2.1 MII Transmit AC Timing Specifications

The following table provides the MII transmit AC timing specifications.

Table 27. MII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
TX_CLK clock period 10 Mbps	t_{MTX}	399.96	400	400.04	ns	—
TX_CLK clock period 100 Mbps	t_{MTX}	39.996	40	40.004	ns	—
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%	—
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	0	—	25	ns	—
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns	—
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns	—

The following figure shows the MII transmit AC timing diagram.

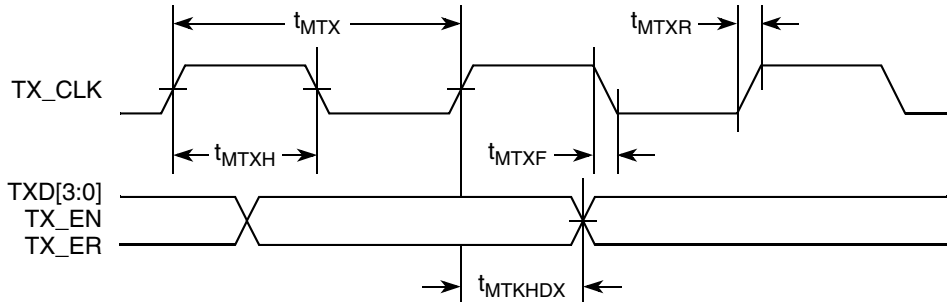


Figure 15. MII Transmit AC Timing Diagram

2.6.3.2.2 MII Receive AC Timing Specifications

The following table provides the MII receive AC timing specifications.

Table 28. MII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period 10 Mbps	t_{MRX}	399.96	400	400.04	ns	1
RX_CLK clock period 100 Mbps	t_{MRX}	39.996	40	40.004	ns	1
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%	2
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns	
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns	
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns	2
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns	2

Note:

1. The frequency of RX_CLK should not exceed the frequency of TX_CLK by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure provides the MII AC test load.

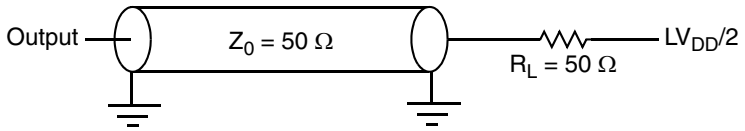


Figure 16. MII AC Test Load

The following figure shows the MII receive AC timing diagram.

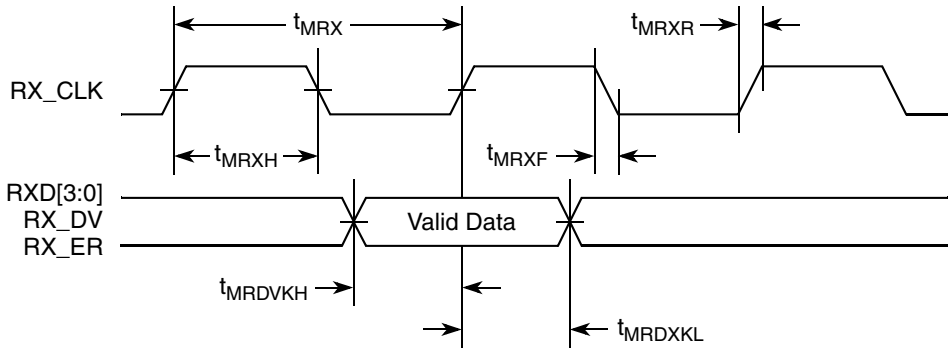


Figure 17. MII Receive AC Timing Diagram

2.6.3.3 SMII AC Timing Specification

The following table shows the SMII timing specifications.

Table 29. SMII Mode Signal Timing

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge setup time	t_{SMDVKH}	1.5	—	ns	—
ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	t_{SMDXKH}	1.0	—	ns	—
ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay	t_{SMXR}	1.5	5.5	ns	—

The following figure shows the SMII mode signal timing.

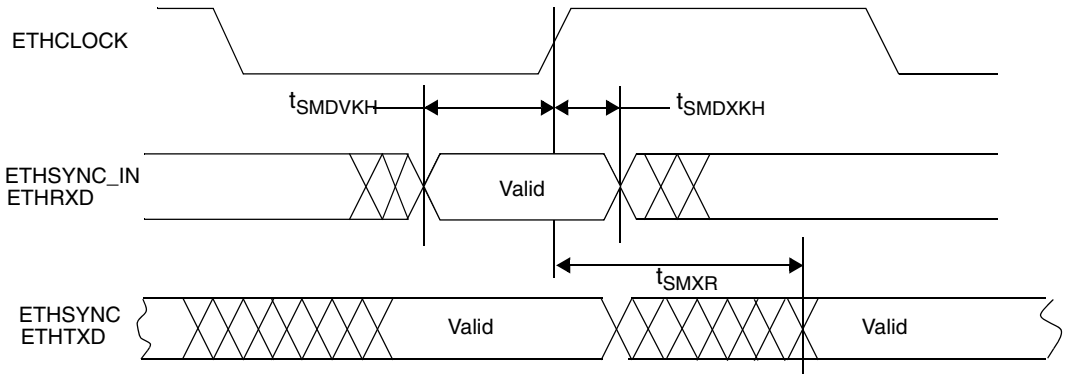


Figure 18. SMII Mode Signal Timing

2.6.3.4 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

2.6.3.4.1 RMII Transmit AC Timing Specifications

The following table shows the RMII transmit AC timing specifications.

Table 30. RMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
REF_CLK clock period	t_{RMT}	—	20.0	—	ns	—
REF_CLK duty cycle	t_{RMTH}	35	—	65	%	—
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps	—
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	4.0	ns	—
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	4.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns	—

The following figure shows the RMII transmit AC timing diagram.

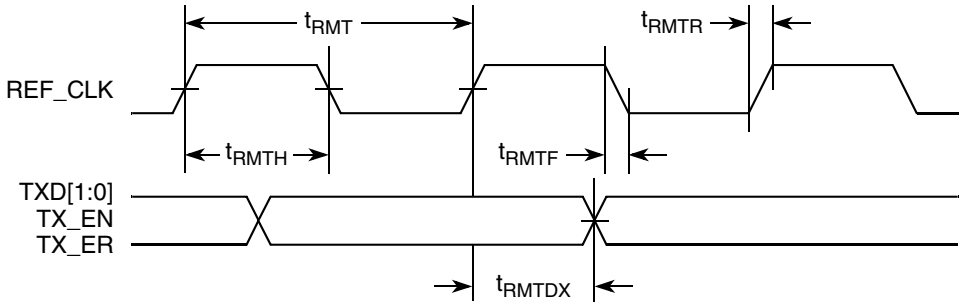


Figure 19. RMII Transmit AC Timing Diagram

2.6.3.4.2 RMII Receive AC Timing Specifications

The following table provides the RMII receive AC timing specifications.

Table 31. RMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
REF_CLK clock period	t_{RMR}	—	20.0	—	ns	—
REF_CLK duty cycle	t_{RMRH}	35	—	65	%	1
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps	1
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	4.0	ns	1

Table 31. RMII Receive AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	4.0	ns	1
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	—	—	ns	—
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	—	—	ns	—

Note:

1. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure provides the AC test load.

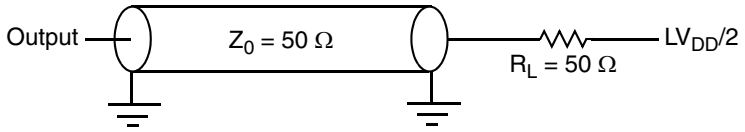


Figure 20. AC Test Load

The following figure shows the RMII receive AC timing diagram.

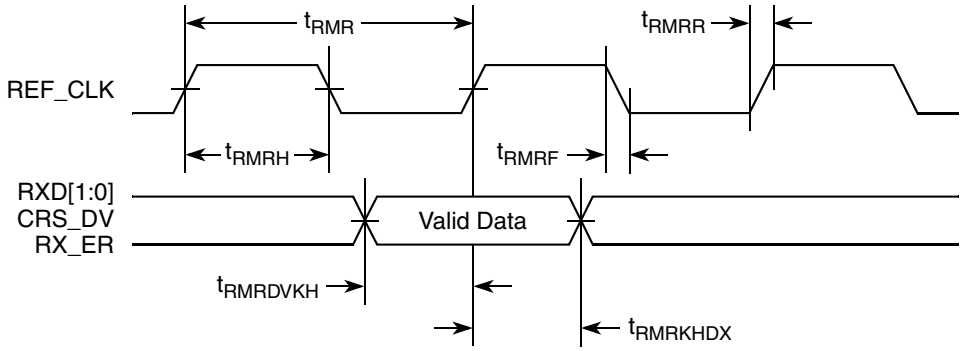


Figure 21. RMII Receive AC Timing Diagram

2.6.3.5 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

2.6.3.5.1 TBI Transmit AC Timing Specifications

The following table provides the TBI transmit AC timing specifications.

Table 32. TBI Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns	—
GTX_CLK to TCG[9:0] delay time	t_{TTKHDX}	1.0	—	—	ns	1
GTX_CLK rise (20%–80%)	t_{TTXZ}	0.7	—	—	ns	—
GTX_CLK fall time (80%–20%)	t_{TTXF}	0.7	—	—	ns	—

Note:

1. Data valid t_{TTKHDV} to GTX_CLK minimum setup time is a function of clock and maximum hold time (min setup = cycle time – max delay).

The following figure shows the TBI transmit AC timing diagram.

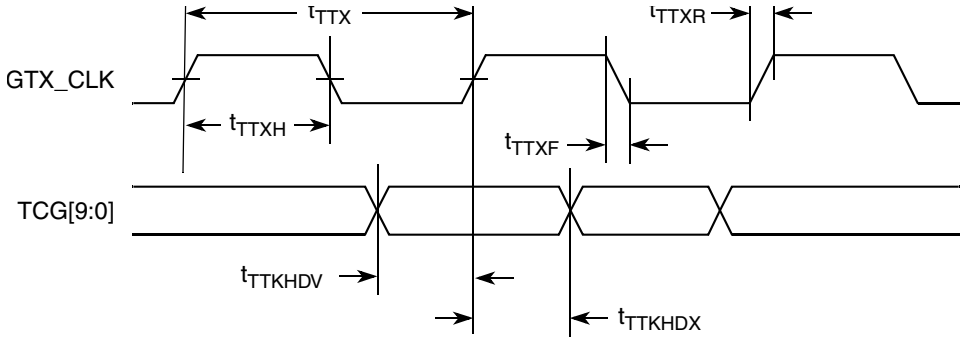


Figure 22. TBI Transmit AC Timing Diagram

2.6.3.5.2 TBI Receive AC Timing Specifications

The following table provides the TBI receive AC timing specifications.

Table 33. TBI Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
PMA_RX_CLK[0:1] clock period	t_{TRX}	—	16.0	—	ns	1
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns	—
PMA_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%	2
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns	—

Table 33. TBI Receive AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	—	—	ns	—
PMA_RX_CLK[0:1] clock rise time (20%–80%)	t_{TRXR}	0.7	—	2.4	ns	2
PMA_RX_CLK[0:1] clock fall time (80%–20%)	t_{TRXF}	0.7	—	2.4	ns	2

Note:

1. The frequency of RX_CLK should not exceed the frequency of gigabit Ethernet reference clock by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure provides the AC test load.

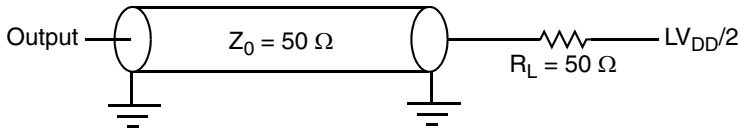


Figure 23. AC Test Load

The following figure shows the TBI receive AC timing diagram.

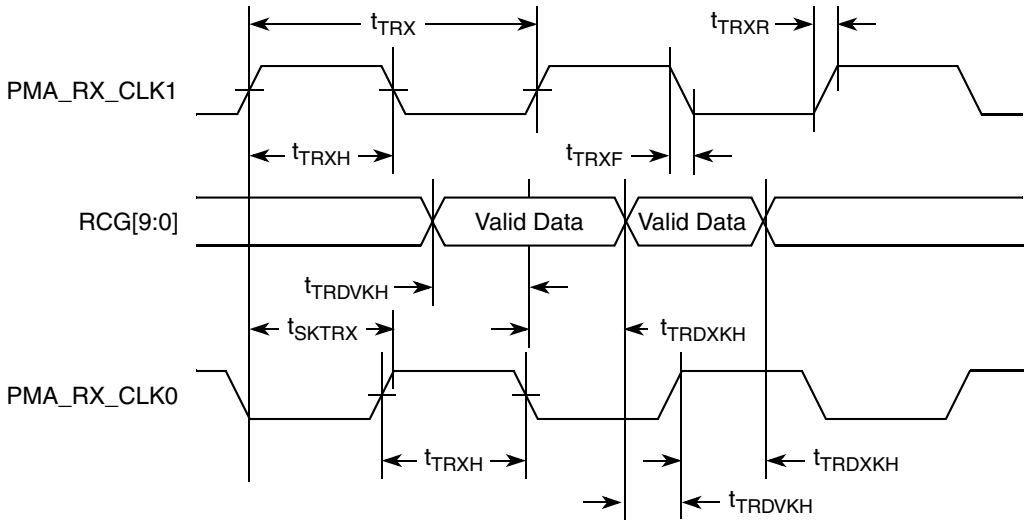


Figure 24. TBI Receive AC Timing Diagram

2.6.3.6 TBI Single-Clock Mode AC Specifications

The following table shows the TBI single-clock mode receive AC timing specifications.

Table 34. TBI Single-Clock Mode Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns	1
RX_CLK duty cycle	t_{TRRH}	40	50	60	%	2
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps	2
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	—	ns	2
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	—	ns	2
RCG[9:0] setup time to RX_CLK rising edge	t_{TRRDV}	2.0	—	—	ns	—
RCG[9:0] hold time to RX_CLK rising edge	t_{TRRDX}	1.0	—	—	ns	—

Note:

1. The frequency of RX_CLK should not exceed the frequency of gigabit Ethernet reference clock by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure shows the TBI single-clock mode receive AC timing diagram.

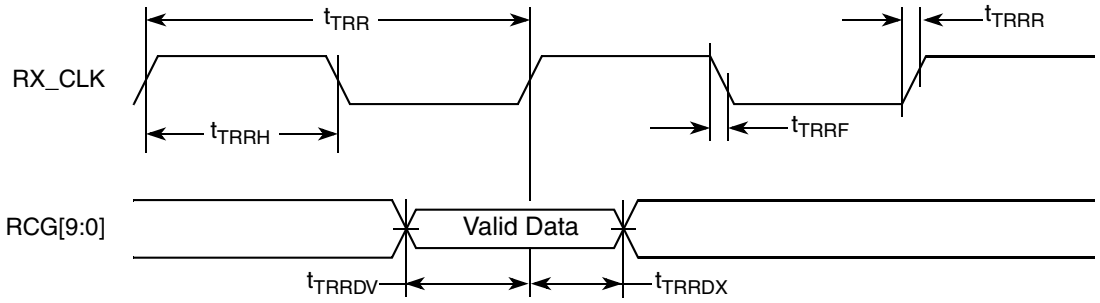


Figure 25. TBI Single-Clock Mode Receive AC Timing Diagram

2.6.3.7 RGMII and RTBI AC Timing Specifications

The following table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.2	—	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4, 6

Table 35. RGMII and RTBI AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	6
Rise time (20%–80%)	t_{RGTR}	—	—	1.75	ns	6
Fall time (20%–80%)	t_{RGTF}	—	—	1.75	ns	6

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of gigabit ethernet reference clock by more than 300 ppm.
6. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

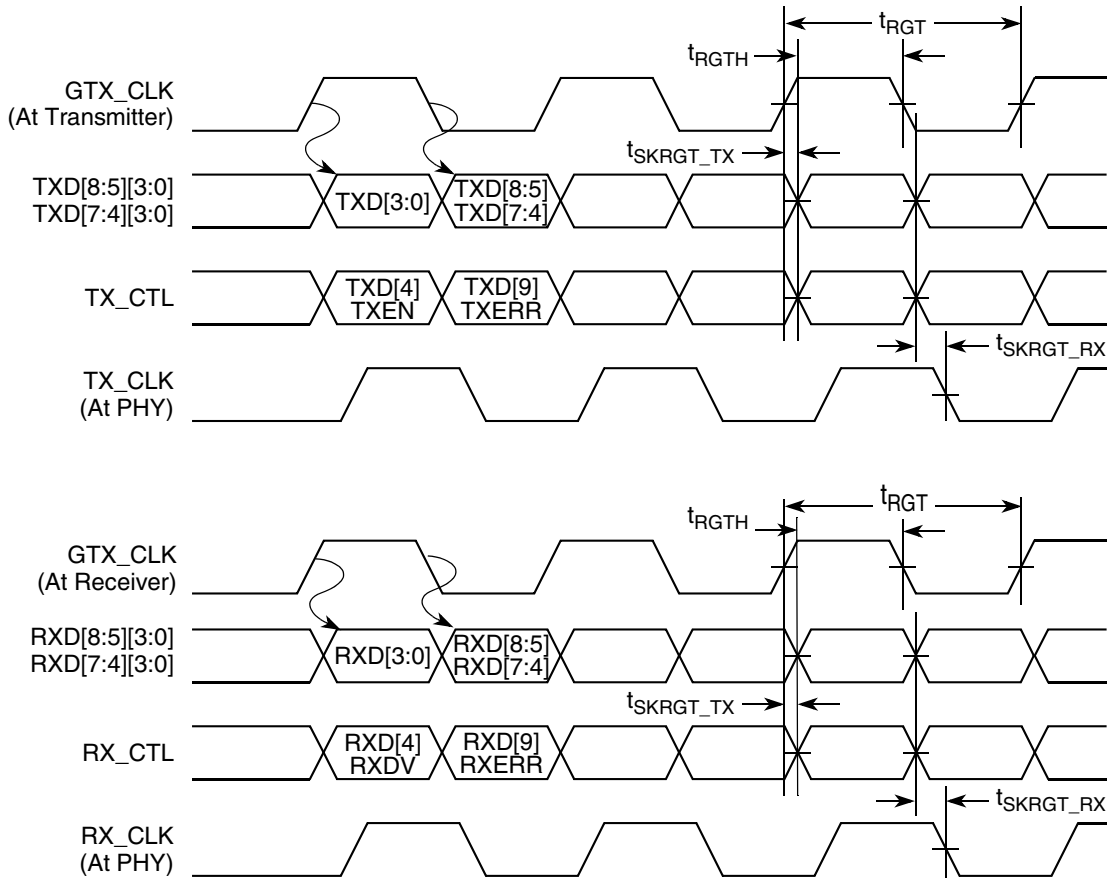


Figure 26. RGMII and RTBI AC Timing and Multiplexing Diagrams

2.6.4 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of MPC8569E as shown in Figure 27, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to GND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 45.

2.6.4.1 SGMII DC Electrical Characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.6.4.1.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 2.9.2.3, “DC Level Requirement for SerDes Reference Clocks.”

2.6.4.1.2 SGMII Transmit DC Timing Specifications

Table 36 and Table 37 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs, SD_TX[*n*] and $\overline{\text{SD\_TX}}$[*n*], as shown in Figure 28.

Table 36. SGMII DC Transmitter Electrical Characteristics

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	$XV_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$	mV	1
Output low voltage	V_{OL}	$XV_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$	—	—	mV	1
Output differential voltage[2, 3, 4] ($XV_{DD\text{-}Typ}$ at 1.0 V)	$\lvert V_{OD}\rvert$	320.0	500.0	725.0	mV	Equalization setting: 1.0×
		293.8	459.0	665.6		Equalization setting: 1.09×
		266.9	417.0	604.7		Equalization setting: 1.2×
		240.6	376.0	545.2		Equalization setting: 1.33×
		213.1	333.0	482.9		Equalization setting: 1.5×
		186.9	292.0	423.4		Equalization setting: 1.71×
		160.0	250.0	362.5		Equalization setting: 2.0×

Table 36. SGMII DC Transmitter Electrical Characteristics (continued)

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage[2, 3, 4] (XV_{DD-Typ} at 1.1 V)	$\|V_{OD}\|$	352.0	550.0	797.5	mV	Equalization setting: 1.0×
		323.1	504.9	732.1		Equalization setting: 1.09×
		293.6	458.7	665.1		Equalization setting: 1.2×
		264.7	413.6	599.7		Equalization setting: 1.33×
		234.4	366.3	531.1		Equalization setting: 1.5×
		205.6	321.2	465.7		Equalization setting: 1.71×
		176.0	275.0	398.8		Equalization setting: 2.0×
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Notes:

1. This does I not align to DC-coupled SGMII.
2. $|V_{OD}| = |V_{SD\_TXn} - V_{\overline{SD\_TXn}}|$. $|V_{OD}|$ is also referred as output differential peak voltage. $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.
3. The $|V_{OD}|$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**AB** (for SerDes lanes 0 & 1) or XMITEQ**EF** (for SerDes lanes 2 & 3) bit field of the MPC8569E SerDes control register:
   - The MSB (bit 0) of the above bit field is set to zero (selecting the full $V_{DD-DIFF-p-p}$ amplitude—power up default);
   - The LSB (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. The $|V_{OD}|$ value shown in the Typ column is based on the condition of XV_{DD-Typ} = 1.0V and 1.1 V, no common mode offset variation, SerDes transmitter is terminated with 100-Ω differential load between SD_TX[*n*] and $\overline{SD\_TX}$[*n*].

The following figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

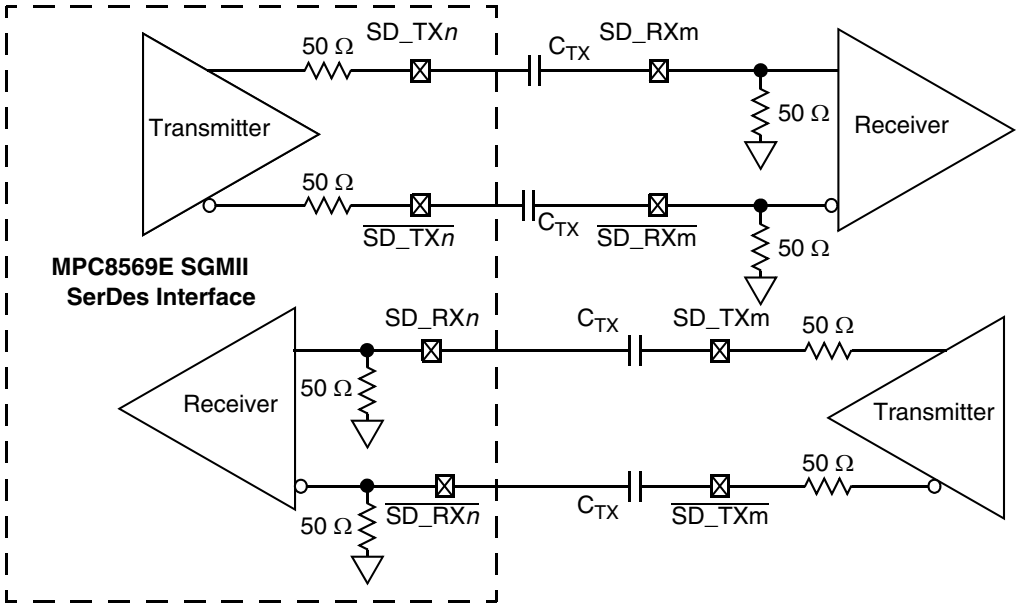


Figure 27. 4-Wire AC-Coupled SGMII Serial Link Connection Example

The following figure shows the SGMII transmitter DC measurement circuit.

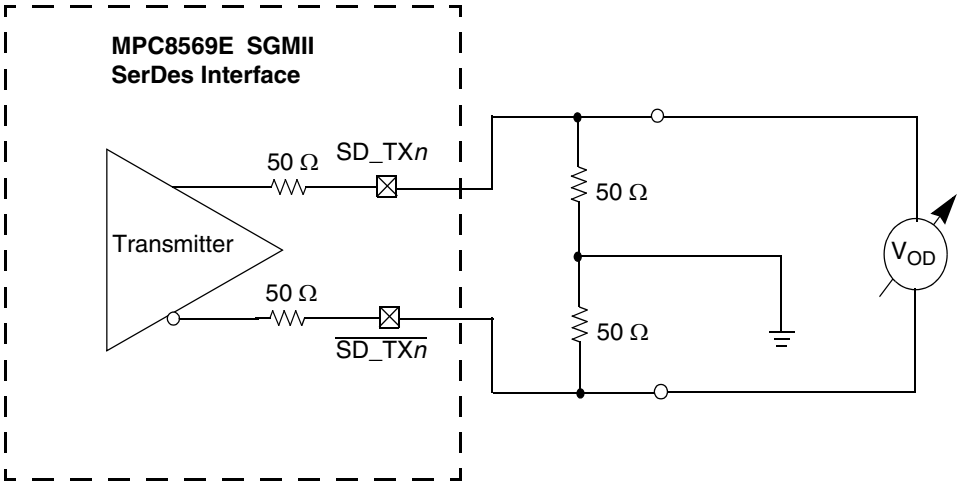


Figure 28. SGMII Transmitter DC Measurement Circuit

2.6.4.1.3 SGMII DC Receiver Electrical Characteristics

The following table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 37. SGMII DC Receiver Electrical Characteristics

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC Input voltage range		—	N/A			—	1
Input differential voltage	LSTS = 001	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	LSTS = 100		175	—			
Loss of signal threshold	LSTS = 001	V_{LOS}	30	—	100	mV	3, 4
	LSTS = 100		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—

Notes:

1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See Section 2.10.2, "PCI Express DC Physical Layer Specifications," and Section 2.10.3, "PCI Express AC Physical Layer Specifications," for further explanation.
4. The LSTS shown in this table refers to the LSTS**2** or LSTS**3** bit field of the MPC8569E's SerDes control register SRDSCR4.

2.6.4.2 SGMII AC Timing Specifications

This section discusses the AC timing specifications for the SGMII interface.

2.6.4.2.1 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Note that the SGMII clock requirements for SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are intended to be used within the clocking guidelines specified by Section 2.9.2.4, "AC Requirements for SerDes Reference Clocks."

2.6.4.2.2 SGMII Transmit AC Timing Specifications

The following table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 38. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	2
Unit interval	UI	799.92	800	800.08	ps	1
AC coupling capacitor	C_{TX}	10	—	200	nF	3

Notes:
1. Each UI is 800 ps ± 100 ppm.
2. See Figure 30 for single frequency sinusoidal jitter limits.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.6.4.2.3 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or at the receiver inputs (SD_RX*n* and $\overline{\text{SD\_RX}n}$), as depicted in the following figure, respectively.

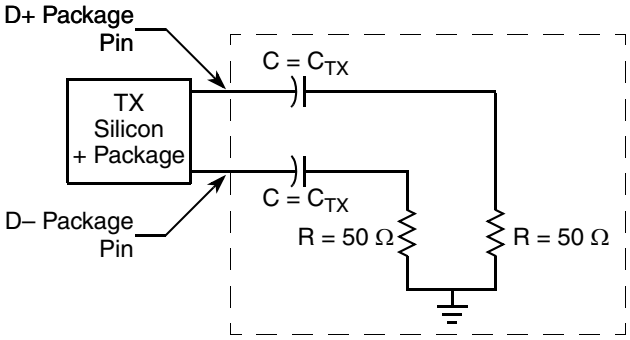


Figure 29. SGMII AC Test/Measurement Load

2.6.4.2.4 SGMII Receiver AC Timing Specifications

The following table provides the SGMII receive AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 39. SGMII Receive AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1, 2, 4
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1, 2, 4
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1, 2, 4
Bit Error Ratio	BER	—	—	10^{-12}	—	—
Unit Interval	UI	799.92	800.00	800.08	ps	3

Notes:
1. Measured at receiver.
2. See *RapidIO 1x/4x LP Serial Physical Layer Specification* for interpretation of jitter specifications.
3. Each UI is 800 ps ± 100 ppm.
4. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of the following figure.

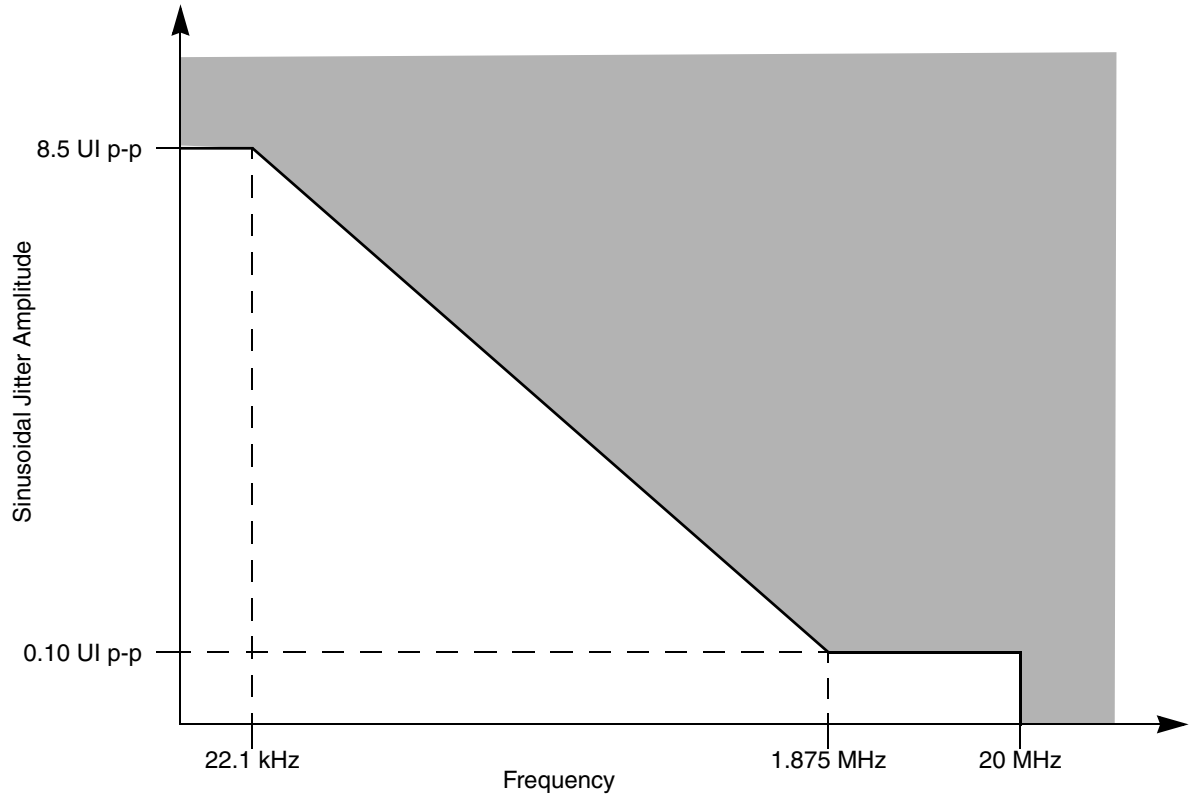


Figure 30. Single Frequency Sinusoidal Jitter Limits

2.6.5 QUICC Engine Block IEEE 1588 Electrical Characteristics

2.6.5.1 QUICC Engine Block IEEE 1588 DC Specifications

The following table shows the QUICC Engine block IEEE 1588 DC specifications when operating from a 3.3 V supply.

Table 40. QUICC Engine Block IEEE 1588 DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = OV_{DD})	I_{IH}	—	40	μA	2
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –4.0 mA)	V_{OH}	2.1	OV_{DD} + 0.3	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbols referenced in Table 2 and Table 3.

2.6.5.2 QUICC Engine Block IEEE 1588 AC Specifications

The following table provides the QUICC Engine block IEEE 1588 AC timing specifications.

Table 41. QUICC Engine Block IEEE 1588 AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
QE_1588_CLK clock period	$t_{T1588CLK}$	3.8	—	$T_{RX\_CLK} \times 7$	ns	1, 3
QE_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	5
QE_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	5
Rise time QE_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	5
Fall time QE_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	5
QE_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
QE_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}/t_{T1588CLKOUT}$	30	50	70	%	—
QE_1588_PPS_OUT	$t_{T1588OV}$	0.5	—	4.0	ns	—

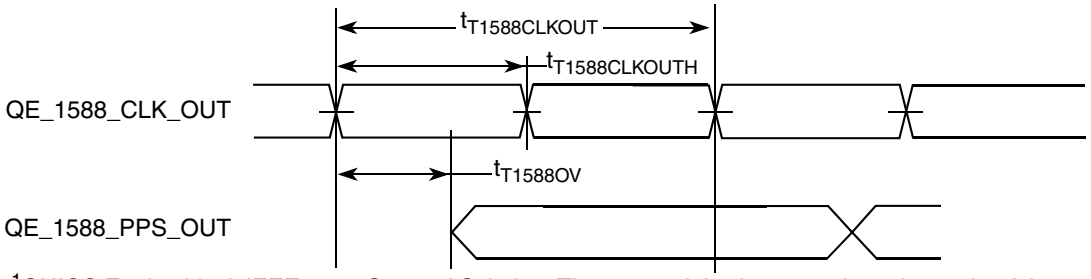
Table 41. QUICC Engine Block IEEE 1588 AC Timing Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
QE_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	2
QE_PTP_SOF_TX_IN pulse width	$t_{T1588TRIGH}$	$T_{TX\_CLK} \times 2$	—	—	ns	4
QE_PTP_SOF_RX_IN pulse width	$t_{T1588TRIGH}$	$T_{RX\_CLK} \times 2$	—	—	ns	4

Notes:

1. T_{RX_CLK} is the max clock period of the QUICC Engine block's receiving clock selected by TMR_CTRL[CKSEL]. See the *QUICC Engine Block with Protocol Interworking Reference Manual,* for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *QUICC Engine Block with Protocol Interworking Reference Manual,* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of t_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ are 2800, 280, and 56 ns, respectively.
4. The minimum value of $t_{TX/RXCLK}$ is defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the value of $t_{TX/RXCLK}$ are 800, 80, and 16 ns, respectively.
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure shows the data and command output AC timing diagram.



[1]QUICC Engine block IEEE 1588 Output AC timing: The output delay is counted starting at the rising edge if $t_{T11588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 31. QUICC Engine Block IEEE 1588 Output AC Timing

The following figure shows the data and command input AC timing diagram.

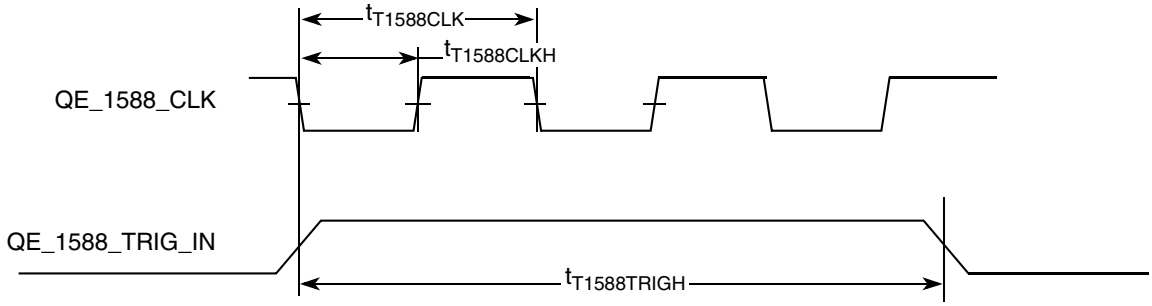


Figure 32. QUICC Engine Block IEEE 1588 Input AC Timing

The following figure shows the data and command input AC timing diagram.

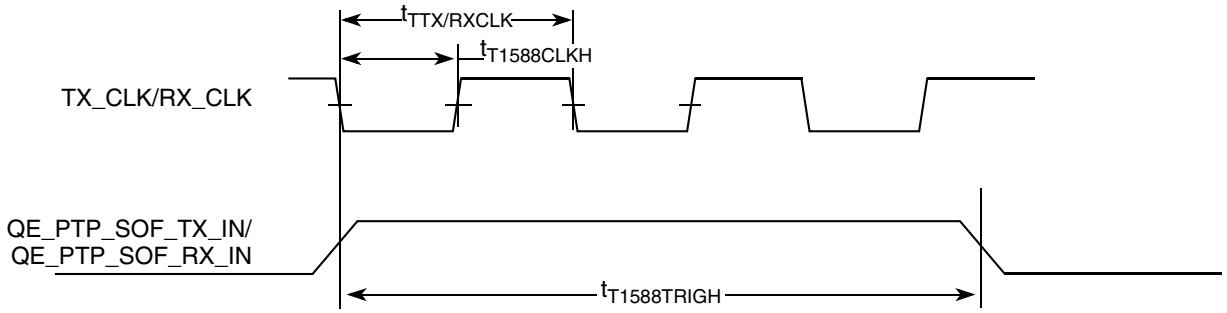


Figure 33. QUICC Engine Block IEEE 1588 Input AC Timing (SOF TRIG)

2.7 Ethernet Management Interface

The electrical characteristics specified in this section apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI, and RTBI are specified in Section 2.6, "Ethernet Interface."

2.7.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The following table provides the DC electrical characteristics for MDIO and MDC.

Table 42. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	—	0.4	V	—

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.

2.7.1.1 MII Management AC Electrical Specifications

The following table provides the MII management AC timing specifications.

Table 43. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} = 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO valid	t_{MDKHDV}	$2\times(t_{plb\_clk}*8)$	—	—	ns	4
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb\_clk}) - 3$	—	$(16 \times t_{plb\_clk}) + 3$	ns	3, 4, 5
MDIO to MDC setup time	t_{MDDVKH}	10	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDCF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the Mgmt Clock CE_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. t_{plb_clk} is the QUICC Engine block clock/2.
5. MDC to MDIO Data valid t_{MDKHDV} is a function of clock period and max delay time (t_{MDKHDX}).
(Min setup = cycle time – max delay

The following figure shows the MII management AC timing diagram.

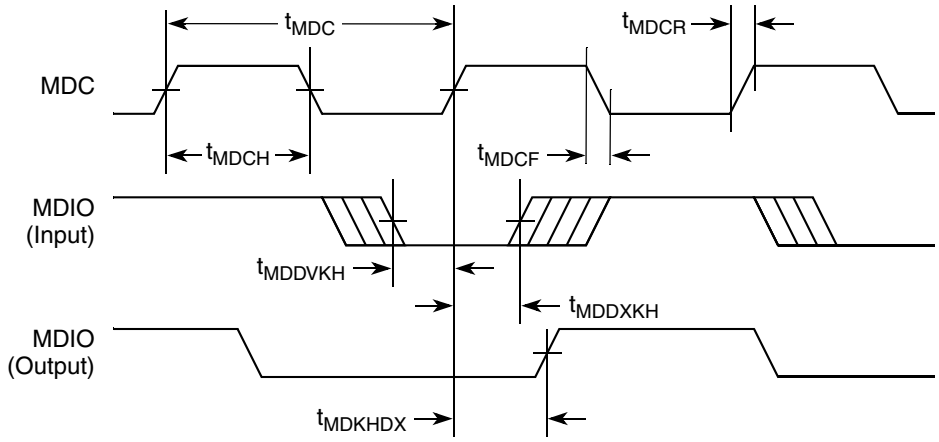


Figure 34. MII Management Interface Timing Diagram

2.8 HDLC, BISYNC, Transparent, and Synchronous UART Interfaces

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART interfaces of the MPC8569E.

2.8.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

The following table provides the DC electrical characteristics for the HDLC, BISYNC, Transparent, and synchronous UART interfaces.

Table 44. HDLC, BISYNC, and Transparent DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.8.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

The following table provides the input and output AC timing specifications for the HDLC, BISYNC, and Transparent protocols.

Table 45. HDLC, BISYNC, and Transparent AC Timing Specifications

For recommended operating conditions, see Table 3

Characteristic	Symbol[1]	Min	Max	Unit	Notes
Outputs—Internal clock delay	t_{HIKHOV}	0	5.5	ns	2
Outputs—External clock delay	t_{HEKHOV}	1	8.4	ns	2
Outputs—Internal clock high Impedance	t_{HIKHOX}	0	5.5	ns	2
Outputs—External clock high Impedance	t_{HEKHOX}	1	8	ns	2
Inputs—Internal clock input setup time	t_{HIIVKH}	6	—	ns	—

Table 45. HDLC, BISYNC, and Transparent AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Characteristic	Symbol[1]	Min	Max	Unit	Notes
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns	—
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns	—
Inputs—External clock input hold time	t_{HEIXKH}	1.3	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following table provides the input and output AC timing specifications for the synchronous UART protocols.

Table 46. Synchronous UART AC Timing Specifications

For recommended operating conditions, see Table 3

Characteristic	Symbol[1]	Min	Max	Unit	Notes
Outputs—Internal clock delay	t_{HIKHOV}	0	11	ns	2
Outputs—External clock delay	t_{HEKHOV}	1	14	ns	2
Outputs—Internal clock high Impedance	t_{HIKHOX}	0	11	ns	2
Outputs—External clock high Impedance	t_{HEKHOX}	1	14	ns	2
Inputs—Internal clock input setup time	t_{HIIVKH}	10	—	ns	—
Inputs—External clock input setup time	t_{HEIVKH}	8	—	ns	—
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns	—
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following figure provides the AC test load.

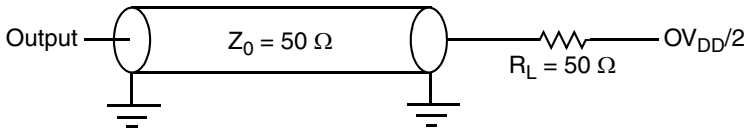
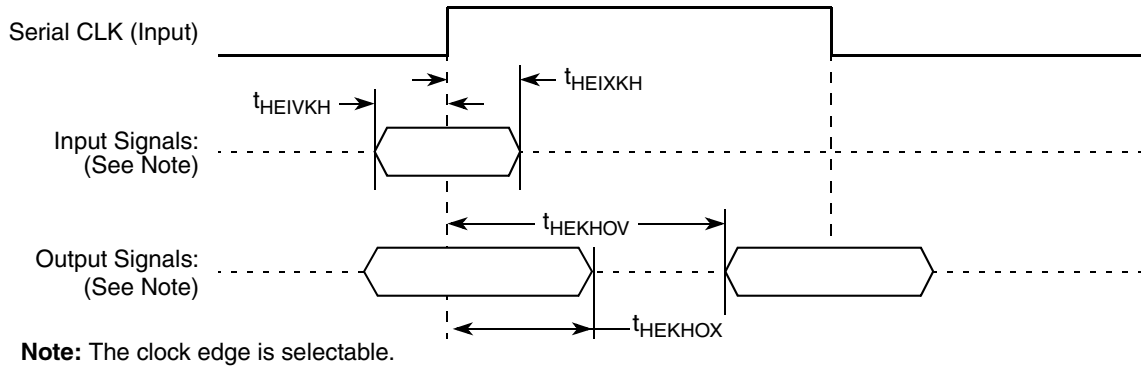


Figure 35. AC Test Load

Figure 36 and Figure 37 represent the AC timing from Table 45 and Table 46. Note that although the specifications generally refer to the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Also note that the clock edge is selectable.

The following figure shows the timing with external clock.



Note: The clock edge is selectable.

Figure 36. AC Timing (External Clock) Diagram

The following figure shows the timing with internal clock.

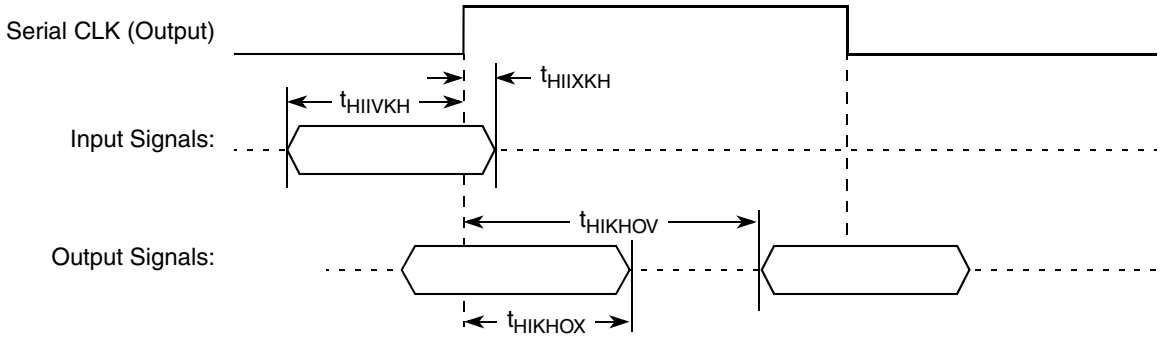


Figure 37. AC Timing (Internal Clock) Diagram

2.9 High-Speed SerDes Interfaces (HSSI)

The MPC859E features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications.The SerDes interface can be used for PCI Express and/or Serial RapidIO and/or SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

2.9.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

The below figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. The following figure shows the waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

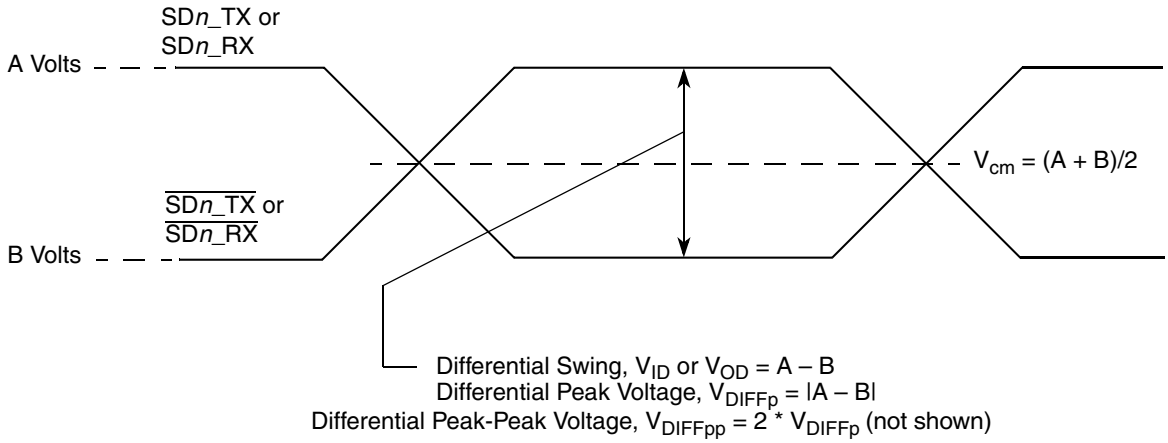


Figure 38. Differential Voltage Definitions for Transmitter or Receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing The transmitter output signals and the receiver input signals SD_TX, $\overline{\text{SD\_TX}}$, SD_RX and $\overline{\text{SD\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or **Differential Output Swing**):

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TX} - V_{\overline{SD\_TX}}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or **Differential Input Swing**):

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RX} - V_{\overline{SD\_RX}}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD\_TX}}$, for example) from the non-inverting signal ($\overline{\text{SD\_TX}}$, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 43 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TX} + V_{\overline{SD\_TX}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage

may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and $\overline{\text{TD}}$. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.9.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes.The SerDes reference clock inputs are SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ for PCI Express, Serial RapidIO, and SGMII interface, respectively.

The following sections describe the SerDes reference clock requirements and provide application information.

2.9.2.1 SerDes Spread Spectrum Clock Source Recommendations

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are designed to work with spread spectrum clock for PCI Express protocol only with the spreading specification defined in Table 47. When using spread spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

The spread spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread spectrum supported protocols. For example, if the spread spectrum clocking is desired on a SerDes reference clock for PCI Express and the same reference clock is used for any other protocol such as SGMII/SRIO due to the SerDes lane usage mapping option, spread spectrum clocking cannot be used at all.

Table 47. SerDes Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 3.

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	—
Frequency spread	+0	–0.5	%	1

Note:

1. Only down spreading is allowed.

2.9.2.2 SerDes Reference Clock Receiver Characteristics

The following figure shows a receiver reference diagram of the SerDes reference clocks.

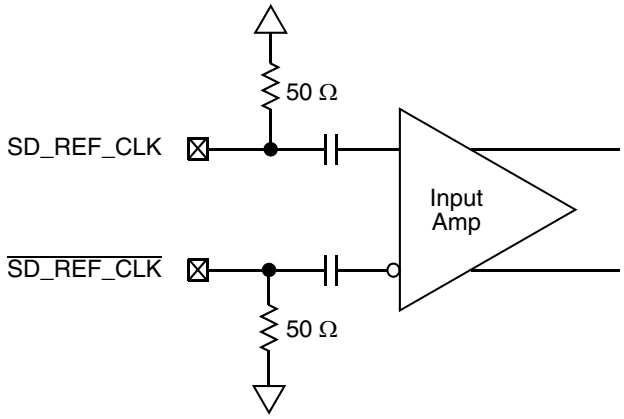


Figure 39. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The supply voltage requirements for XV_{DD} are as specified in Table 3.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 39. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to SCOREGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC-coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SCOREGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to SCOREGND DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.

2.9.2.3 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- Differential mode
  - The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC- or AC-coupled connections.

— For external DC-coupled connection, as described in Section 2.9.2.2, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. The following figure shows the SerDes reference clock input requirement for DC-coupled connection scheme.

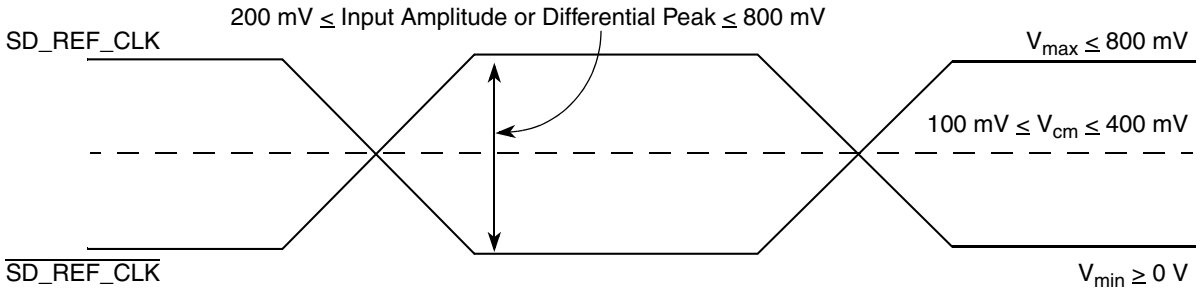


Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

— For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SCOREGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SCOREGND). The following figure shows the SerDes reference clock input requirement for AC-coupled connection scheme.

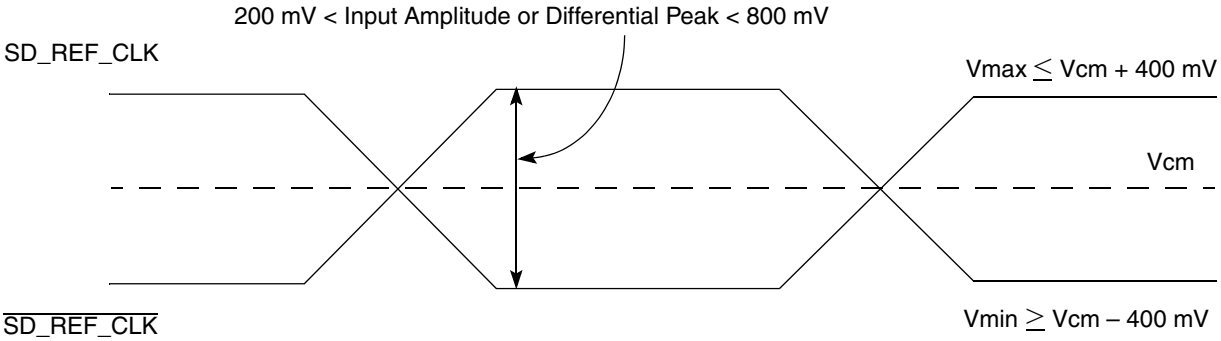


Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-ended mode
  - — The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-peak (from V_{min} to V_{max}) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  - — The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - — To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

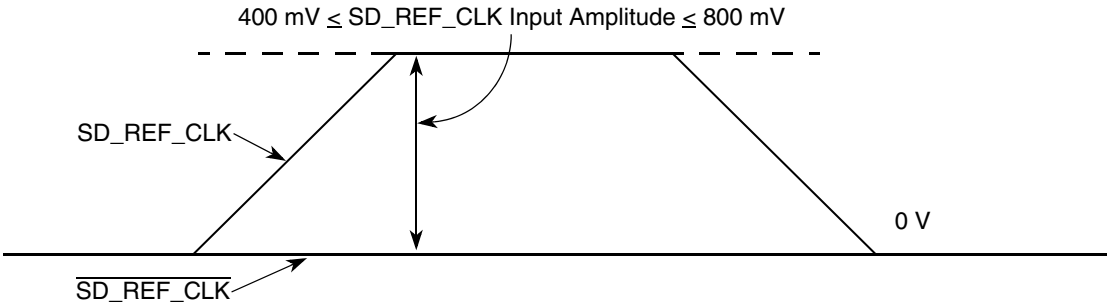


Figure 42. Single-Ended Reference Clock Input DC Requirements

2.9.2.4 AC Requirements for SerDes Reference Clocks

The following table lists AC requirements for the PCI Express, SGMII, and Serial RapidIO SerDes reference clocks to be guaranteed by the customer's application design.

Table 48. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ Input Clock Requirements

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	7
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	7
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2, 7
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3, 7

Table 48. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ Input Clock Requirements (continued)

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SD*n*_REF_CLK) to falling edge rate (SD*n*_REF_CLK) matching	Rise-Fall Matching	—	—	20	%	5, 6, 7

Notes:
1. **Caution:** Only 100 and 125 have been tested. In-between values will not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK minus $\overline{\text{SD\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 43.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD_REF_CLK and falling edge rate for $\overline{\text{SD\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK rising meets $\overline{\text{SD\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK must be compared to the fall edge rate of $\overline{\text{SD\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 44.
7. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

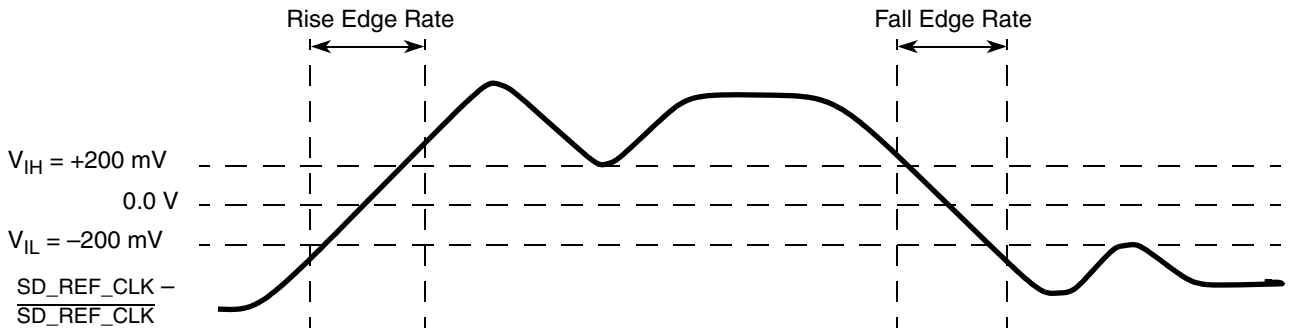


Figure 43. Differential Measurement Points for Rise and Fall Time

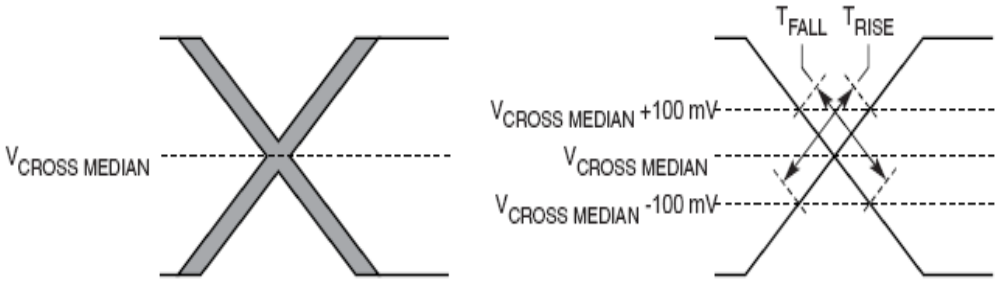


Figure 44. Single-Ended Measurement Points for Rise and Fall Time Matching

2.9.2.5 SerDes Transmitter and Receiver Reference Circuits

The following figure shows the reference circuits for SerDes data lane's transmitter and receiver.

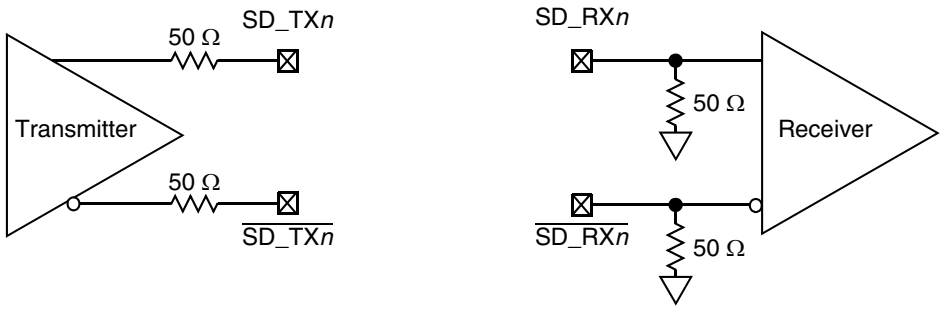


Figure 45. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section (SGMII, PCI Express, or Serial Rapid IO) in this document based on the application usage

- Section 2.6.4, "SGMII Interface Electrical Characteristics"
- Section 2.10, "PCI Express"
- Section 2.11, "Serial RapidIO (SRIO)"

Note that external AC-coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in the specification of each protocol section.

2.9.2.6 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

2.10 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8569E.

2.10.1 PCI Express DC Requirements for SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

For more information, see Section 2.9.2.3, "DC Level Requirement for SerDes Reference Clocks."

2.10.2 PCI Express DC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.10.2.1 PCI Express DC Physical Layer Transmitter Specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 Gb/s.

The following table defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 49. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output DC Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000[2]/ 1100[3]	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential TX impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	TX DC Differential mode Low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required TX D+ as well as D– DC Impedance during all states

Note:
1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 46 and measured over any 250 consecutive TX UIs.
2. Typ-$V_{TX-DIFFp-p}$ with XV_{DD} = 1.0 V
3. Typ-$V_{TX-DIFFp-p}$ with XV_{DD} = 1.1 V

2.10.2.2 PCI Express DC Physical Layer Receiver Specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 Gb/s

The following table defines the DC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 50. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	175	—	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$. See note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	RX DC Differential mode impedance. See Note 2.

Table 50. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications (continued)

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	KΩ	Required RX D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$. Measured at the package pins of the receiver.

Notes:
1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 46 must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

2.10.3 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.10.3.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5 Gb/s.

The following table defines the PCI Express (2.5Gb/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 51. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum TX eye width	T_{TX-EYE}	0.70	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.

Table 51. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications (continued)

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
AC-coupling capacitor	C_{TX}	75	—	200	nF	All transmitters are AC-coupled. The AC-coupling is required either within the media or within the transmitting component itself. See Note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 46 and measured over any 250 consecutive TX UIs.
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The MPC8569E SerDes transmitter does not have CTX built-in. An external AC-coupling capacitor is required.

2.10.3.2 PCI Express AC Physical Layer Receiver Specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 Gb/s.

The following table defines the AC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 52. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input AC Specifications

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Unit interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 4.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 46 must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.10.4 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

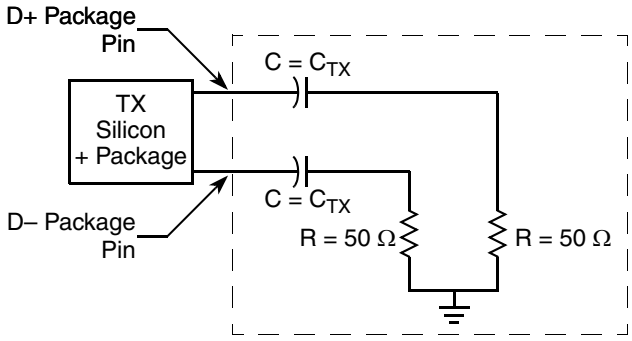


Figure 46. Compliance Test/Measurement Load

2.11 Serial RapidIO (SRIO)

This section describes the DC and AC electrical specifications for the Serial RapidIO interface of the MPC8569E, for the LP-serial physical layer. The electrical specifications cover both single- and multiple-lane links. Two transmitters (short and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short- and long-run transmitter specifications.

The short-run transmitter must be used mainly for chip-to-chip connections on either the same printed-circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short-run specification reduce the overall power used by the transceivers.

The long-run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC-coupling at the receiver input must be used.Signal Definitions

2.11.1 Signal Definitions

This section defines terms used in the description and specification of differential signals used by the LP-Serial links. Figure 47 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input

(RD and $\overline{RD}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{TD}$, RD, and $\overline{RD}$ each have a peak-to-peak swing of A – B volts
2. The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{\overline{TD}}$
3. The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{\overline{RD}}$
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A – B volts
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) volts

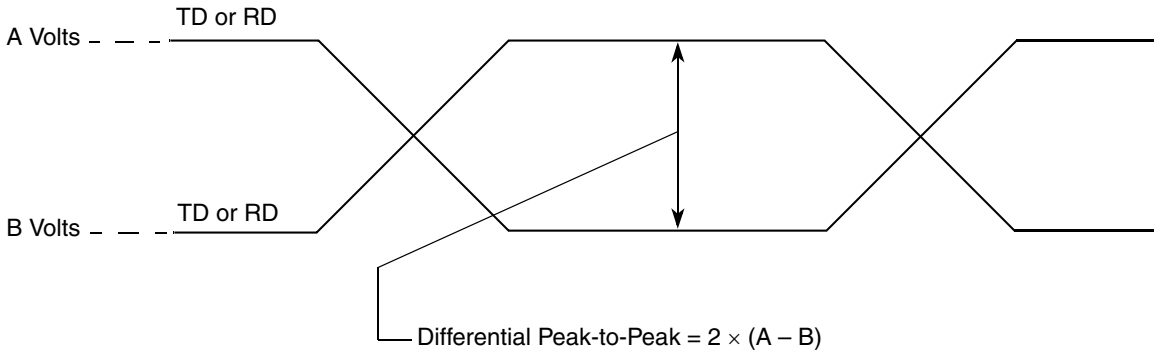


Figure 47. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{TD}$ is 500 mV p-p. The differential output signal ranges between 500 and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

2.11.2 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- Pre-emphasis on the transmitter
- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

2.11.3 DC Requirements for Serial RapidIO

This section explains the DC requirements for the Serial RapidIO interface.

2.11.3.1 DC Requirements for Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clocks of the SRIO interface are described in Section 2.9.2.3, "DC Level Requirement for SerDes Reference Clocks."

2.11.3.2 DC Serial RapidIO Timing Transmitter Specifications

The LP-serial transmitter electrical and timing specifications are given in the following sections.

The differential return loss, S11, of the transmitter in each case are better than the following:

- –10 dB for (Baud Frequency) ÷ 10 < Freq(f) < 625 MHz
- –10 dB + 10log(f ÷ 625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100-Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

The following table defines the serial RapidIO transmitter DC specifications.

Table 53. SRIO Transmitter DC Timing Specifications—1.25, 2.5, and 3.125 GBauds

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output voltage	V_O	–0.40	—	2.30	V	1
Long-run differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—
Short-run differential output voltage	V_{DIFFPP}	500	—	1000	mV p-p	—

Note:
1. Voltage relative to COMMON of either signal comprising a differential pair.

2.11.3.3 DC Serial RapidIO Receiver Specifications

The LP-serial receiver electrical and timing specifications are given in the following sections.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (baud frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

The following table defines the serial RapidIO receiver DC specifications.

Table 54. SRIO Receiver DC Timing Specifications—1.25 GBaud, 2.5 GBaud, 3.125 GBaud

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	V_{IN}	200	—	1600	mV p-p	1

Note:
1. Measured at receiver

2.11.4 AC Requirements for Serial RapidIO

This section explains the AC requirements for the Serial RapidIO interface.

2.11.4.1 AC Requirements for Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Note that the Serial RapidIO clock requirements for SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ are intended to be used within the clocking guidelines specified by Section 2.9.2.4, “AC Requirements for SerDes Reference Clocks.”

2.11.4.2 AC Requirements for Serial RapidIO Transmitter

The following table defines the transmitter AC specifications for the Serial RapidIO. The AC timing specifications do not include RefClk jitter

Table 55. SRIO Transmitter AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter	J_D	—	—	0.17	UI p-p	—
Total jitter	J_T	—	—	0.35	UI p-p	—
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—

The following table defines the receiver AC specifications for Serial RapidIO. The AC timing specifications do not include RefClk jitter.

Table 56. SRIO Receiver AC Timing Specifications

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1, 3
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1, 3
Total jitter tolerance[2]	J_T	0.65	—	—	UI p-p	1, 3
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—

Notes:
1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 48. The sinusoidal jitter component is included to ensure margin for low-frequency jitter, wander, noise, crosstalk, and other variable system effects.
3. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

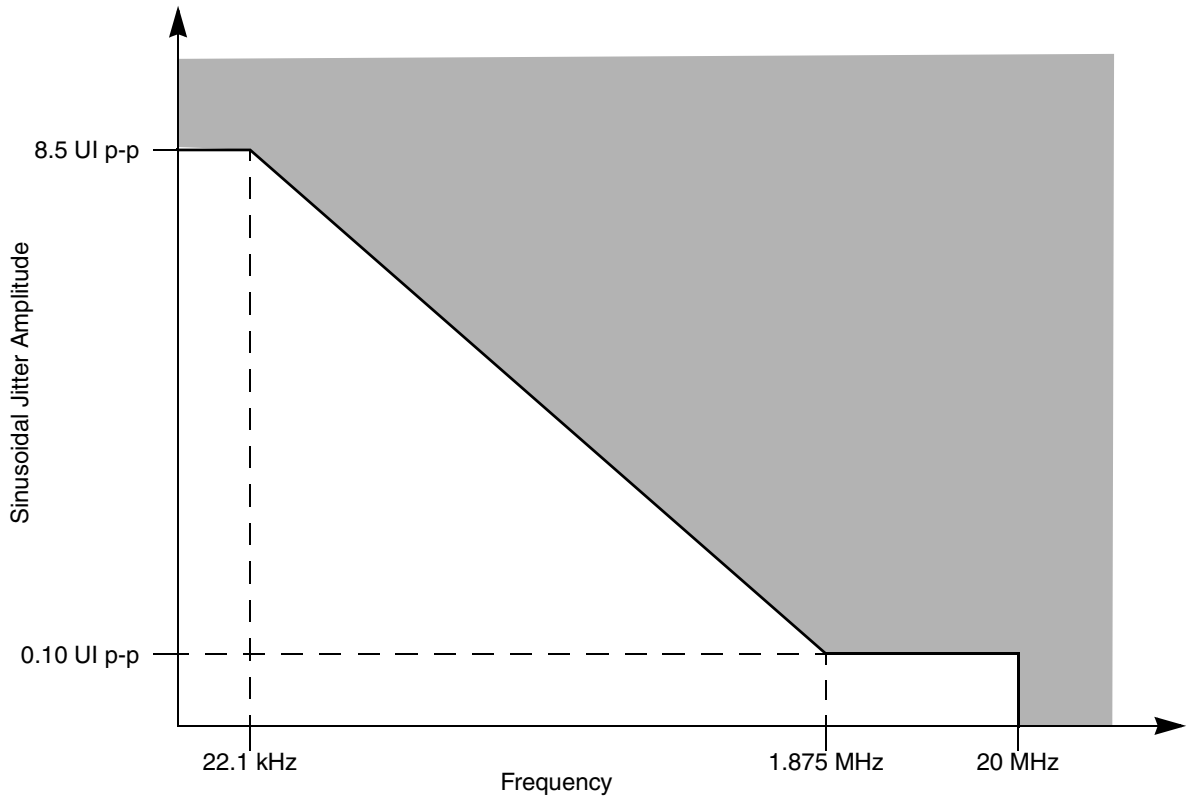


Figure 48. Single Frequency Sinusoidal Jitter Limits

2.12 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8569E.

2.12.1 I²C DC Electrical Characteristics

The following table provides the DC electrical characteristics for the I²C interface.

Table 57. I²C DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.4	V	2

Table 57. I²C DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD} (max))	I_I	–10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the *MPC8569E PowerQUICC III Integrated Processor Family Reference Manual* for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.12.2 I²C AC Electrical Specifications

The following table provides the AC timing parameters for the I²C interface.

Table 58. I²C AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%

Parameter	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—

Table 58. I²C AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%

Parameter	Symbol[1]	Min	Max	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the MPC8659E provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the MPC8569E acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8569E does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the MPC8569E as transmitter, application note AN2919, referred to in note 4 below, is recommended.
4. The maximum t_{I2OVKL} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

The following figure provides the AC test load for the I²C.

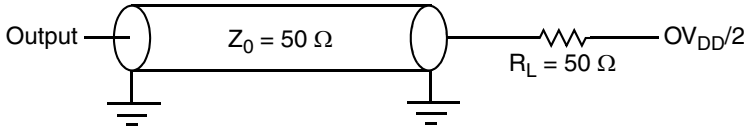


Figure 49. I²C AC Test Load

The following figure shows the AC timing diagram for the I²C bus.

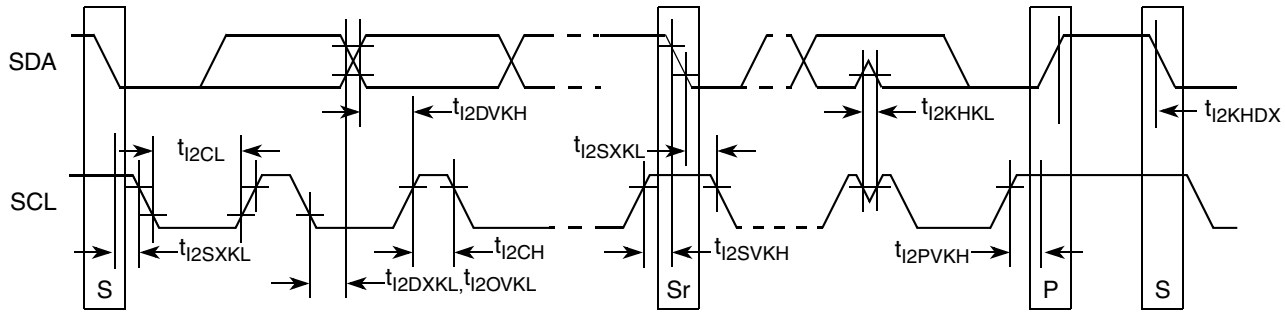


Figure 50. I²C Bus AC Timing Diagram

2.13 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface.

2.13.1 GPIO DC Electrical Characteristics

The following table provides the DC electrical characteristics for the GPIO interface when operating from a 3.3 V supply

Table 59. GPIO DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.13.2 GPIO AC Timing Specifications

The following table provides the GPIO input and output AC timing specifications.

Table 60. GPIO Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

The following figure provides the AC test load for the GPIO.

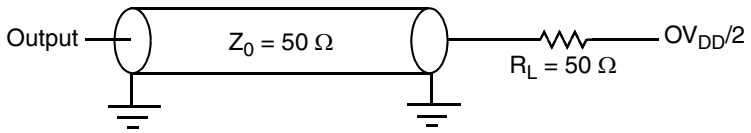


Figure 51. GPIO AC Test Load

2.14 JTAG Controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

2.14.1 JTAG DC Electrical Characteristics

The following table provides the JTAG DC electrical characteristics.

Table 61. JTAG DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.14.2 JTAG AC Timing Specifications

The following table provides the JTAG AC timing specifications as defined in Figure 52 through Figure 55.

Table 62. JTAG AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	4
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	—

Table 62. JTAG AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times: Boundary-scan data TDO	t_{JTKLDV}	 — —	 15 10	ns	3
Output hold times	t_{JTKLDX}	0	—	ns	3

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
4. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing

The following figure provides the AC test load for TDO and the boundary-scan outputs of the device.

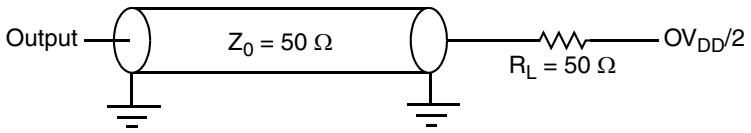


Figure 52. AC Test Load for the JTAG Interface

The following figure provides the JTAG clock input timing diagram.

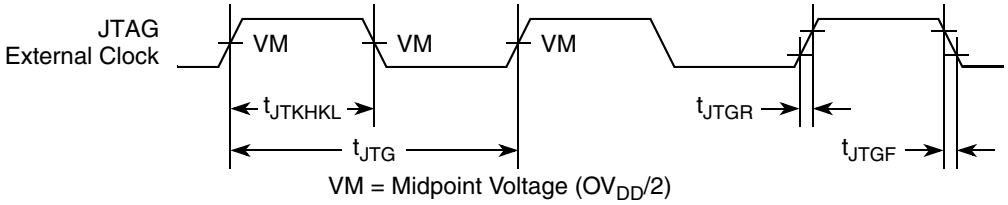


Figure 53. JTAG Clock Input Timing Diagram

The following figure provides the $\overline{\text{TRST}}$ timing diagram.

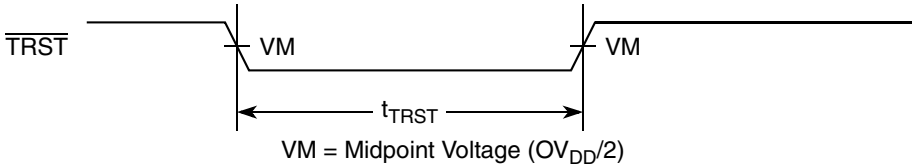


Figure 54. $\overline{\text{TRST}}$ Timing Diagram

The following figure provides the boundary-scan timing diagram.

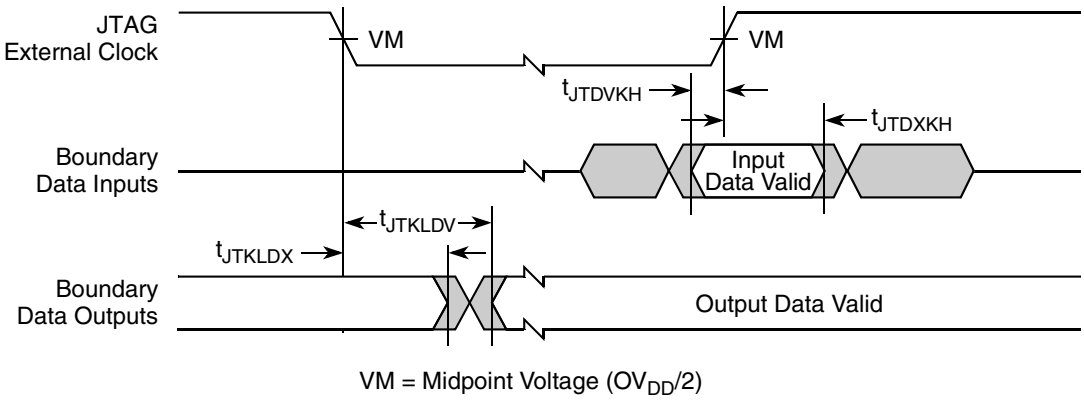


Figure 55. Boundary-Scan Timing Diagram

2.15 Enhanced Local Bus Controller

This section describes the DC and AC electrical specifications for the enhanced local bus interface of the MPC8569E.

2.15.1 Enhanced Local Bus DC Electrical Characteristics

The following table provides the DC electrical characteristics for the enhanced local bus interface when operating at BV_{DD} = 3.3 V DC.

Table 63. Enhanced Local Bus DC Electrical Characteristics (3.3 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.1.1, “Recommended Operating Conditions.”

The following table provides the DC electrical characteristics for the enhanced local bus interface when operating at BV_{DD} = 2.5 V DC.

Table 64. Enhanced Local Bus DC Electrical Characteristics (2.5 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.1.1, "Recommended Operating Conditions."

The following table provides the DC electrical characteristics for the enhanced local bus interface when operating at BV_{DD} = 1.8 V DC.

Table 65. Enhanced Local Bus DC Electrical Characteristics (1.8 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.1.1, "Recommended Operating Conditions."

2.15.2 Enhanced Local Bus AC Electrical Specifications

This section describes the AC timing specifications for the enhanced local bus interface.

2.15.2.1 Test Condition

The following figure provides the AC test load for the enhanced local bus.

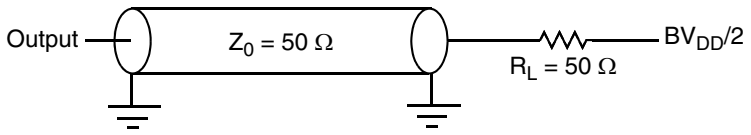


Figure 56. Enhanced Local Bus AC Test Load

2.15.2.2 Enhanced Local Bus AC Timing Specifications for PLL Enable Mode

For PLL enable mode, all timings are relative to the rising edge of LSYNC_IN.

The following table describes the timing specifications of the enhanced local bus interface at BV_{DD} = 3.3 V, 2.5 V and 1.8 V for PLL enable mode.

Table 66. Enhanced Local Bus Timing Specifications (BV_{DD} = 3.3 V 2.5 V and 1.8 V) —PLL Enabled Mode

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
Enhanced local bus cycle time	t_{LBK}	7.5	12	ns	—
Enhanced local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	5
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	680	ps	2
Input setup	t_{LBIVKH}	2	—	ns	—
Input hold	t_{LBIXKH}	1.0	—	ns	—
Output delay (Except LALE)	t_{LBKHOV}	—	3.8	ns	—
Output hold (Except LALE)	t_{LBKHOX}	0.6	—	ns	—
Enhanced local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	1 – 0.475 ns (LBCR[AHD]=0) ½ – 0.475 ns (LBCR[AHD] = 1)	—	eLBC controller clock cycle (= 1 platform clock cycle in ns)	4

Notes:

1. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLK signals at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle. The eLBC controller clock refers to the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle × LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure shows the AC timing diagram for PLL-enabled mode.

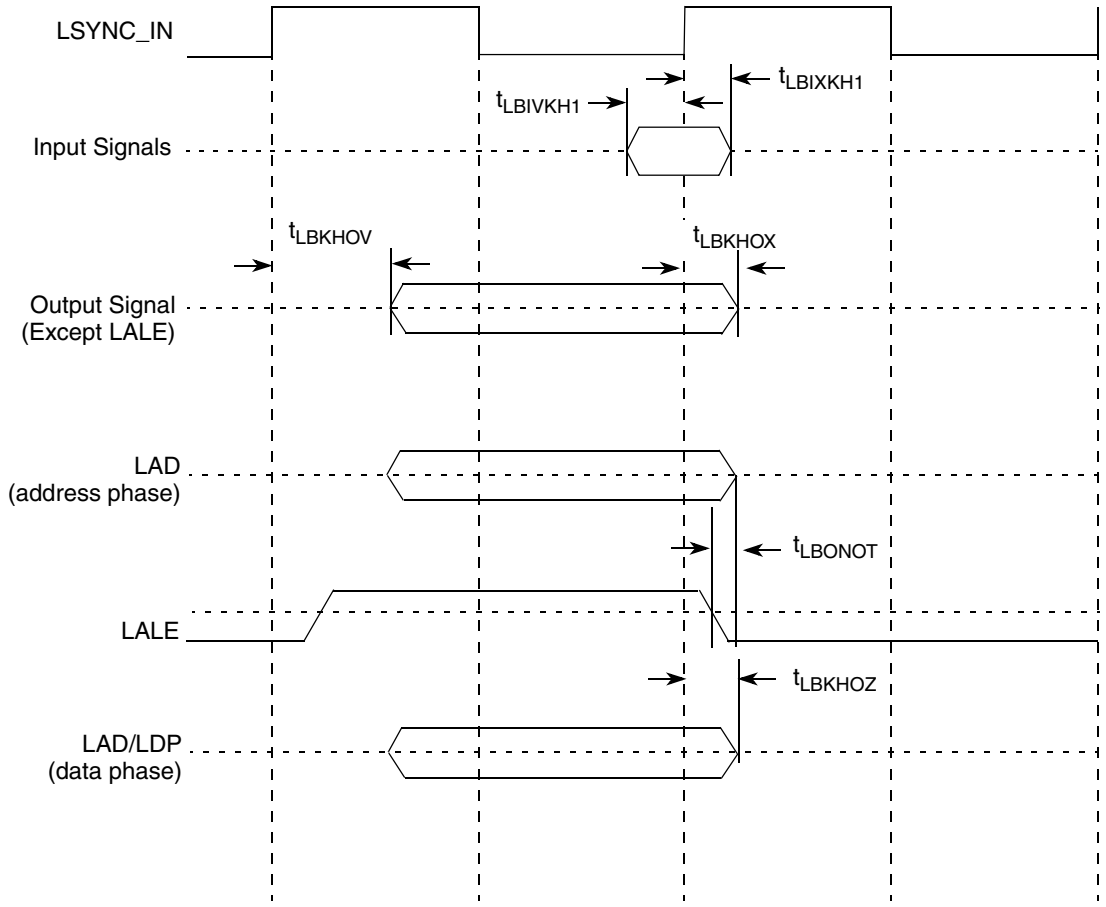


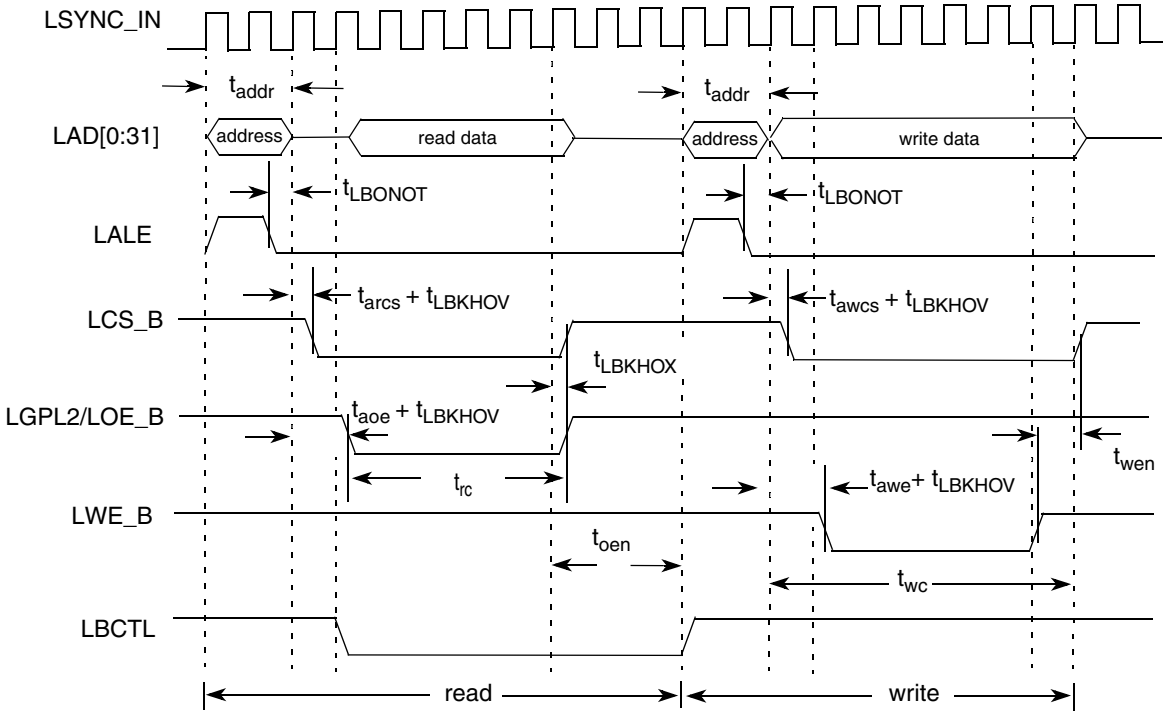
Figure 57. Local Bus AC Timing Diagram (PLL Enabled)

The above figure applies to all three controllers that eLBC supports: GPCM, UPM and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

The following figure shows how the AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. Refer to reference manual.

Figure 58. GPCM Output Timing Diagram (PLL Enabled)

2.15.2.3 Enhanced Local Bus AC Timing Specifications for PLL Bypass Mode

All output signal timings are relative to the falling edge of any LCLKs for PLL bypass mode. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LUPWAIT/LFRB are relative to the rising edge of LCLKs. LUPWAIT/LFRB are relative to the falling edge of LCLKs.

The following table describes the timing specifications of the enhanced local bus interface at BV_{DD} = 3.3, 2.5, and 1.8 V DC with PLL disabled.

Table 67. Enhanced Local Bus Timing Specifications (BV_{DD} = 3.3 V, 2.5 V, and 1.8 V)—PLL Bypassed

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
Enhanced local bus cycle time	t_{LBK}	12	—	ns	—
Enhanced local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	6
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	2
Input setup (except LUPWAIT/LFRB)	t_{LBIVKH}	6.5	—	ns	—
Input hold (except LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—
Input setup (for LUPWAIT/LFRB)	t_{LBIVKL}	6.5	—	ns	—
Input hold (for LUPWAIT/LFRB)	t_{LBIXKL}	1	—	ns	—
Output delay (Except LALE)	t_{LBKLOV}	—	1.5	ns	—
Output hold (Except LALE)	t_{LBKLOX}	–3.5	—	ns	5
Enhanced local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ}	—	2	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	1 – 1 ns (LBCR[AHD] = 0) 1/2 – 1 ns (LBCR[AHD] = 1)	—	eLBC controller clock cycle (=1 platform clock cycle in ns)	4

Notes:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLK signals at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle × LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.
5. Output hold is negative. This means that output transition happens earlier than the falling edge of LCLK.
6. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure shows the AC timing diagram for PLL bypass mode.

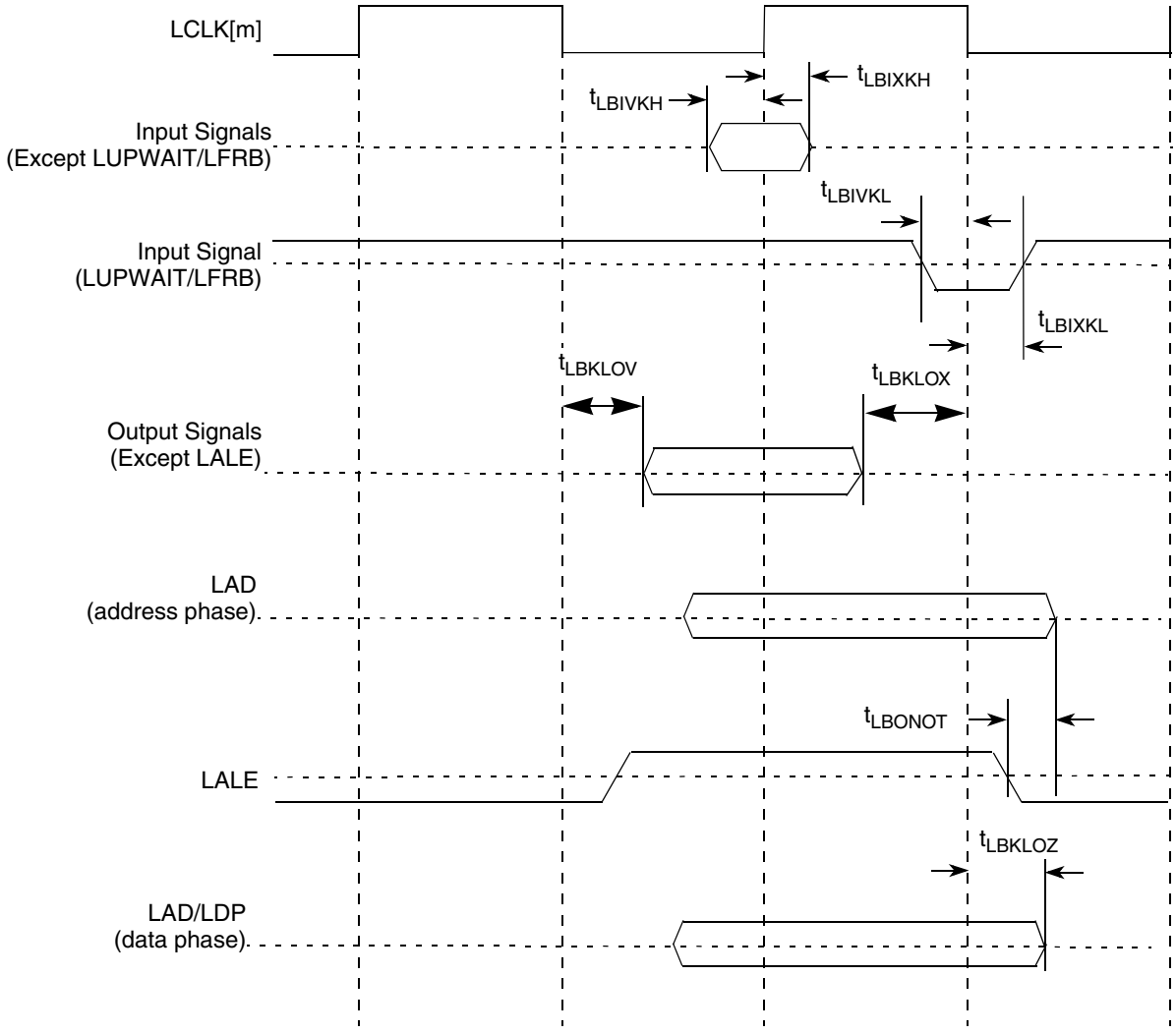


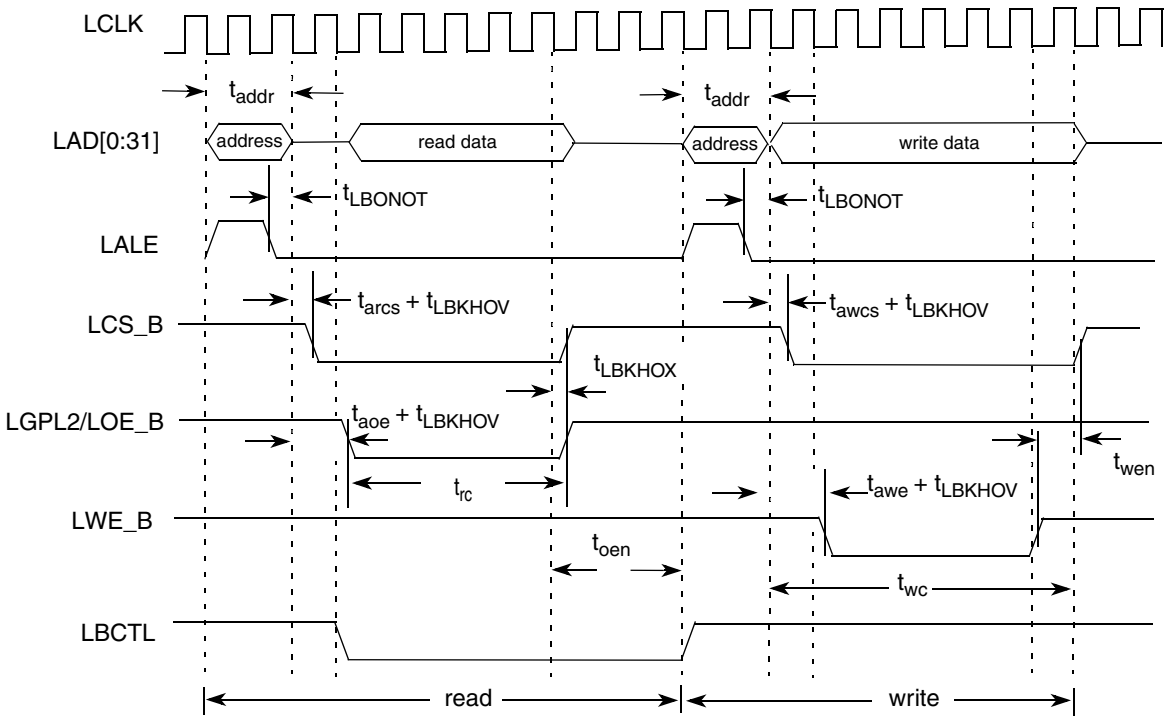
Figure 59. Enhanced Local Bus Signals (PLL Bypass Mode)

The above figure applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

The following figure shows how the AC timing diagram applies to GPCM in PLL bypass mode. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. Refer to the MPC8569E reference manual.

Figure 60. GPCM Output Timing Diagram (PLL Bypass Mode)

2.16 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface of the MPC8569E.

2.16.1 eSDHC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the eSDHC interface of the MPC8569E.

Table 68. eSDHC Interface DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	0.625 × OV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.25 × OV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = –100 µA at OV_{DD} min	0.75 × OV_{DD}	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100 µA at OV_{DD} min	—	0.125 × OV_{DD}	V	—

Table 68. eSDHC Interface DC Electrical Characteristics (continued)

At recommended operating conditions with OV_{DD} = 3.3 V

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –100 μA	OV_{DD} – 0.2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	μA	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Open drain mode for MMC cards only.

2.16.2 eSDHC AC Timing Specifications

The following table provides the eSDHC AC timing specifications as defined in Figure 61 and Figure 62.

Table 69. eSDHC AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency: SD/SDIO full speed/high speed mode MMC full speed/high speed mode	f_{SHSCK}	0	 25/50 20/52	MHz	2, 4
SD_CLK clock low time—High speed/Full speed mode	t_{SHSCKL}	7/10	—	ns	4
SD_CLK clock high time—High speed/Full speed mode	t_{SHSCKH}	7/10	—	ns	4
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	4, 5
Input setup times: SD_CMD, SD_DATx, $\overline{SD\_CD}$ to SD_CLK	$t_{SHSIVKH}$	3.7	—	ns	3, 4, 6
Input hold times: SD_CMD, SD_DATx, $\overline{SD\_CD}$ to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	4, 6
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	–3	3	ns	4, 6

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full speed mode, clock frequency value can be 0–25 MHz for a SD/SDIO card and 0–20 MHz for a MMC card. In high speed mode, clock frequency value can be 0–50 MHz for a SD/SDIO card and 0–52 MHz for a MMC card.
3. To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 0.65ns.
4. Ccard ≤10 pF, (1 card) and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF.
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
6. The parameter values apply to both full speed and high speed modes.

The following figure provides the eSDHC clock input timing diagram.

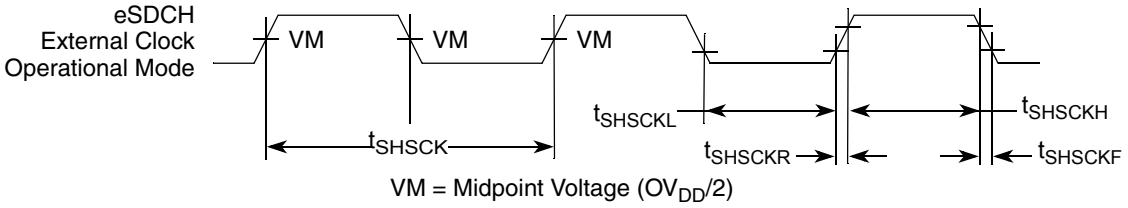


Figure 61. eSDHC Clock Input Timing Diagram

The following figure provides the data and command input/output timing diagram.

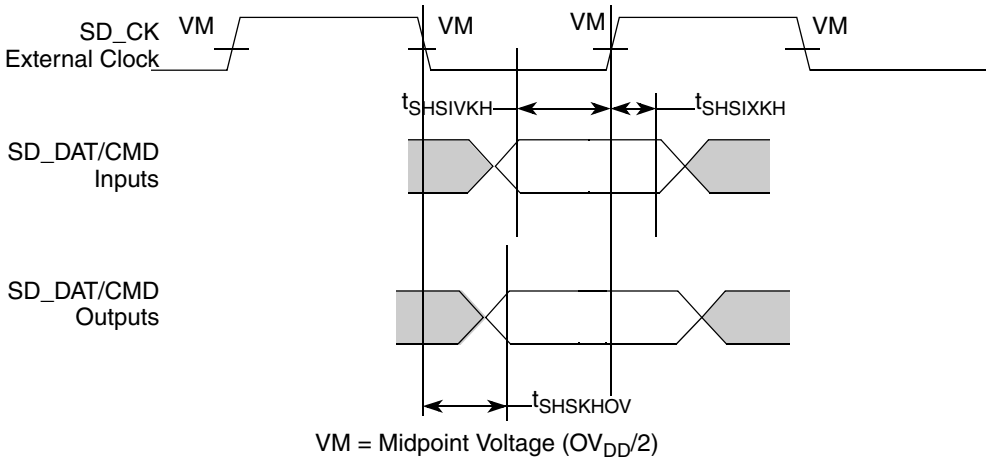


Figure 62. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.17 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8569E.

2.17.1 Timers DC Electrical Characteristics

The following table provides the timers DC electrical characteristics.

Table 70. Timers DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OVIN = 0 V or OVIN = OVDD)	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.17.2 Timers AC Timing Specifications

The following table provides the timers input and output AC timing specifications.

Table 71. Timers Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Typ	Unit	Notes
Timers inputs—minimum pulse width	t_{TIWID}	20	ns	1, 2

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs must be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

The following figure provides the AC test load for the timers.

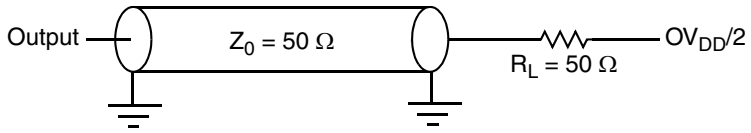


Figure 63. Timers AC Test Load

2.18 Programmable Interrupt Controller (PIC)

This section describes the DC and AC electrical specifications for the PIC of the MPC8569E.

2.18.1 PIC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the external interrupt pins $\overline{IRQ}[0:6]$, $\overline{IRQ}[8:11]$ and $\overline{IRQ\_OUT}$ of the PIC, as well as the port interrupts of the QUICC Engine block.

Table 72. PIC DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.18.2 PIC AC Timing Specifications

The following table provides the PIC input and output AC timing specifications.

Table 73. PIC Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLK	1

Note:

1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs must be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

2.19 SPI Interface

This section describes the SPI DC and AC electrical specifications of the MPC8569E.

2.19.1 SPI DC Electrical Characteristics

The following table provides the SPI DC electrical characteristics.

Table 74. SPI DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.19.2 SPI AC Timing Specifications

The following table and provide the SPI input and output AC timing specifications.

Table 75. SPI AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}	—	6	ns	2
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns	2
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}	—	9	ns	2
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2	—	ns	2

Table 75. SPI AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4	—	ns	—
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns	—
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns	—

Note:

1 The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following figure provides the AC test load for the SPI.

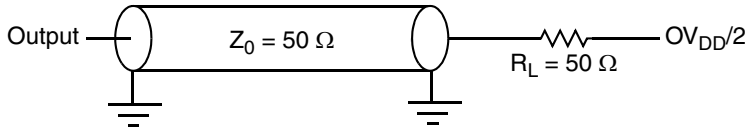
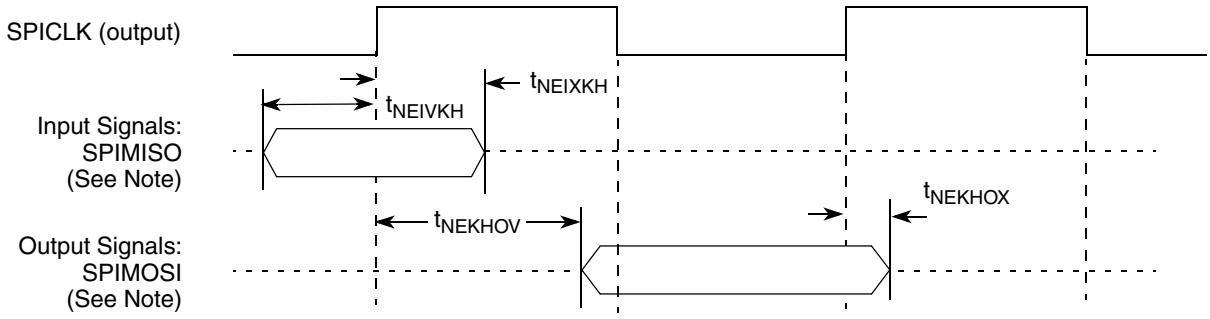


Figure 64. SPI AC Test Load

Figure 65 and Figure 66 represent the AC timing from Table 75. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

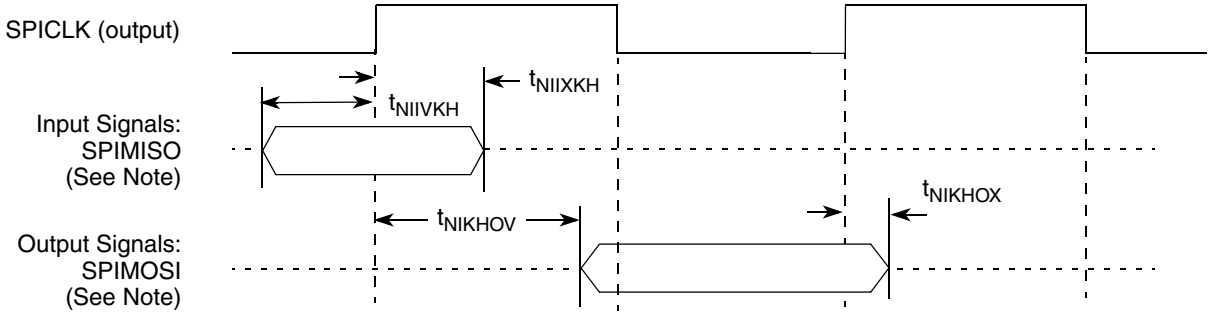
The following figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 65. SPI AC Timing in Slave Mode (External Clock) Diagram

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 66. SPI AC Timing in Master Mode (Internal Clock) Diagram

2.20 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8569E.

2.20.1 TDM/SI DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8569E TDM/SI.

Table 76. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—
Input high voltage	V_{IH}	2.0	OV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.8	V	—
Input current (0 V ≤ V_{IN} ≤ OV_{DD})	I_{IN}	—	±40	μA	1

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} referenced in Table 2 and Table 3.

2.20.2 TDM/SI AC Timing Specifications

The following table provides the TDM/SI input and output AC timing specifications.

NOTE: Rise/Fall Time on QE Input Pins

The rise / fall time on QE input pins should not exceed 5ns. This must be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of Vcc; fall time refers to transitions from 90% to 10% of Vcc.

Table 77. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	11	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

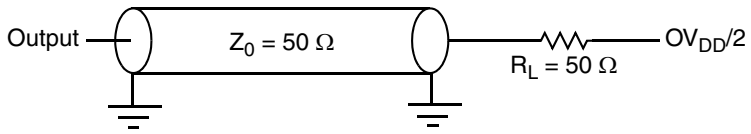
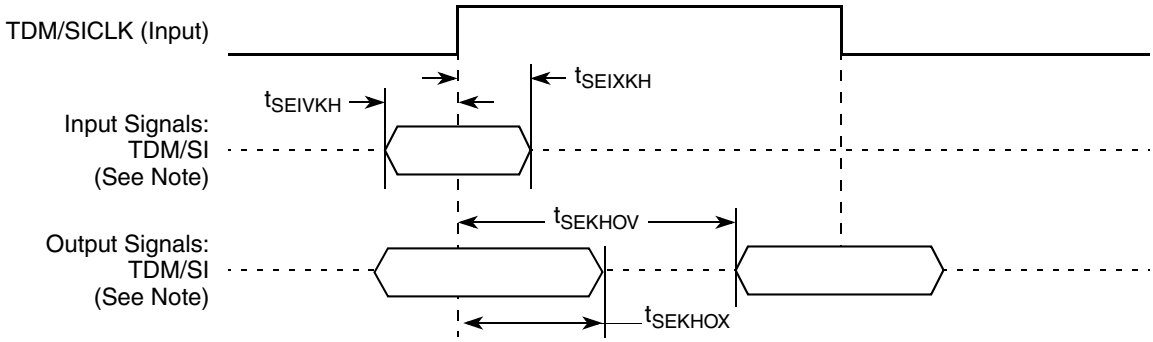


Figure 67. TDM/SI AC Test Load

The below figure represents the AC timing from Table 77. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. The following figure shows the TDM/SI timing with external clock.



Note: The clock edge is selectable on TDM/SI.

Figure 68. TDM/SI AC Timing (External Clock) Diagram

2.21 USB Interface

This section provides the AC and DC electrical specifications for the USB interface of the MPC8569E.

2.21.1 USB DC Electrical Characteristics

The following table provides the USB DC electrical characteristics.

Table 78. USB DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—
Differential input sensitivity	V_{DI}	0.2	—	V	3
Differential common mode range	V_{CM}	0.8	2.5	V	3

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.
3. Applies to low/full speed

2.21.2 USB AC Electrical Specifications

The following table describes the general USB timing specifications.

Table 79. USB General Timing Parameters

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	20.83	—	ns	Full speed 48 MHz
USB clock cycle time	t_{USCK}	166.67	—	ns	Low speed 6 MHz
Skew between TXP and TXN	t_{USTSPN}	—	5	ns	2
Skew among RXP, RXN, and RXD	$t_{USRSPND}$	—	10	ns	Full-speed transitions, 2
Skew among RXP, RXN, and RXD	t_{USRPND}	—	100	ns	Low-speed transitions, 2

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(state)(signal)}}$ for receive signals and $t_{\text{(first two letters of functional block)(state)(signal)}}$ for transmit signals. For example, $t_{USRSPND}$ symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).
2. Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

The following figure provide the AC test load for the USB.

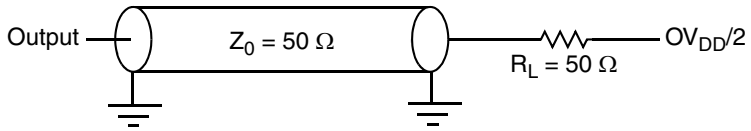


Figure 69. USB AC Test Load

2.22 UTOPIA/POS Interface

This section describes the DC and AC electrical specifications for the UTOPIA interface.

2.22.1 UTOPIA/POS DC Electrical Characteristics

The following table provides the DC electrical characteristics.

Table 80. UTOPIA/POS DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.22.2 UTOPIA/POS AC Timing Specifications

The following table provides the UTOPIA/POS input and output AC timing specifications.

Table 81. UTOPIA/POS AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
UTOPIA/POS outputs—Internal clock delay	t_{UIKHOV}	0	8.0	ns
UTOPIA/POS outputs—External clock delay	t_{UEKHOV}	1.0	10.0	ns
UTOPIA/POS outputs—Internal clock high Impedance	t_{UIKHOX}	0	8.0	ns
UTOPIA/POS outputs—External clock high impedance	t_{UEKHOX}	1.0	10.0	ns
UTOPIA/POS inputs—Internal clock input setup time	t_{UIIVKH}	6.4	—	ns

Table 81. UTOPIA/POS AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
UTOPIA/POS inputs—External clock input setup time	t_{UEIVKH}	4.0	—	ns
UTOPIA/POS inputs—Internal clock input hold time	t_{UIIXKH}	0	—	ns
UTOPIA/POS inputs—External clock input hold time	t_{UEIXKH}	1.2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA/POS outputs internal timing (UI) for the time t_{Utopia} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the UTOPIA/POS.

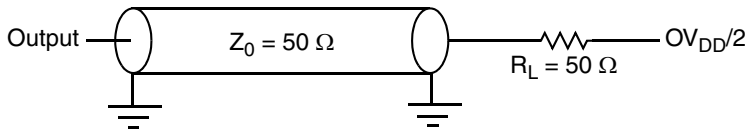


Figure 70. UTOPIA/POS AC Test Load

Figure 71 and Figure 72 represent the AC timing from Table 81. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

The following figure shows the UTOPIA/POS timing with external clock.

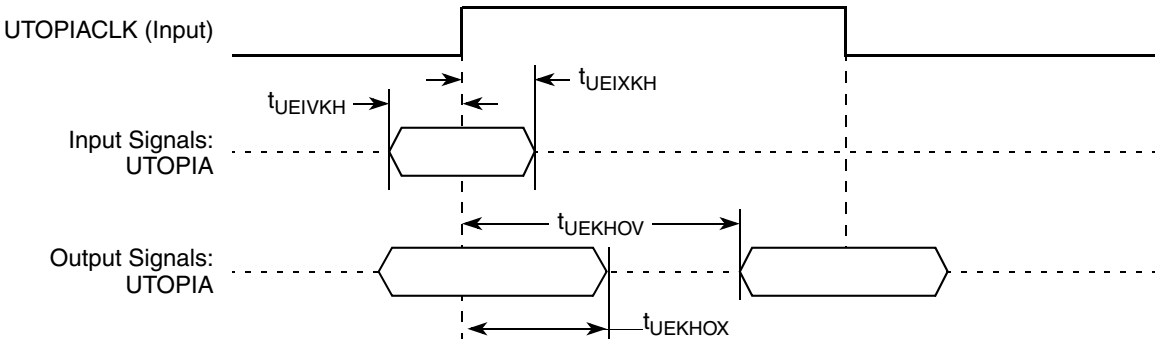


Figure 71. UTOPIA/POS AC Timing (External Clock) Diagram

The following figure shows the UTOPIA/POS timing with internal clock.

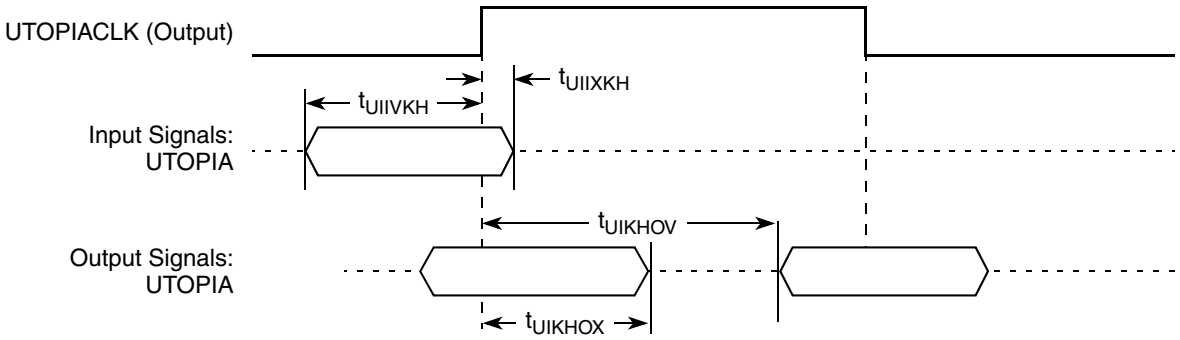


Figure 72. UTOPIA/POS AC Timing (Internal Clock) Diagram

3 Thermal

This section describes the thermal specifications of the MPC8569E.

3.1 Thermal Characteristics

The following table provides the package thermal characteristics of the MPC8569E.

Table 82. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	16	°C/W	1, 2
Junction-to-ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	12	°C/W	1, 2
Junction-to-ambient (at 200 ft/min)	Single layer board (1s)	$R_{\theta JA}$	12	°C/W	1, 2
Junction-to-ambient (at 200 ft/min)	Four layer board (2s2p)	$R_{\theta JA}$	9	°C/W	1, 2
Junction-to-board thermal	—	$R_{\theta JB}$	5	°C/W	3
Junction-to-case thermal	—	$R_{\theta JC}$	1.0	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

3.2 Recommended Thermal Model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

3.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in the following figure. The heat sink must be attached to the printed-circuit board with the spring force centered over the package. This spring force should not exceed 10 pounds force (45 Newtons).

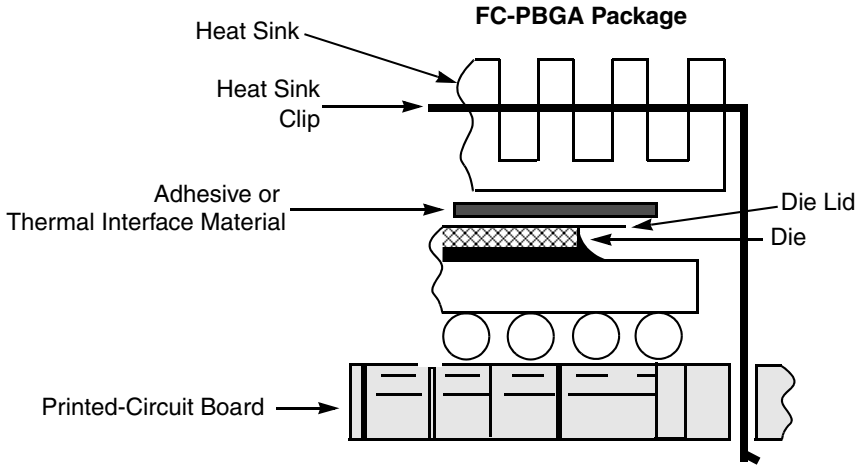


Figure 73. Package Exploded Cross-Sectional View

The system board designer can choose among several types of commercially-available heat sinks to determine the appropriate one to place on the device. Ultimately, the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.3.1 Internal Package Conduction Resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

The following figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

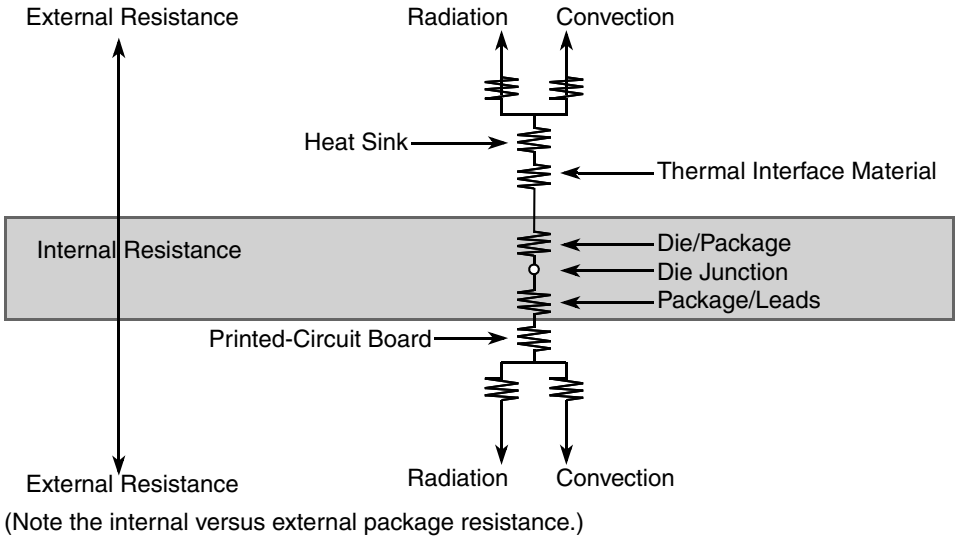


Figure 74. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and the heat sink attach material (or thermal interface material), and to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

3.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increased contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 73).

The system board designer can choose among several types of commercially-available thermal interface materials.

3.3.3 Temperature Diode

The device has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as On Semiconductor, NCT1008™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the MPC8569E on-board temperature diode:

Operating range: 10 – 230 μA

Ideality factor over 13.5 – 220 μA; n = 1.006 +/- 0.008

4 Package Description

The following section describes the detailed content and mechanical description of the package.

4.1 Package Parameters for the MPC8569E

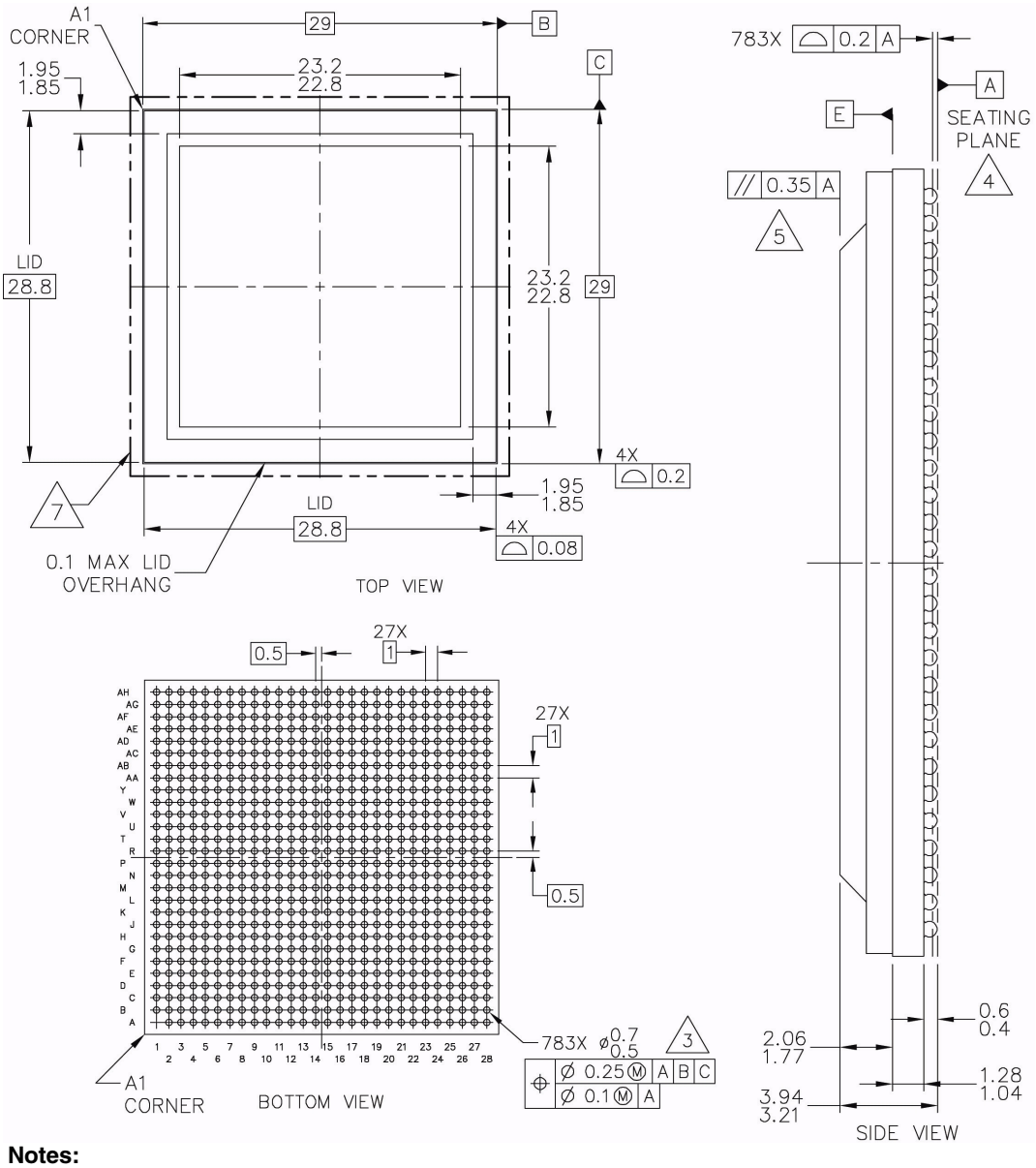
The following table provides the package parameters for the FC-PBGA. The package type is 29 mm × 29 mm, 783 plastic ball grid array (FC-PBGA).

Table 83. Package Parameters

Parameter	PBGA
Package outline	29 mm × 29 mm
Interconnects	783
Ball pitch	1 mm
Ball diameter (typical)	0.6 mm
Solder ball (lead-free)	96.5% Sn 3% Ag 0.5% Cu

4.2 Mechanical Dimensions of the FC-PBGA with Full Lid

The following figure shows the mechanical dimensions and bottom surface nomenclature for the MPC8569E FC-PBGA package with full lid.



Notes:

[1]All dimensions are in millimeters.
[2]Dimensions and tolerances per ASME Y14.5M-1994.
[3]Maximum solder ball diameter measured parallel to datum A.
[4]Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
[5]Parallelism measurement shall exclude any effect of mark on top surface of package.
[6]All dimensions are symmetric across the package center lines unless dimensioned otherwise.
[7]29.2 mm maximum package assembly (lid and laminate) x and y.

Figure 75. MPC8569E FC-PBGA Package with Full Lid

5 Ordering Information

Contact your local Freescale sales office or regional marketing team for ordering information.

Ordering information for the parts fully covered by this specification document is provided in Section 5.1, "Part Numbers Fully Addressed by This Document."

5.1 Part Numbers Fully Addressed by This Document

The following table shows the device nomenclature.

Table 84. Device Nomenclature

MPC	nnnn	E	C	Vx	AA	X	G	R
Product Code[1]	**Part Identifier**	**Security Engine**	**Temperature Range**	**Package** [2]	**Processor Frequency** [3]	**DDR Frequency**[4]	**QE Frequency**	**Revision Level**
MPC PPC	8569	E = included	Blank = 0° to 105°C C = –40° to 105°C	VT = FC-PBGA, Pb free, C5 spheres VJ = FC-PBGA, Pb free C4 bumps and pb free C5 spheres	AN = 800 MHz AQ = 1067 MHz AU = 1333 MHz	K = 600 MHz L = 667 MHz N = 800 MHz	G = 400 MHz J = 533 MHz L = 667 MHz	Blank = Rev. 1.0 (SVR = 0x8088_0010 A = Rev. 2.0 (SVR = 0x8088_0020 B = Rev. 2.1 (SVR = 0x8088_0021
		Blank = not included						A = Rev. 2.0 (SVR = 0x8080_0020 B = Rev. 2.1 (SVR = 0x8080_0021

Notes:

1. MPC stands for "qualified." PPC stands for pre-production samples.
2. See Section 4, "Package Description," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
4. See Table 85 for the corresponding maximum platform frequency.
5. C5 spheres are used by customer to attach to pcb. C4 bumps are bumps used on die of the device to connect between die and package substrate.

5.2 Part Marking

Parts are marked as the example shown in the following figure.

FC-PBGA

Notes:
MPC8569xxxxxx is the orderable part number.
MMMMM is the mask number.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.
ATWLYYWW is the traceability code.

Figure 76. Part Marking for FC-PBGA Device

6 Product Documentation

The following documents are required for a complete description of the device and are needed to design properly with the part.

- *MPC8569E PowerQUICC III Integrated Processor Reference Manual* (document number: MPC8569ERM)
- *e500 PowerPC Core Reference Manual* (document number: E500CORERM)
- *QUICC Engine Block Reference Manual with Protocol Interworking* (document number: QEIWRM)

7 Document Revision History

The following table provides a revision history for this document.

Table 85. Document Revision History

Revision	Date	Substantive Change(s)
2	10/2013	• Added footnote 5 and added new VJ package description in Table 84, “Device Nomenclature.
1	02/2012	• In Table 1, “MPC8569E Pinout Listing,” updated pin U20 from Reserved to THERM1 (internal thermal diode anode) and pin U21 from Reserved to THERM0 (internal thermal diode cathode). Removed note 9 and added note 32 to pins U20 and U21. • In Table 38, “SGMII Transmit AC Timing Specifications,” updated min and typical values for the AC coupling capacitor parameter. • In Table 48, “SD_REF_CLK and SD_REF_CLK Input Clock Requirements,” removed the condition that the reference clock duty cycle should be measured at 1.6 V. • Added Section 2.6.5.1, “QUICC Engine Block IEEE 1588 DC Specifications.” • Added Section 3.3.3, “Temperature Diode.”
0	06/2011	Initial public release

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