

AD1882A

High Definition Audio Codec

Data Sheet

Ordering Information

Device Set Order ID	Package Type	Package	Operating Temperature
AD1882AJCPZ*	QFN	48-Lead QFN, 7x7 mm	0 °C to 70 °C
AD1882AJCIZ*	QFN	48-Lead QFN, 7x7 mm	-20 °C to 85 °C
*Lead-free (Pb Free) and RoHS compliant			

Revision History

Revision	Date	Description
A	February 27, 2009	Initial release
B	November 30, 2009	Revision B release
C	December 8, 2009	Revision C release

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High Definition Audio Codec

The AD1882A audio codec and software provide superior HD audio quality that exceeds Vista Premium performance. The AD1882A has six DACs and four ADCs, two stereo headphone ports, C/LFE swapping, digital and analog PCBeep, and S/PDIF output, making the AD1882A the right choice for desktop and notebook PCs where performance is the primary consideration.

The jack retasking feature on this product supports various configurations, including platforms for 5.1 on 5 or 3 jacks, and front-panel jack retasking.

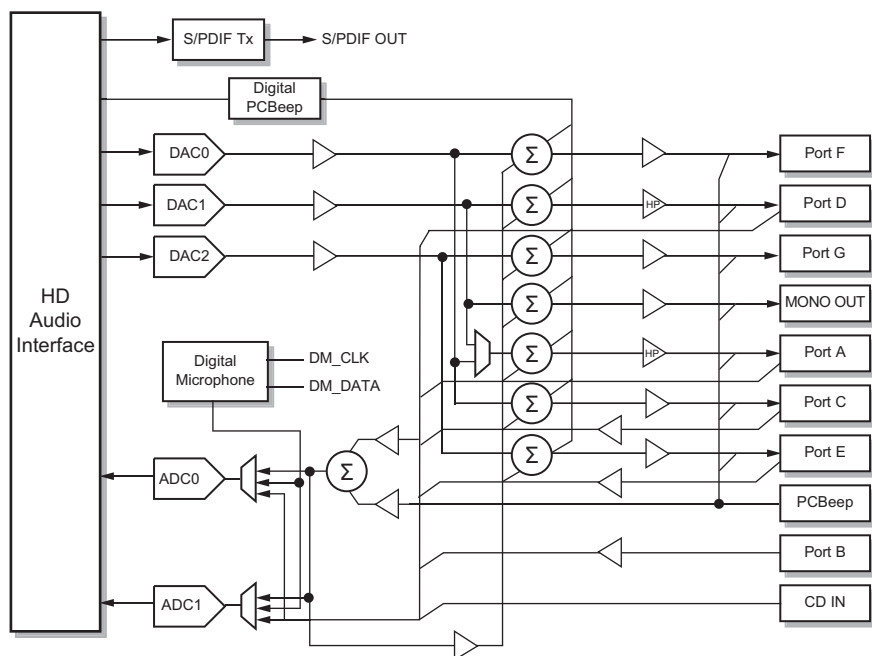
The AD1882A is available in a 48-lead Pb-free lead frame chip scale package in both reels and trays. See the Ordering Information table on the previous page

Optional Software Features

The AD1882A audio codec also supports the following additional software features:

- ◆ Voice input enhancements: Andrea Electronics best-in-class noise reduction, beam forming, and echo cancellation
- ◆ Output enhancements: Sensaura/Sonic Focus, spreading/downmixing, MP3 refinement, adaptive dynamics, compressor/limiter, speaker/graphic EQ, Voice Clarity/X-Matrix™, AGC, UI tuning tools
- ◆ DTS® SRS® Virage Logic's Sonic Focus™

Functional Block Diagram



Distinguishing Features

- ◆ Six 192 kHz, 95 dB DACs
 - All independent sample rates, 8 kHz through 192 kHz
 - 16-, 20-, and 24-bit PCM resolution
 - Selectable stereo mixer on outputs
- ◆ Four 192 kHz, 90 dB ADCs
 - Simultaneous record of up to 2 stereo channels
 - All independent sample rates, 8 kHz through 192 kHz
 - 16-, 20-, and 24-bit resolution
- ◆ S/PDIF Output
 - Supports all sample rates 44.1 kHz through 192 kHz
 - 16-, 20-, and 24-bit data widths; PCM and AC3 formats
 - Digital PCM gain control
- ◆ Dedicated auxiliary pins
 - Stereo CD input w/GND sense
 - Mono out pin for internal speaker with EAPD support
 - Analog PCBeep input pin
- ◆ Stereo digital microphone
 - Two 192 kHz digital microphone channels
 - Supports 1 or 2 microphones on 1 pin
 - Selectable bit clock rates of 1.5 MHz, 2.0 MHz, and 3.0 MHz
 - All sample rates, 8 kHz through 192 kHz
 - 16-, 20-, and 24-bit resolution
- ◆ Microsoft Vista Premium® logo for notebook and desktop
- ◆ Impedance and presence detection on all jack pins
- ◆ 2 general-purpose digital I/O (GPIO) pins
- ◆ Advanced power management modes
- ◆ EAPD control for internal speakers
- ◆ 3.3 V analog and digital supply voltage
- ◆ 1.5 V and 3.3 V HD Audio link signaling
- ◆ Very low power consumption in D3 state

Contents

	Figures	7
	Tables	9
1	High Definition Audio Codec	11
1.1	Jack Configuration	11
1.2	Specifications	12
1.2.1	HD Audio Link Specifications	17
1.2.2	Absolute Maximum Ratings	18
1.2.3	Environmental Conditions	18
1.3	Pin Configuration and Functional Descriptions	19
1.4	Digital Microphone Interface Timing Specifications	22
1.5	HD Audio Parameters	23
1.6	HD Audio Widgets	24
1.7	Default Configuration Bytes	26
1.8	Package Dimensions	27

Figures

Figure 1.	AD1882A Pinout	19
Figure 2.	Uniplex Microphone Timing	22
Figure 3.	Multiplex Microphone Timing	22
Figure 4.	Package Dimensions	27

Tables

Table 1.	Typical Desktop Configuration with Discreet Jacks	11
Table 2.	Typical Desktop Configuration with 5.1 on 3 Jacks	11
Table 4.	Typical Notebook Configuration with Digital Microphone	12
Table 5.	Test Conditions	12
Table 3.	Typical Notebook Configuration	12
Table 6.	Performance	13
Table 7.	General Specifications	13
Table 8.	Power-Down States	17
Table 9.	Absolute Maximum Ratings	18
Table 10.	Pin Descriptions	20
Table 11.	Microphone Timing Parameters	22
Table 12.	Root and Function Node Parameters	23
Table 13.	SubSystem ID	23
Table 14.	HD Audio Widgets	24
Table 15.	Default Configuration Bytes	26

High Definition Audio Codec

This data sheet provides a general overview of the AD1882A codec's architecture and functionality. Additional information on the AD1882A is available in the *AD1882A Programmers Reference Manual*. Please contact your local Conexant sales representative for more information.

1.1 Jack Configuration

Use the guidelines shown in [Tables 1](#) through [4](#) when selecting ports for particular functions.

Table 1. *Typical Desktop Configuration with Discreet Jacks*

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Panel Line-In
Port D	Rear Panel Line-Out/Headphone
Port E	Rear Panel Microphone
Port F	Rear Panel Surround
Port G	Rear Panel C/LFE

Table 2. *Typical Desktop Configuration with 5.1 on 3 Jacks*

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Panel Line-In/Surround
Port D	Rear Panel Line-Out/Headphone
Port E	Rear Panel Microphone / C/LFE

Table 3. Typical Notebook Configuration

Port	Function
Port A	Headphone
Port B	Microphone
Port C	Internal Microphone
Port D	Internal Stereo Speakers
Port E	Docking Station Line-In/Microphone

Table 4. Typical Notebook Configuration with Digital Microphone

Port	Function
Port A	Headphone
Port B	Microphone
Digital Microphone	Internal Microphone
Port D	Internal Stereo Speakers
Port E	Docking Station Line-In/Microphone

1.2 Specifications

Table 5. Test Conditions

Parameter	Test Condition
Temperature	25°C
Digital Supply	3.3 V
Analog Supply	3.3 V
MIC_BIAS_IN (via Low-Pass Filter)	5.0 V
Sample Rate f_s	48 kHz
Input Signal (Frequency Sine Wave)	1008 Hz
Amplitude for THD + N	-3.0 dB Full Scale
Analog Output Pass Band	20 Hz to 20 kHz
DAC	10 k Ω Output Load: Line Out Tests 32 Ω Output Load: Headphone Tests
ADC	0 dB Gain

Table 6. Performance

Parameter	Min	Typ	Max	Unit
Line-Out Drive (10 k Ω Loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		–85		dB
Dynamic Range (–60 dB in Ref to f_S A-Weighted)		95		dB
Signal-to-Noise Ratio		95		dB
Headphone Drive (32 Ω Loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		–83		dB
Dynamic Range (–60 dB in Ref to f_S A-Weighted)		95		dB
Signal-to-Noise Ratio		95		dB
Input Ports (Pin to ADC, Mic Boost = 0 dB)				
Total Harmonic Distortion (THD + N)		–81		dB
Dynamic Range (–60 dB in Ref to f_S A-Weighted)		90		dB
Signal-to-Noise Ratio		90		dB

Table 7. General Specifications (1 of 4)

Parameter	Min	Typ	Max	Unit
Digital Decimation and Interpolation Filters—f_S = 8 kHz to 96 kHz⁽¹⁾				
Pass Band	0		$0.4 f_S$	Hz
Pass-Band Ripple			± 0.005	dB
Stop Band	$0.6 f_S$			Hz
Stop-Band Rejection			–100	dB
Group Delay		+20		$1/f_S$
Group Delay Variation Over Pass Band		0		μs
Analog-to-Digital Converters				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage) ⁽²⁾			± 10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			± 0.5	dB
ADC Offset Error ⁽¹⁾			± 5	mV
ADC Crosstalk ⁽¹⁾				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–85		dB
Line Inputs to Other		–100	–80	dB

Table 7. General Specifications (2 of 4)

Parameter		Min	Typ	Max	Unit
Digital to Analog Converters					
Resolution			24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage) ⁽¹⁾				±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)				±0.5	dB
DAC Crosstalk (Input L, Zero R, Read R_OUT; Input R, Zero L, Read L_OUT) ⁽¹⁾			−95		dB
DAC Volumes					
Step Size (DAC-0, DAC-1, DAC-2)			1.5		dB
Output Gain/Attenuation Range		−58.5		0	dB
Mute Attenuation of 0 dB Fundamental ⁽¹⁾			−80		dB
ADC Volumes					
Step Size (ADCSEL-0, ADCSEL-1)			1.5		dB
PGA Gain/Attenuation Range		−58.5		+22.5	dB
Mute Attenuation of 0 dB Fundamental ⁽¹⁾			−80		dB
Analog Mixer					
Signal-to-Noise Ratio (SNR) Input to Output			95		dB
Step Size: All Mixer Inputs			1.5		dB
Input Gain/Attenuation Range: All Mixer Inputs		−34.5		+12.0	dB
Analog Line Level Outputs					
Full-Scale Output Voltage		1.0	1.0		V _{rms} ⁽³⁾
Ports C, E, F, and G Mono Out		2.83			V p-p
	Output Impedance ⁽¹⁾			300	Ω
	External Load Impedance ⁽¹⁾	10			kΩ
	Output Capacitance ⁽¹⁾		15		pF
	External Load Capacitance ⁽¹⁾			1000	pF

Table 7. General Specifications (3 of 4)

Parameter		Min	Typ	Max	Unit
Analog HP Drive Outputs					
Full-Scale Output Voltage		1.0			V _{rms} ⁽³⁾
Ports A and D		2.83			V p-p
	Output Impedance ⁽¹⁾			0.5	Ω
	External Load Impedance ⁽¹⁾	32			Ω
	Output Capacitance ⁽¹⁾		15		pF
	External Load Capacitance ⁽¹⁾			1000	pF
Analog Inputs					
CD, Port D (When Used as Input)			1 2.83		V _{rms} ⁽³⁾ V p-p
Microphone Boost Amplifier, Ports B, C, or E (When Used as Inputs)	Boost = 0 dB		1 2.83		V _{rms} ⁽³⁾ V p-p
	Boost = 10 dB		0.316 0.894		V _{rms} ⁽³⁾ V p-p
	Boost = 20 dB		0.1 0.283		V _{rms} ⁽³⁾ V p-p
	Boost = 30 dB		0.032 0.089		V _{rms} ⁽³⁾ V p-p
Input Impedance ⁽¹⁾			20		kΩ
Input Capacitance ⁽¹⁾			5	7.5	pF
Digital GPIO Pins: GPIO_0, GPIO_1/EAPD					
Input Signal High (V _{IH})		DV _{GPIO} × 0.60		DV _{GPIO}	V
Input Signal Low (V _{IL})		0		DV _{GPIO} × 0.24	V
Input Leakage Current (Signal High, (I _{IH}))			150		nA
Input Leakage Current (Signal Low, (I _{IL}))			50		μA
Output Signal High (V _{OH})	I _{OUT} = -500 μA	DV _{IO} × 0.72		DV _{GPIO}	V
Output Signal Low (V _{OL})	I _{OUT} = +1500 μA	0		DV _{GPIO} × 0.10	V
DM_CLK					
Output Signal High (V _{OH})	I _{OUT} = -500 μA	DV _{IO} × 0.72		DV _{GPIO}	V
Output Signal Low (V _{OL})	I _{OUT} = +1500 μA	0		DV _{GPIO} × 0.10	V

Table 7. General Specifications (4 of 4)

Parameter		Min	Typ	Max	Unit
DM_DATA					
Input Signal High (V_{IH})		$DV_{GPIO} \times 0.60$		DV_{GPIO}	V
Input Signal Low (V_{IL})		0		$DV_{GPIO} \times 0.24$	V
Input Leakage Current (Signal High, (I_{IH}))			150		nA
Input Leakage Current (Signal Low, (I_{IL}))			50		μ A
S/PDIF_OUT					
Output Signal High (V_{OH})	$I_{OUT} = -500 \mu$ A	$DV_{GPIO} \times 0.72$		DV_{GPIO}	V
Output Signal Low (V_{OL})	$I_{OUT} = +1500 \mu$ A	0		$DV_{GPIO} \times 0.10$	V
Power Supply					
Analog (AV_{DD}) 3.3 V $\pm$ 5% Power Supply Range Power Dissipation Supply Current		3.13	3.30 116 35	3.46	V mW mA
Digital (DV_{DD}) 3.3 V $\pm$ 10% Power Supply Range Power Dissipation Supply Current		2.97	3.30 162 49	3.63	V mW mA
Digital I/O (DV_{IO}) 3.3 V $\pm$ 10% Power Supply Range Power Dissipation Supply Current		2.97	3.30 3.96 1.20	3.63	V mW mA
Digital I/O (DV_{IO}) 1.5 V $\pm$ 5.5% Power Supply Range Power Dissipation Supply Current		2.97	3.30 3.96 1.20	3.63	V mW mA
Digital I/O (DV_{GPIO}) 3.3 V $\pm$ 10% Power Supply Range Power Dissipation Supply Current		2.97	3.30 3.63 1.10	3.63	V mW mA
Power Supply Rejection (100 mV p-p Signal @ 1 kHz) ⁽¹⁾			80		dB
FOOTNOTES: ⁽¹⁾ Guaranteed but not tested. ⁽²⁾ Measurements reflect ADC. ⁽³⁾ RMS values assume sine wave input.					

1.2.1 HD Audio Link Specifications

HD Audio signals comply with the High Definition Audio specifications. Please refer to these specifications at www.intel.com/standards/hdaudio.

Table 8. Power-Down States

Parameter	ID _{VDD} Typ	IA _{VDD} Typ	Unit
Function Node In D0, All Nodes Active	49	35	mA
Function Node in D3	16	0.7	mA
Codec in $\overline{\text{RESET}}$	3	3	mA
Individual block power savings			
DAC Pair Powered Down Saves (Each)	6	6	mA
ADC Pair Powered Down Saves (Each)	5	4.4	mA
Mixer Power Control (and Associated Amps) Saves	0	3	mA
MIC_BIAS Powered Down Saves ⁽¹⁾	0	1.0	mA
FOOTNOTES: ⁽¹⁾ Powering down the MIC_BIAS powers down all port MIC_BIAS pins. This disables all microphone bias circuits set to 100% or 50%, setting them to the high-Z state.			

1.2.2 Absolute Maximum Ratings

Stresses greater than those listed below may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute Maximum Ratings

Power Supplies	Rating
Digital (DV _{DD})	−0.30 V to +3.65 V
Digital I/O (DV _{I/O})	−0.30 V to +3.65 V
Digital I/O (DV _{GPIO})	−0.30 V to +3.65 V
Analog (AV _{DD})	−0.30 V to +3.65 V
Input Current (Except Supply Pins)	±10.0 mA
Analog Input Voltage (Signal Pins)	−0.30 V to AV _{DD} + 0.3 V
Digital Input Voltage (Signal Pins)	−0.30 V to DV _{I/O} + 0.3 V
Ambient Temperature (Operating) Commercial (AD1882AJCPZ) Extended Temperature (AD1882AJCIZ)	0 °C to +70 °C −20°C to +85°C
Storage Temperature	−65 °C to +150 °C



Electrostatic Discharge Device (ESD)

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

1.2.3 Environmental Conditions

Ambient Temperature Rating:

$$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$$

T_{CASE} = case temperature in °C

PD = power dissipation in W

θ_{CA} = thermal resistance (case-to-ambient)

θ_{JA} = thermal resistance (junction-to-ambient)

θ_{JC} = thermal resistance (junction-to-case)

All measurements per EIA-JESD51 with 2S2P test board per EIA-JESD51-7.

Package	θ _{JA}	θ _{JC}	θ _{CA}	Unit
QFN	47	15	32	°C/W

1.3 Pin Configuration and Functional Descriptions

Figure 1. AD1882A Pinout

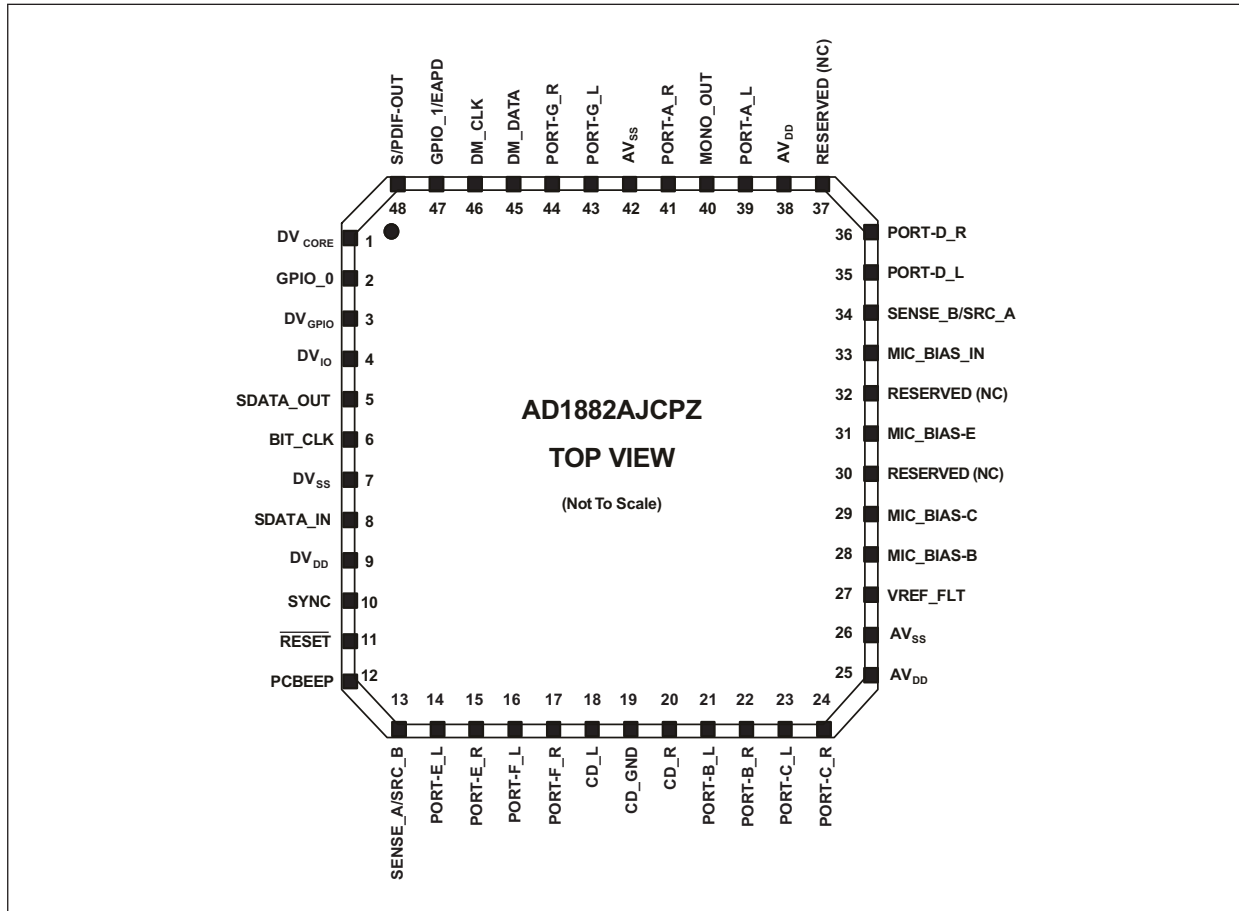


Table 10. Pin Descriptions (1 of 2)

Mnemonic	Pin No.	Function	Description
Digital Interface			
SDATA_OUT	5	I	Link Serial Data Output. AD1882A input stream. Clocked on both edges of the BIT_CLK.
BIT_CLK	6	I	Link Bit Clock. 24.000 MHz serial data clock.
SDATA_IN	8	I/O	Link Serial Data Input. AD1882A output stream Clocked only on one edge of BIT_CLK.
SYNC	10	I	Link Frame Sync.
RESET	11	I	Link Reset. AD1882A master hardware reset.
Digital I/O			
GPIO_0 GPIO_1/EAPD SPDIF_OUT	2 47 48	I/O I/O O	General-Purpose Input/Output Pin. Digital signal used to control external circuitry. General-Purpose Input/Output Pin/EAPD Pin. Digital signal used to control external circuitry. Defaults to high-Z. When used as EAPD: high-Z = amp-on, DV _{SS} = amp off. S/PDIF_OUT. Supports S/PDIF output.
DM_DATA	45	I	Digital Microphone Data Input Support for two digital microphones.
DM-CLK	46	O	Digital Microphone Clock Output.
JACK SENSE and EAPD			
SENSE_A/SRC_B SENSE_B/SRC_A	13 34	I/O I/O	JACK SENSE A-D Input/Sense B Drive. JACK SENSE E-H Input/Sense A Drive.
Analog I/O			
PCBEEP	12	LI	Monaural Input from System for Analog PCBeep.
PORT-E_L	14	LI, MIC, LO, SWAP	Auxiliary Input/Output Left Channel.
PORT-E_R	15	LI, MIC, LO, SWAP	Auxiliary Input/Output Right Channel.
PORT-F_L	16	I/O	Auxiliary Input/Output Left Channel.
PORT-F_R	17	I/O	Auxiliary Input/Output Right Channel.
CD_L	18	LI	CD Audio Left Channel.
CD_GND	19	LI	CD Audio Analog Ground Reference (for Differential CD Input). Must be connected to AGND via 0.1 mF capacitor if not in use as CD_GND.
CD_R	20	LI	CD Audio Right Channel.
PORT-B_L	21	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.
PORT-B_R	22	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.
PORT-C_L	23	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.
PORT-C_R	24	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.
PORT-D_L	35	LI, HP, LO	Rear Panel Headphone/Line-Out.
PORT-D_R	36	LI, HP, LO	Rear Panel Headphone/Line-Out.

Table 10. Pin Descriptions (2 of 2)

Mnemonic	Pin No.	Function	Description
Analog I/O (continued)			
PORT-A_L	39	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
MONO_OUT	40	LO	Monaural Output to Internal Speaker or Telephony Subsystem Speakerphone.
PORT-A_R	41	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
PORT-G_L	43	LO, SWAP	Rear Panel C/LFE Output.
PORT-G_R	44	LO, SWAP	Rear Panel C/LFE Output.
Filter/Reference			
MIC_BIAS-B	28	O	Switchable Microphone Bias. For use with Port B (Pins 21, 22).
MIC_BIAS-C	29	O	Switchable Microphone Bias. For use with Port C (Pins 23, 24).
MIC_BIAS-E	31	O	Switchable Microphone Bias. For use with Port E (Pins 14, 15).
DV _{CORE}	1	O	CAUTION: DO NOT APPLY 3.3 V TO THIS PIN! Filter connection for internal core voltage regulator. This pin must be connected to filter caps: 10 μ F, 1.0 μ F, and 0.1 μ F connected in parallel between Pin 1 and DV _{SS} (Pin 4).D
VREF_FLT	27	O	Voltage Reference Filter. This pin must be connected to filter caps: 1.0 μ F and 0.1 μ F connected in parallel between Pin 27 and AV _{SS} (Pins 26, 42).
Power and Ground			
DV _{IO} 3.3 V $\pm$ 10% or DV _{IO} 1.5 V $\pm$ 5.5%	4	I	Connect to the I/O Voltage Used for the HD Audio Controller Signals.
DV _{GPIO}	3	I	Connect to 3.3 V digital supply to power the GPIO and S/PDIF pins.
DV _{SS}	7	I	Digital Supply Return (Ground).
DV _{DD} (3.3 V)	9	I	Digital Supply Voltage 3.3 V. This is regulated down to DV _{CORE} on Pin 1 to supply the internal digital core internal to the AD1882A.
AV _{DD} (3.3 V)	25, 38	I	CAUTION: DO NOT APPLY 5.0 V TO THESE PINS! Analog supply voltage 3.3 V ONLY. Note: AV _{DD} supplies should be well regulated and filtered as supply noise degrades audio performance.
MIC_BIAS_IN	33	I	Source Power for Microphone Bias Boost Circuitry. Connect this pin to 5.0 V via a low-pass filter. When connected this way, the AD1882A is capable of providing 3.9 V as a microphone bias to all of the MIC_BIAS pins. If 5 V is not available, connect this pin to 3.3 V (AV _{DD}) via a low-pass filter.
AV _{SS}	26, 42	I	Analog Supply Return (Ground). AV _{SS} should be connected to DV _{SS} using a conductive trace under, or close to, the AD1882A.
GENERAL NOTES:			
1. The symbols used in this table are defined as follows:			
I = Input			
O = Output			
LI = Line level input			
LO = Line level output			
HP = Output capable of driving headphone load			
MIC = Input supports microphones with MIC bias and boost amplifier			
SWAP = Outputs can swap L/R channels (typically used to support C/LFE or shared C/LFE function).			

1.4 Digital Microphone Interface Timing Specifications

The digital microphone interface can support one or two digital microphones using two or three codec pins. Both uniplex (one microphone per data pin) and multiplex (two microphones sharing the same data pin) are supported. The timing for these configurations are shown in Figures 2 and 3. The interface can generate a microphone clock at 1.5 MHz, 2.0 MHz, or 3.0 MHz to suit quality and power requirements.

Table 11. Microphone Timing Parameters

Parameter		Min	Typ	Max	Unit
Timing Requirements					
t_0	DM_CLK (1.5 MHz) Period Duty Cycle		667 50/50		ns %
t_0	DM_CLK (2.0 MHz) Period Duty Cycle		500 50/50		ns %
t_0	DM_CLK (3.0 MHz) Period Duty Cycle		333 50/50		ns %
t_1	DM_CLK Rise Time			5	ns
t_2	DM_CLK Fall Time			5	ns
t_3	Data Setup to DM_CLK Edge	100			ns
t_4	Data Hold from DM_CLK Edge	5			ns

Figure 2. Uniplex Microphone Timing

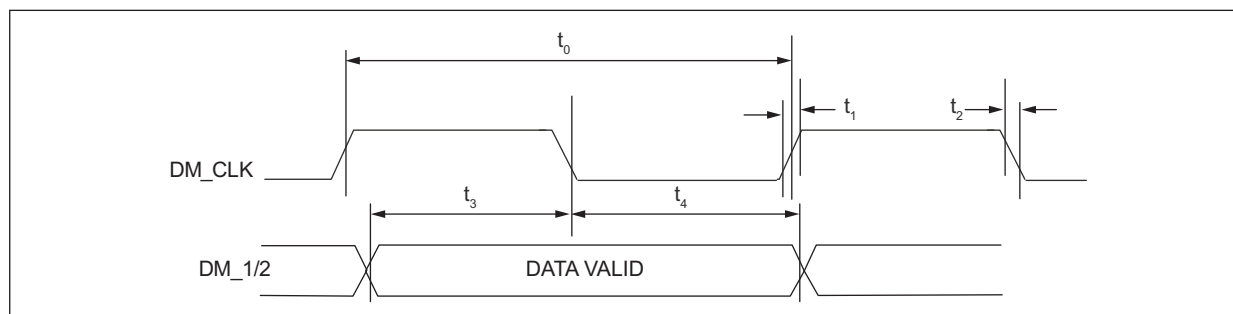
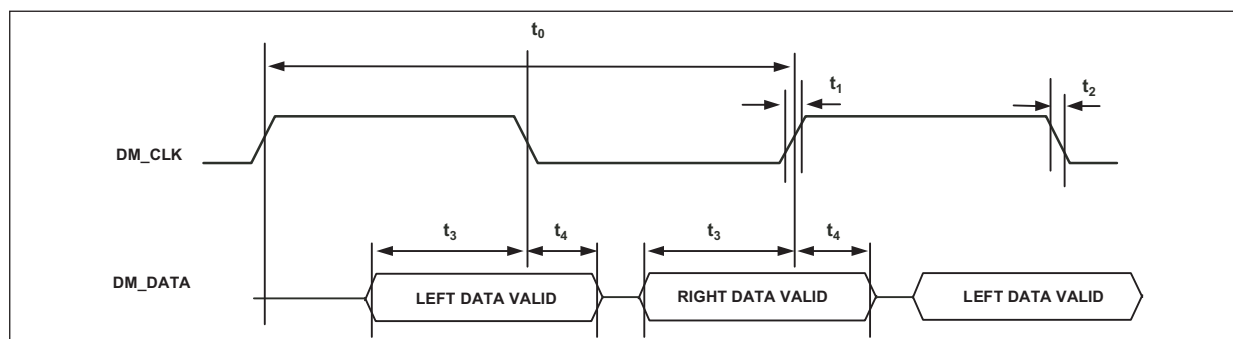


Figure 3. Multiplex Microphone Timing



1.5 HD Audio Parameters

The SSID value is set on codec power-up only. SSID is not reset by link or soft reset in order to preserve modifications by BIOS control.

Table 12. Root and Function Node Parameters

Node ID	Name	Vendor ID 00	01	Revision ID 02 ⁽¹⁾	03	Sub Node Count 04	Func. Group Type 05	Audio F.G. Caps 08	GPIO Caps 11
00	ROOT	11D4 882A		0010 0100		0001 0001			
01	FUNCTION					0002 003B	0000 0001	0001 0C0C	4000 0002
FOOTNOTES: ⁽¹⁾ Subject to change with silicon stepping.									

Table 13. SubSystem ID

Node ID	Name	Value	31:16 SSID	15:8 SKU	7:0 Asm ID
01	FUNCTION	BFD20000	BFD2	00	00
GENERAL NOTES: 1. The default SSID is overwritten by platform BIOS after power on. It is preserved across HD Audio link reset and verb reset.					

1.6 HD Audio Widgets

In [Table 14](#) below, node IDs that are not shown are reserved for future use.

Table 14. HD Audio Widgets (1 of 2)

Node ID	Name	Type ID	Type	Description
00	ROOT	x	Root	Device Identification
01	FUNCTION	x	Function	Designates this Device as an Audio Codec
02	S/PDIF DAC	0	Audio Output	S/PDIF Digital Stream Output Interface
03	DAC_0	0	Audio Output	Headphone/Surround Side (7.1) Channel Digital/Audio Converters
04	DAC_1	0	Audio Output	Stereo Front Channel Digital/Audio Converters
05	DAC_2	0	Audio Output	Stereo C/LFE Channel Digital/Audio Converters
08	ADC_0	1	Audio Input	Stereo Record Channel 1 Audio/Digital Converters
09	ADC_1	1	Audio Input	Stereo Record Channel 2 Audio/Digital Converters
0C	ADC Selector 0	3	Audio Selector	Selects and Amplifies/Attenuates the Input to ADC0
0D	ADC Selector 1	3	Audio Selector	Selects and Amplifies/Attenuates the Input to ADC1
10	Digital Beep	7	Beep Generator	Internal Digital PCBeep Signal
11	Port A (Headphone)	4	Pin Complex	Front Panel Headphone/Microphone Jack
12	Port D (Front L/R)	4	Pin Complex	Rear Panel Front/Headphone Jack
13	Mono Out	4	Pin Complex	Monaural Output Pin (Internal Speakers or Telephony System)
14	Port B (Front Mic)	4	Pin Complex	Front Panel Microphone/Headphone Jack
15	Port C (Line In)	4	Pin Complex	Rear Panel Line-In Jack
16	Port F (Surr Back)	4	Pin Complex	Rear Panel Surround-Rear (5.1) Jack
17	Port E (Rear Mic)	4	Pin Complex	Rear Panel Mic Jack
18	CD In	4	Pin Complex	Analog CD Input
19	Mixer Power Down	5	Power Widget	Powers Down the Analog Mixer and Associated Amps
1A	Analog PCBeep	4	Pin Complex	External Analog PCBeep Signal Input
1B	S/PDIF Out	4	Pin Complex	S/PDIF Output Pin
1E	Mono Out Mixer	2	Audio Mixer	Selects Which Source Drives the Mono Out Signal
1F	Digital Microphone	4	Pin Complex	Digital Microphone Interface
20	Analog Mixer	2	Audio Mixer	Mixes Individually Gainable Analog Inputs

Table 14. HD Audio Widgets (2 of 2)

Node ID	Name	Type ID	Type	Description
21	Mixer Output Atten	3	Audio Selector	Attenuates the Mixer Output to Drive the Port Mixers
22	Port A Mixer	2	Audio Mixer	Mixes the Port A Selected DAC and Mixer Output Amps to Drive Port A
23	VREF Power Down	F	Vendor Defined	Powers Down the Internal and External VREF Circuitry
24	Port G (C/LFE)	4	Pin Complex	Rear Panel C/LFE Jack
26	Port E Mixer	2	Audio Mixer	Mixes DAC1 and Mixer Output Amps to Drive Port E
27	Port G Mixer	2	Audio Mixer	Mixes DAC1 and Mixer Output Amps to Drive Port G
29	Port D Mixer	2	Audio Mixer	Mixes DAC0 and Mixer Output Amps to Drive Port D
2A	Port F Mixer	2	Audio Mixer	Mixes DAC2 and Mixer Output Amps to Drive Port F
2C	Port C Mixer	2	Audio Mixer	Mixes the Port C Selected DAC and Mixer Output Amps to Drive Port C
2D	Stereo Mix Down	2	Audio Mixer	Mixes the Stereo L/R Channels to Drive Mono Output
2F	BIAS Power Down	F	Vendor Defined	Powers Down the Internal MIC_BIAS_IN and all MIC_BIAS Pins
37	Port A Out Selector	3	Audio Selector	Selects the Port A DAC (0, 1)
39	Port B Boost	3	Audio Selector	Microphone Boost Amp for Port B
3A	Port C Boost	3	Audio Selector	Microphone Boost Amp for Port C
3C	Port E Boost	3	Audio Selector	Microphone Boost Amp for Port E

1.7 Default Configuration Bytes

In [Table 15](#), default configuration values are set on codec power-up only. Default configuration values are not reset by link or soft reset to preserve modifications by BIOS control.

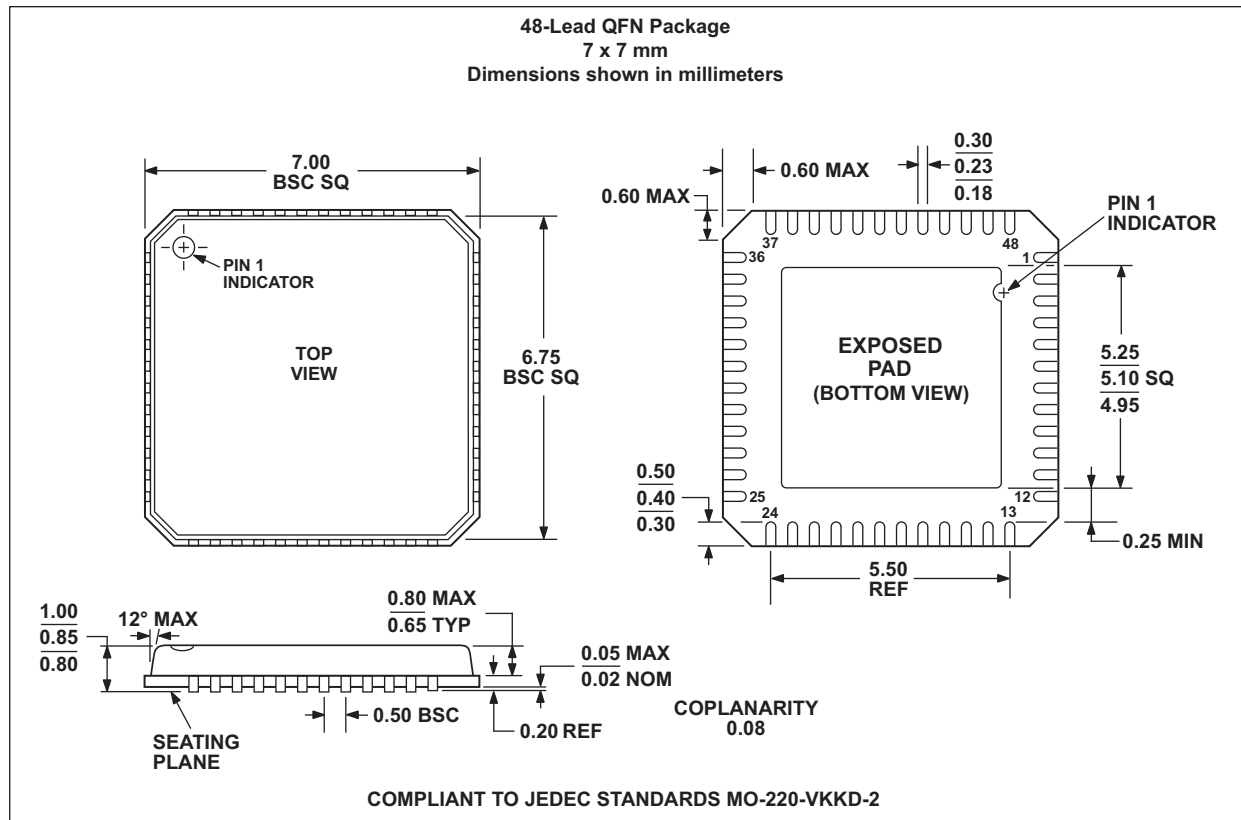
Table 15. Default Configuration Bytes

Name	Value	31:30	29:28	27:24	23:20	19:16	15:12	8	7:4	3:0
		Connectivity	Location		Def. Device	Conn Type	Color	Misc.	Def Assn	Sequence
			Chasis	Position				JD Over Ride		
Port A (Headphone)	0x0221 401F	Jack	External	Front	HP Out	1/8" Jack	Green	0	1	F
Port D (Front L/R)	0x0101 4010	Jack	External	Rear	Line Out	1/8" Jack	Green	0	1	0
Mono Out	0x9017 01F0	Fixed	Internal	N/A	Speaker	Other Analog	Unknown	1	F	0
Port B (Front Mic)	0x02A1 90F0	Jack	External	Front	Mic In	1/8" Jack	Pink	0	F	0
Port C (Line In)	0x0181 3021	Jack	External	Rear	Line In	1/8" Jack	Blue	0	2	1
Port F (Surr Back)	0x0101 1012	Jack	External	Rear	Line Out	1/8" Jack	Black	0	1	2
Port E (Rear Mic)	0x01A1 9020	Jack	External	Rear	Mic In	1/8" Jack	Pink	0	2	0
CD IN	0x9933 012E	Fixed	Internal	Special 3	CD	ATAPI	Unknown	1	2	E
Analog PCBeep	0x90F7 01F0	Fixed	Internal	N/A	Other	Other Analog	Unknown	1	F	0
S/PDIF Out	0x0145 11F0	Jack	External	Rear	SPDIF Out	Optical	Black	1	F	0
Digital Microphone	0x97A6 09F0	Fixed	Internal	Special 1	Mic In	Other Digital	Unknown	1	F	0
Port G (C/LFE)	0x0101 6011	Jack	External	Rear	Line Out	1/8" Jack	Orange	0	1	1

1.8 Package Dimensions

Figure 4 provides the package dimensions, shown in millimeters

Figure 4. Package Dimensions



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