

TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (U-MOSIII)

2SK3843

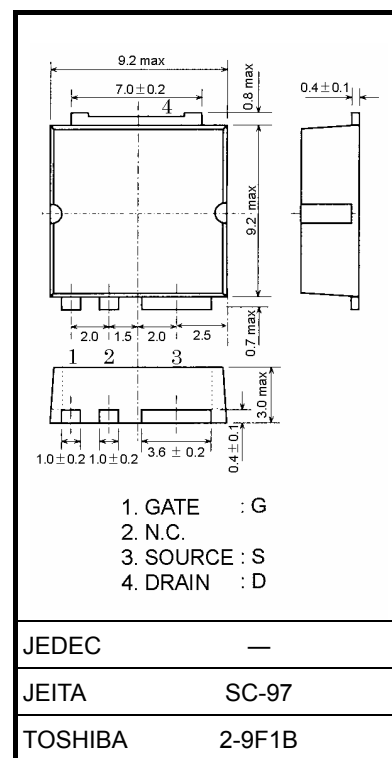
Switching Regulator, DC/DC Converter and Motor Drive Applications

Unit: mm

- Low drain-source ON resistance : $R_{DS(ON)} = 2.7 \text{ m}\Omega$ (typ.)
- High forward transfer admittance : $|Y_{fs}| = 120 \text{ S}$ (typ.)
- Low leakage current : $I_{DSS} = 10 \text{ }\mu\text{A}$ (max) ($V_{DS} = 40 \text{ V}$)
- Enhancement mode : $V_{th} = 1.5 \sim 3.0 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$)

Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	40	V
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	V_{DGR}	40	V
Gate-source voltage	V_{GSS}	± 20	V
Drain current	DC (Note 1)	I_D	A
	Pulse (Note 1)	I_{DP}	A
Drain power dissipation ($T_c = 25^\circ\text{C}$)	P_D	125	W
Single-pulse avalanche energy (Note 2)	E_{AS}	542	mJ
Avalanche current	I_{AR}	75	A
Repetitive avalanche energy (Note 3)	E_{AR}	12.5	mJ
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature range	T_{stg}	$-55 \sim 150$	$^\circ\text{C}$



Weight: 0.74 g (typ.)

Thermal Characteristics

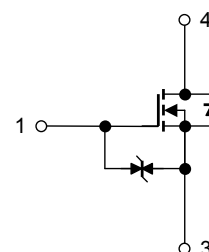
Characteristic	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	1.0	$^\circ\text{C/W}$

Note 1: Ensure that the channel temperature does not exceed 150°C .

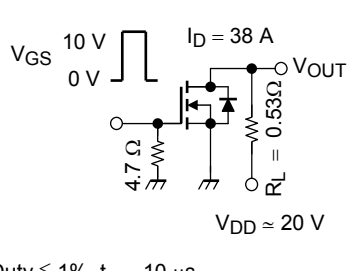
Note 2: $V_{DD} = 25 \text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 100 \text{ }\mu\text{H}$, $I_{AR} = 75 \text{ A}$, $R_G = 25 \text{ }\Omega$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature.

This transistor is an electrostatic-sensitive device. Handle with care.



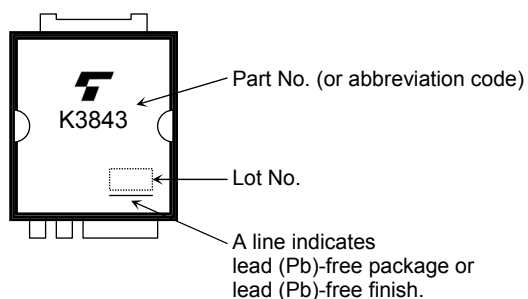
Electrical Characteristics (Ta = 25°C)

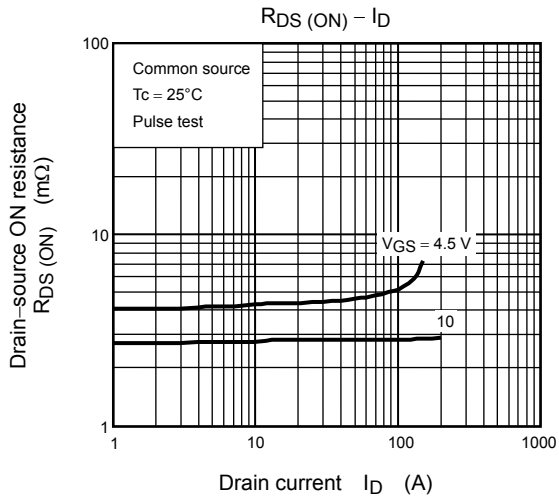
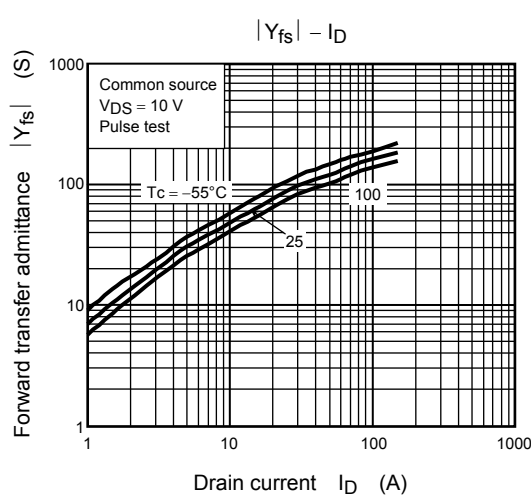
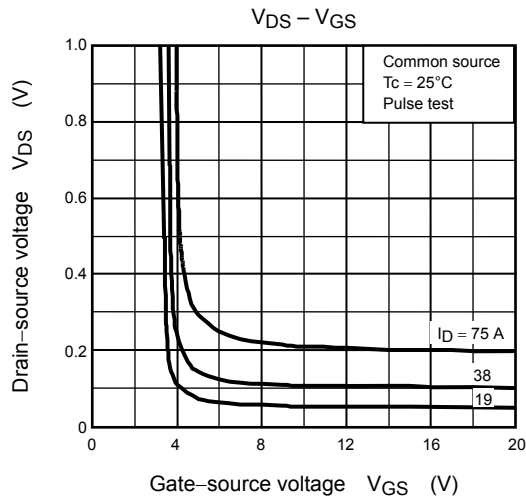
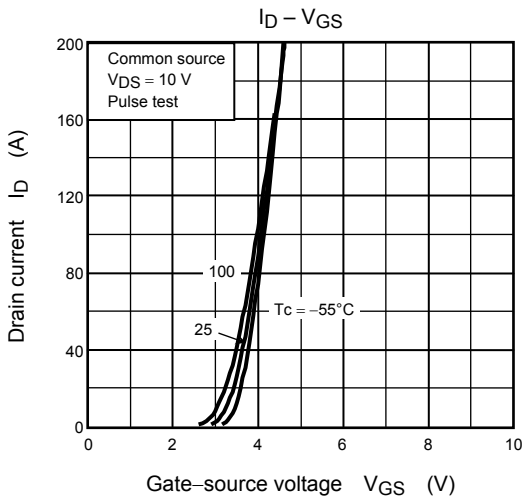
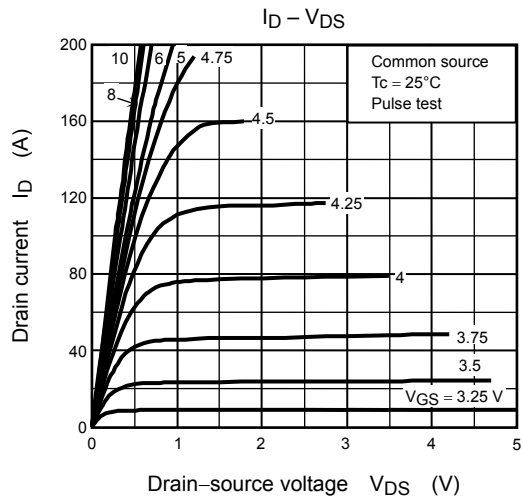
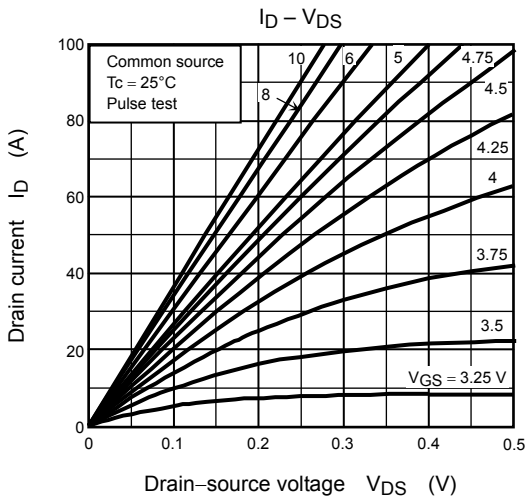
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V	—	—	±10	μA
Drain cutoff current		I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	—	—	10	μA
Drain–source breakdown voltage		V _{(BR) DSS}	I _D = 10 mA, V _{GS} = 0 V	40	—	—	V
		V _{(BR) DSX}	I _D = 10 mA, V _{GS} = –20 V	15	—	—	
Gate threshold voltage		V _{th}	V _{DS} = 10 V, I _D = 1 mA	1.5	—	3.0	V
Drain–source ON resistance		R _{DS (ON)}	V _{GS} = 4.5 V, I _D = 38 A	—	4.3	8.0	mΩ
			V _{GS} = 10 V, I _D = 38 A	—	2.7	3.5	
Forward transfer admittance		Y _{fs}	V _{DS} = 10 V, I _D = 38 A	60	120	—	S
Input capacitance		C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	—	11200	—	pF
Reverse transfer capacitance		C _{rss}		—	800	—	
Output capacitance		C _{oss}		—	1350	—	
Switching time	Rise time	t _r	 V _{DD} ≈ 20 V Duty ≤ 1%, t _W = 10 μs	—	12	—	ns
	Turn-on time	t _{on}		—	40	—	
	Fall time	t _f		—	65	—	
	Turn-off time	t _{off}		—	260	—	
Total gate charge (gate–source plus gate–drain)		Q _g	V _{DD} ≈ 32 V, V _{GS} = 10 V, I _D = 75 A	—	210	—	nC
Gate–source charge		Q _{gs}		—	150	—	
Gate–drain (“Miller”) Charge		Q _{gd}		—	60	—	

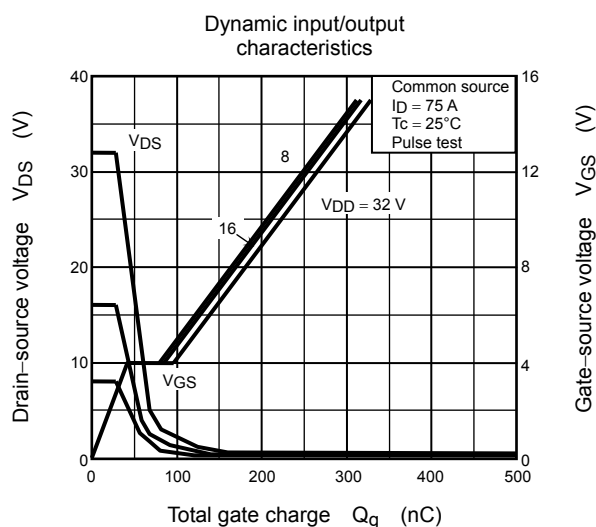
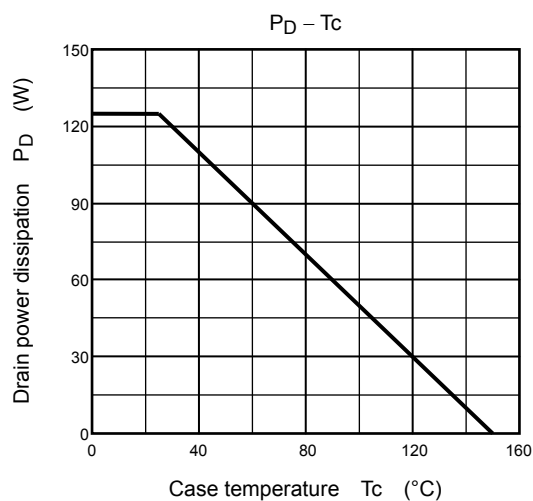
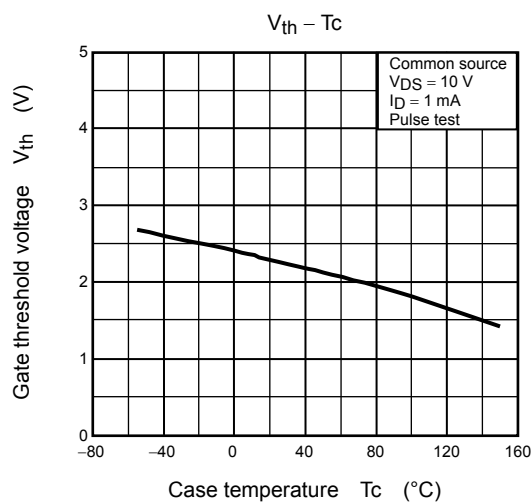
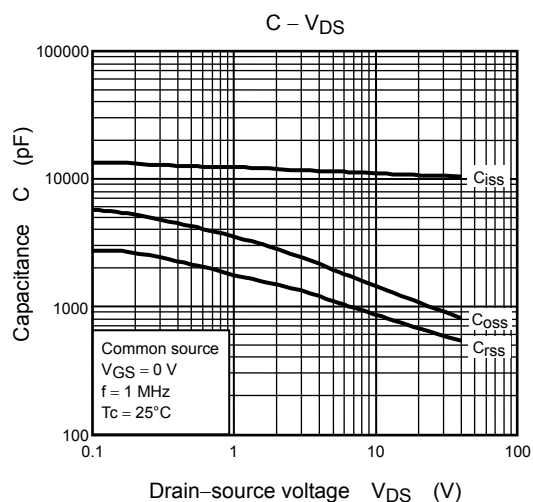
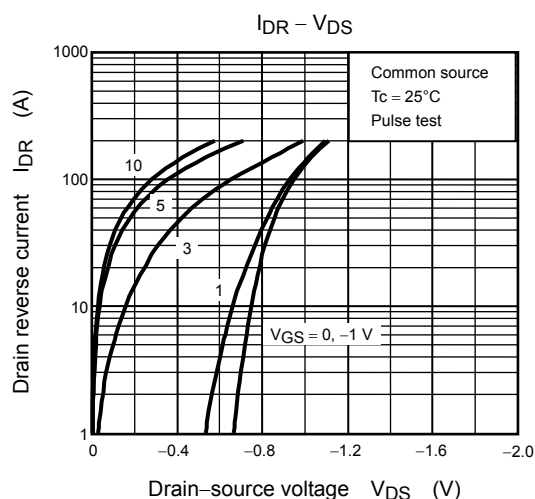
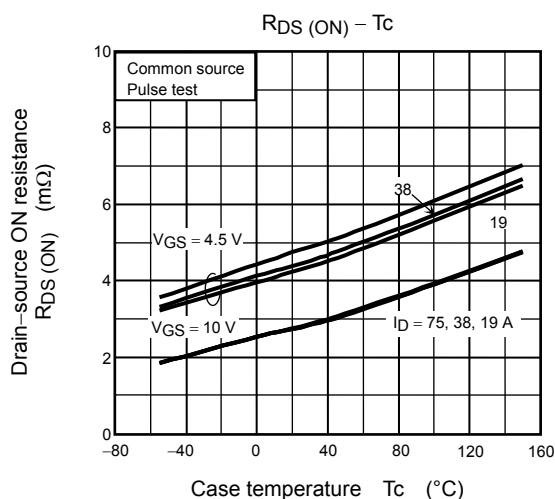
Source–Drain Ratings and Characteristics (Ta = 25°C)

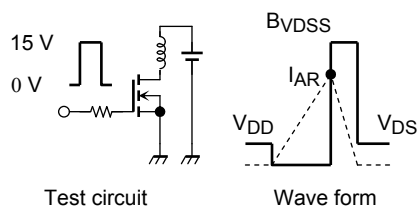
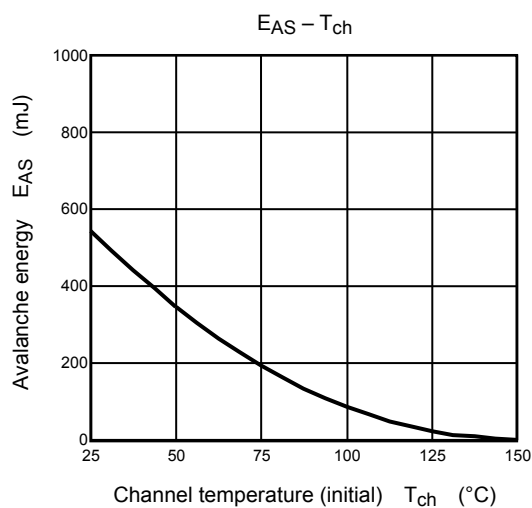
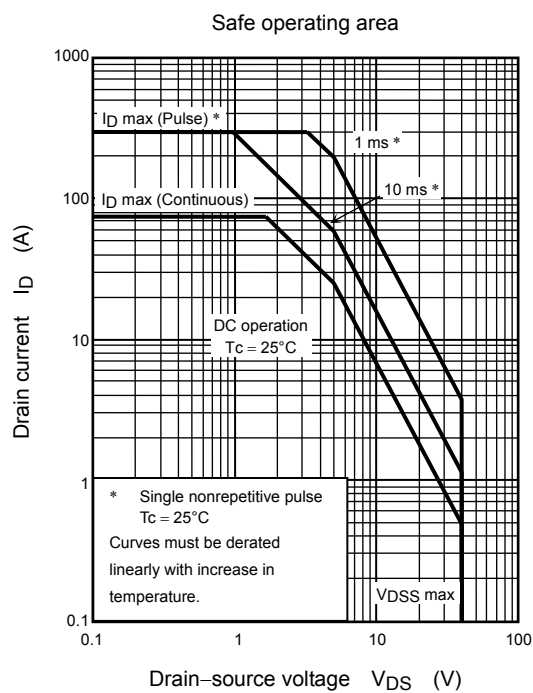
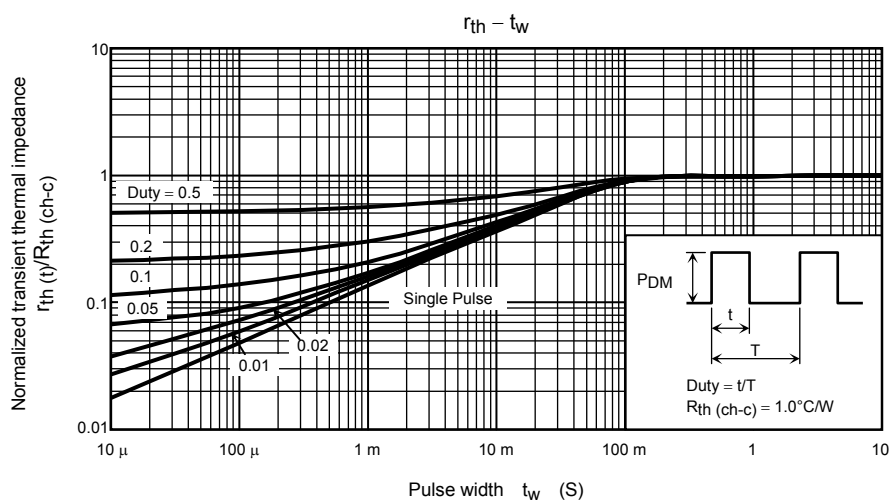
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	75	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	300	A
Forward voltage (diode)	V_{DSF}	$I_{DR1} = 75 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	–1.5	V
Reverse recovery time	t_{rr}	$I_{DR} = 75 \text{ A}, V_{GS} = 0 \text{ V}$	—	100	—	ns
Reverse recovery charge	Q_{rr}	$dI_{DR}/dt = 30 \text{ A}/\mu\text{s}$	—	120	—	nC

Marking









$$R_G = 25 \, \Omega$$

$$V_{DD} = 25 \, \text{V}, L = 100 \, \mu\text{H}$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2 \cdot \left(\frac{BVDSS}{BVDSS - V_{DD}} \right)$$

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