LMV331-N Single / LMV393-N Dual / LMV339-N Quad General Purpose, Low Voltage, Tiny Pack Comparators

Check for Samples: LMV331-N, LMV339-N, LMV393-N

FEATURES

- **(For 5V Supply, Typical Unless Otherwise Noted)**
- **Guaranteed 2.7V and 5V Performance**
- **Industrial Temperature Range −40°C to +85°C**
- **Low Supply Current 60 µA/Channel**
- **Input Common Mode Voltage Range Includes Ground**
- **Low Output Saturation Voltage 200 mV**
- **Propagation Delay 200 ns**
- **Space Saving 5-pin SC70 and 5-Pin SOT23 Packages**

APPLICATIONS

- **Mobile Communications**
- **Notebooks and PDA's**
- **Battery Powered Electronics**
- **General Purpose Portable Device**
- **General Purpose Low Voltage Applications**

DESCRIPTION

The LMV393-N and LMV339-N are low voltage (2.7-5V) versions of the dual and quad comparators, LM393/339, which are specified at 5-30V. The LMV331-N is the single version, which is available in space saving 5-pin SC70 and 5-pin SOT23 packages. The 5-pin SC70 is approximately half the size of the 5-pin SOT23.

The LMV393-N is available in 8-pin SOIC and VSSOP. The LMV339-N is available in 14-pin SOIC and TSSOP.

The LMV331-N/393-N/339-N is the most cost-effective solution where space, low voltage, low power and price are the primary specification in circuit design for portable consumer products. They offer specifications that meet or exceed the familiar LM393/339 at a fraction of the supply current.

The chips are built with TI's advanced Submicron Silicon-Gate BiCMOS process. The LMV331-N/393-N/339-N have bipolar input and output stages for improved noise performance.

Typical Applications

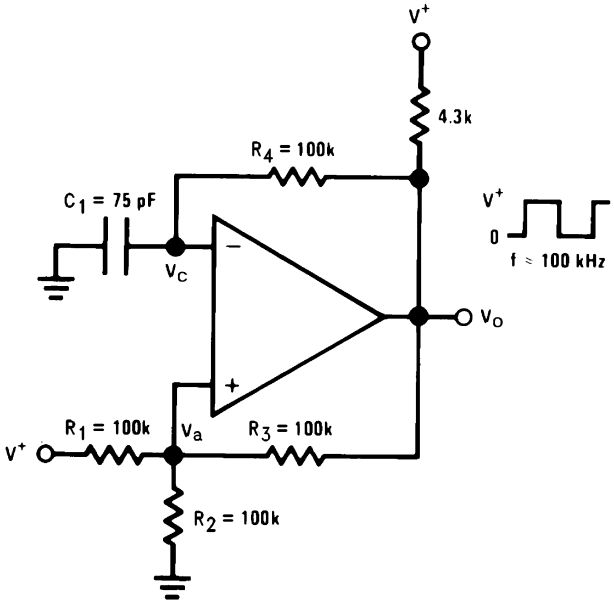
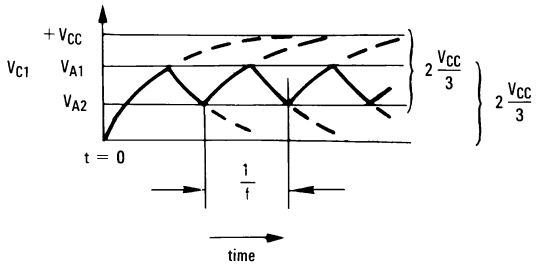


Figure 1. Squarewave Oscillator



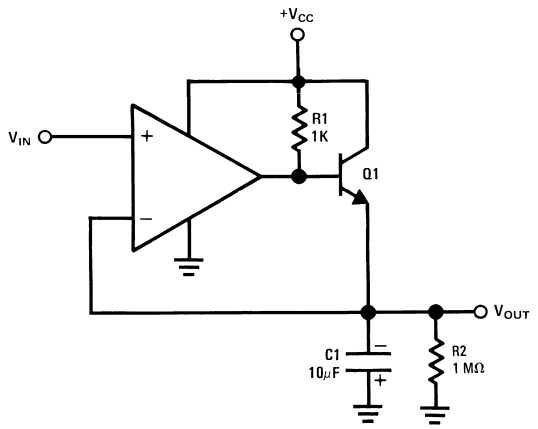


Figure 2. Positive Peak Detector

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Body Model	
LMV331-N/393-N/339-N	800V
Machine Model LMV331-N/339-N/393-N	120V
Differential Input Voltage	±Supply Voltage
Voltage on any pin (referred to V^- pin)	5.5V
Soldering Information	
Infrared or Convection (20 sec)	235°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (4)	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.
(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings (1)

Supply Voltage	2.7V to 5.0V
Temperature Range (2)	
LMV393-N. LMV339-N, LMV331-N	−40°C to +85°C
Thermal Resistance (θ_{JA})	
5-Pin SC70	478°C/W
5-Pin SOT23	265°C/W
8-Pin SOIC	190°C/W
8-Pin VSSOP	235°C/W
14-Pin SOIC	145°C/W
14-Pin TSSOP	155°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			1.7	7	mV
TCV_{OS}	Input Offset Voltage Average Drift			**5**		µV/°C
I_B	Input Bias Current			10	250 **400**	nA
I_{OS}	Input Offset Current			5	50 **150**	nA

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

2.7V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{CM}	Input Voltage Range			−0.1		V
				2.0		V
V_{SAT}	Saturation Voltage	I_{SINK} ≤ 1 mA		120		mV
I_O	Output Sink Current	V_O ≤ 1.5V	5	23		mA
I_S	Supply Current	LMV331-N		40	100	µA
		LMV393-N Both Comparators		70	140	µA
		LMV339-N All four Comparators		140	200	µA
	Output Leakage Current			.003	**1**	µA

2.7V AC Electrical Characteristics

T_J = 25°C, V^+ = 2.7V, R_L = 5.1 kΩ, V^- = 0V.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 10 mV		1000		ns
		Input Overdrive = 100 mV		350		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 10 mV		500		ns
		Input Overdrive = 100 mV		400		ns

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	max (1)	Units
V_{OS}	Input Offset Voltage			1.7	7 **9**	mV
TCV_{OS}	Input Offset Voltage Average Drift			5		µV/°C
I_B	Input Bias Current			25	250 **400**	nA
I_{OS}	Input Offset Current			2	50 **150**	nA
V_{CM}	Input Voltage Range			−0.1		V
				4.2		V
A_V	Voltage Gain		20	50		V/mV
V_{sat}	Saturation Voltage	I_{SINK} ≤ 4 mA		200	400 **700**	mV
I_O	Output Sink Current	V_O ≤ 1.5V		84	10	mA

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	max (1)	Units
I_S	Supply Current	LMV331-N		60	120 **150**	µA
		LMV393-N Both Comparators		100	200 **250**	µA
		LMV339-N All four Comparators		170	300 **350**	µA
	Output Leakage Current			.003	**1**	µA

5V AC Electrical Characteristics

T_J = 25°C, V^+ = 5V, R_L = 5.1 kΩ, V^- = 0V.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 10 mV		600		ns
		Input Overdrive = 100 mV		200		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 10 mV		450		ns
		Input Overdrive = 100 mV		300		ns

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C

Supply Current vs. Supply Voltage Output High (LMV331-N)

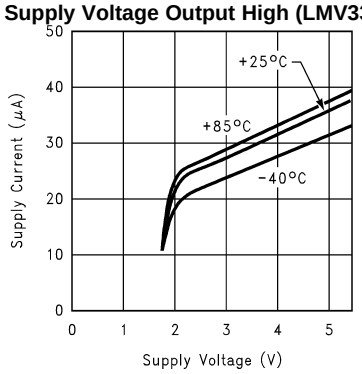


Figure 3.

Supply Current vs. Supply Voltage Output Low (LMV331-N)

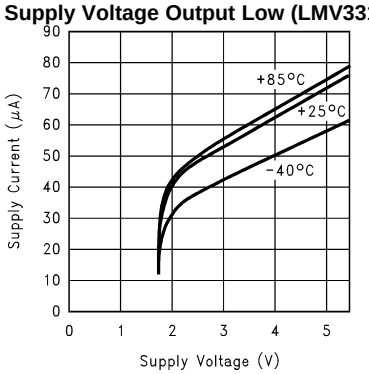


Figure 4.

Output Voltage vs. Output Current at 5V Supply

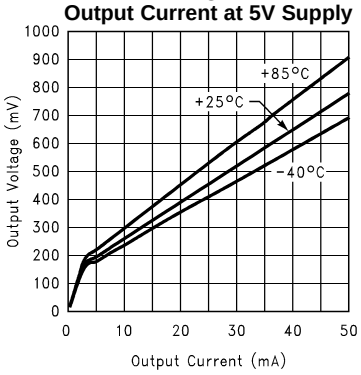


Figure 5.

Output Voltage vs. Output Current at 2.7 Supply

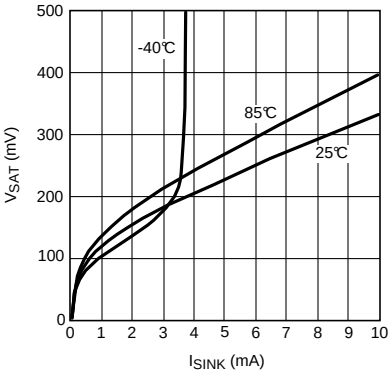


Figure 6.

Input Bias Current vs. Supply Voltage

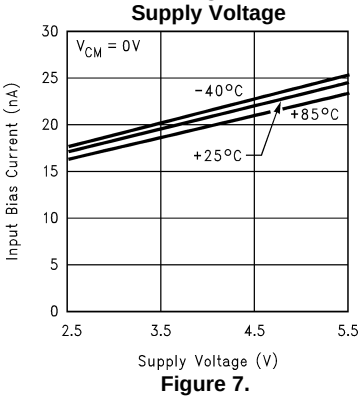


Figure 7.

Response Time vs. Input Overdrives Negative Transition

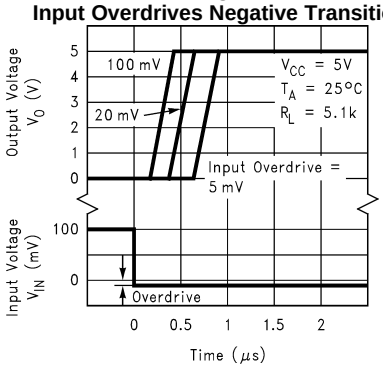


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C

Response Time for Input Overdrive Positive Transition

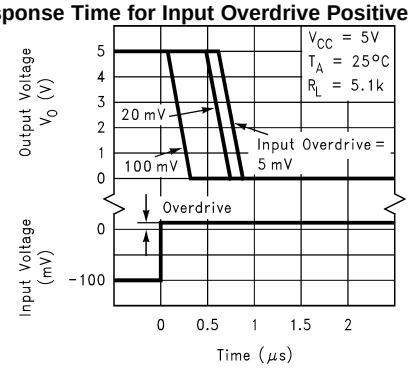


Figure 9.

Response Time vs. Input Overdrives Negative Transition

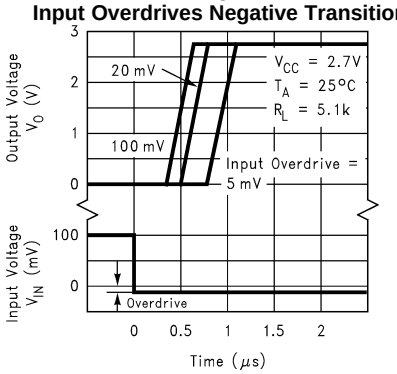


Figure 10.

Response Time for Input Overdrive Positive Transition

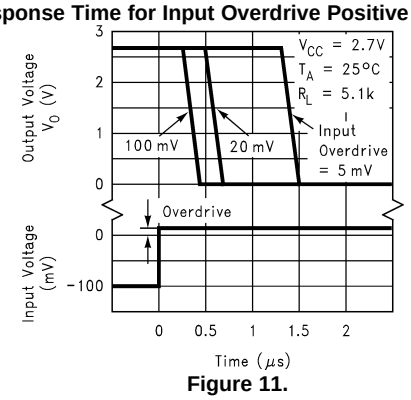
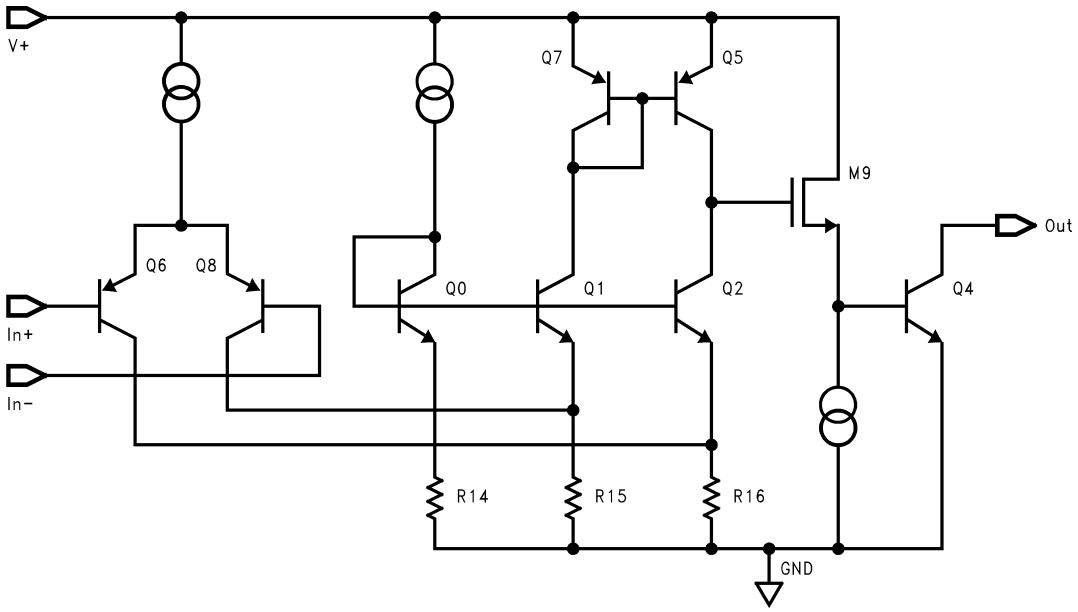


Figure 11.

SIMPLIFIED SCHEMATIC



APPLICATION CIRCUITS

BASIC COMPARATOR

A basic comparator circuit is used for converting analog signals to a digital output. The LMV331-N/393-N/339-N have an open-collector output stage, which requires a pull-up resistor to a positive supply voltage for the output to switch properly. When the internal output transistor is off, the output voltage will be pulled up to the external positive voltage.

The output pull-up resistor should be chosen high enough so as to avoid excessive power dissipation yet low enough to supply enough drive to switch whatever load circuitry is used on the comparator output. On the LMV331-N/393-N/339-N the pull-up resistor should range between 1k to 10kΩ.

The comparator compares the input voltage (V_{IN}) at the non-inverting pin to the reference voltage (V_{REF}) at the inverting pin. If V_{IN} is less than V_{REF}, the output voltage (V_O) is at the saturation voltage. On the other hand, if V_{IN} is greater than V_{REF}, the output voltage (V_O) is at V_{CC}.

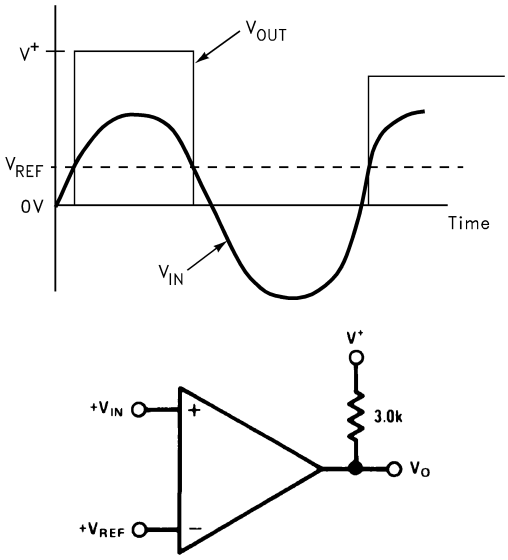


Figure 12. Basic Comparator

COMPARATOR WITH HYSTERESIS

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the comparator's switching threshold. This problem can be prevented by the addition of hysteresis or positive feedback.

INVERTING COMPARATOR WITH HYSTERESIS

The inverting comparator with hysteresis requires a three resistor network that are referenced to the supply voltage V_{CC} of the comparator. When V_{in} at the inverting input is less than V_a, the voltage at the non-inverting node of the comparator ($V_{in} < V_a$), the output voltage is high (for simplicity assume V_O switches as high as V_{CC}). The three network resistors can be represented as $R_1//R_3$ in series with R_2. The lower input trip voltage V_{a1} is defined as

$$V_{a_1} = \frac{V_{CC}\ R_2}{(R_1 \,||\, R_3) + R_2} \tag{1}$$

When V_{in} is greater than V_a ($V_{in} > V_a$), the output voltage is low very close to ground. In this case the three network resistors can be presented as $R_2//R_3$ in series with R_1. The upper trip voltage V_{a2} is defined as

$$V_{a2} = \frac{V_{CC}(R_2 // R_3)}{R_1 + (R_2 // R_3)} \tag{2}$$

The total hysteresis provided by the network is defined as

$$\Delta V_a = V_{a1} - V_{a2} \quad (3)$$

To assure that the comparator will always switch fully to V_{CC} and not be pulled down by the load the resistors values should be chosen as follow:

$$R_{PULL\text{-}UP} << R_{LOAD} \quad (4)$$

and $R_1 > R_{PULL\text{-}UP}$. (5)

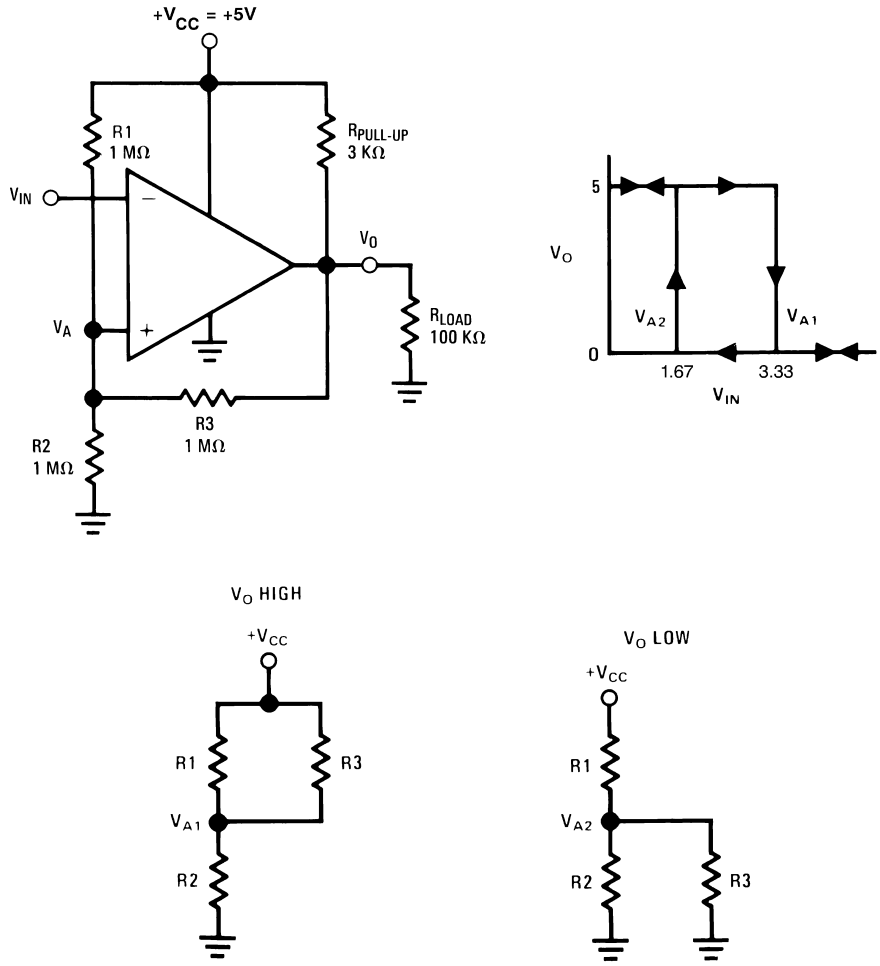


Figure 13. Inverting Comparator with Hysteresis

NON-INVERTING COMPARATOR WITH HYSTERESIS

Non inverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{ref}) at the inverting input. When V_{in} is low, the output is also low. For the output to switch from low to high, V_{in} must rise up to V_{in1} where V_{in1} is calculated by

$$V_{in1} = \frac{V_{ref}(R_1 + R_2)}{R_2} \quad (6)$$

When V_{in} is high, the output is also high, to make the comparator switch back to it's low state, V_{in} must equal V_{ref} before V_A will again equal V_{ref}. V_{in} can be calculated by:

$$V_{in2} = \frac{V_{ref}(R_1 + R_2) - V_{CC}R_1}{R_2} \quad (7)$$

The hysteresis of this circuit is the difference between V_{in1} and V_{in2}.

$$\Delta V_{in} = V_{CC}R_1/R_2 \quad (8)$$

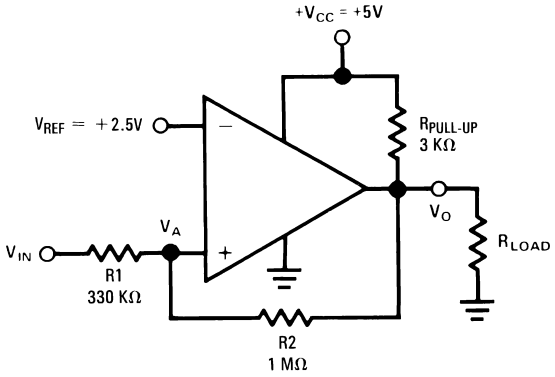


Figure 14.

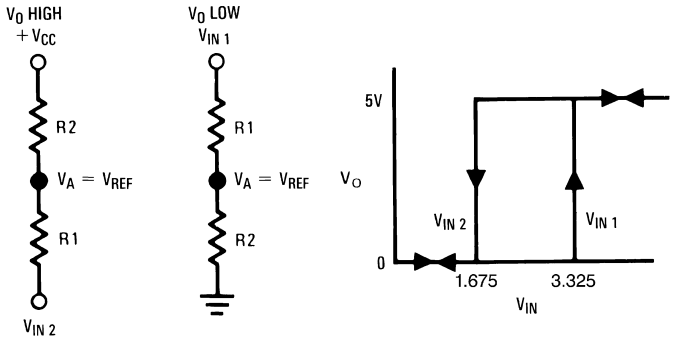


Figure 15.

SQUAREWAVE OSCILLATOR

Comparators are ideal for oscillator applications. This square wave generator uses the minimum number of components. The output frequency is set by the RC time constant of the capacitor C_1 and the resistor in the negative feedback R_4. The maximum frequency is limited only by the large signal propagation delay of the comparator in addition to any capacitive loading at the output, which would degrade the output slew rate.

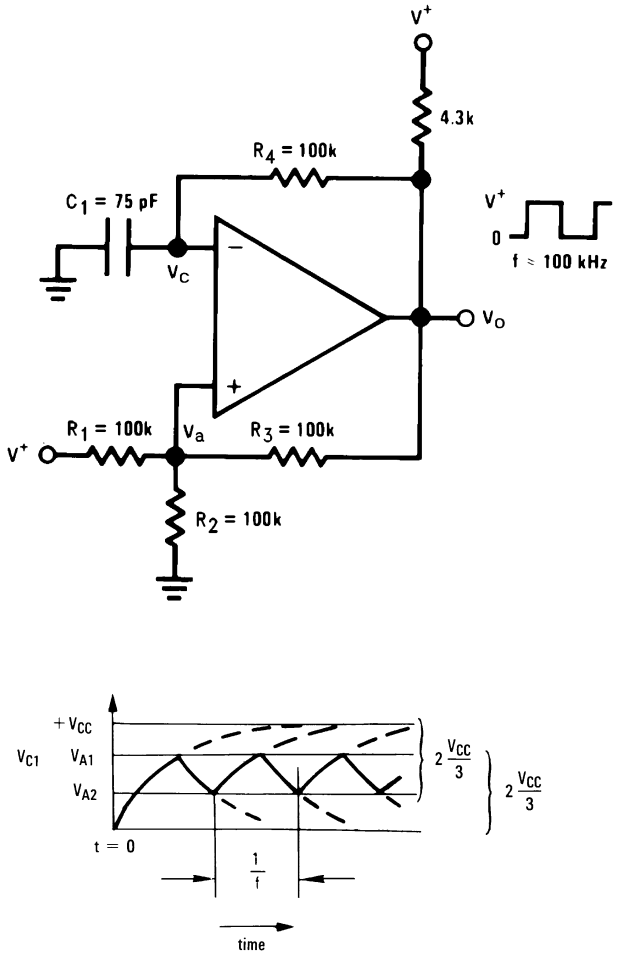


Figure 16. Squarewave Oscillator

To analyze the circuit, assume that the output is initially high. For this to be true, the voltage at the inverting input V_c has to be less than the voltage at the non-inverting input V_a. For V_c to be low, the capacitor C_1 has to be discharged and will charge up through the negative feedback resistor R_4. When it has charged up to value equal to the voltage at the positive input V_{a1}, the comparator output will switch.

V_{a1} will be given by:

$$V_{a1} = \frac{V_{CC} R_2}{R_2 + (R_1 // R_2)} \quad (9)$$

If:

$$R_1 = R_2 = R_3 \quad (10)$$

Then:

$$V_{a1} = 2V_{CC}/3 \quad (11)$$

When the output switches to ground, the value of V_a is reduced by the hysteresis network to a value given by:

$$V_{a2} = V_{CC}/3 \quad (12)$$

Capacitor C_1 must now discharge through R_4 towards ground. The output will return to its high state when the voltage across the capacitor has discharged to a value equal to V_{a2}.

For the circuit shown, the period for one cycle of oscillation will be twice the time it takes for a single RC circuit to charge up to one half of its final value. The time to charge the capacitor can be calculated from

$$V_C = V_{max}\ e^{\frac{-t}{RC}} \quad (13)$$

Where V_{max} is the max applied potential across the capacitor = ($2V_{CC}/3$)

and V_C = Vmax/2 = $V_{CC}/3$

One period will be given by:

$$1/freq = 2t \quad (14)$$

or calculating the exponential gives:

$$1/freq = 2(0.694)\ R_4\ C_1 \quad (15)$$

Resistors R_3 and R_4 must be at least two times larger than R_5 to insure that V_O will go all the way up to V_{CC} in the high state. The frequency stability of this circuit should strictly be a function of the external components.

FREE RUNNING MULTIVIBRATOR

A simple yet very stable oscillator that generates a clock for slower digital systems can be obtained by using a resonator as the feedback element. It is similar to the free running multivibrator, except that the positive feedback is obtained through a quartz crystal. The circuit oscillates when the transmission through the crystal is at a maximum, so the crystal in its series-resonant mode.

The value of R_1 and R_2 are equal so that the comparator will switch symmetrically about $+V_{CC}/2$. The RC constant of R_3 and C_1 is set to be several times greater than the period of the oscillating frequency, insuring a 50% duty cycle by maintaining a DC voltage at the inverting input equal to the absolute average of the output waveform.

When specifying the crystal, be sure to order series resonant with the desired temperature coefficient.

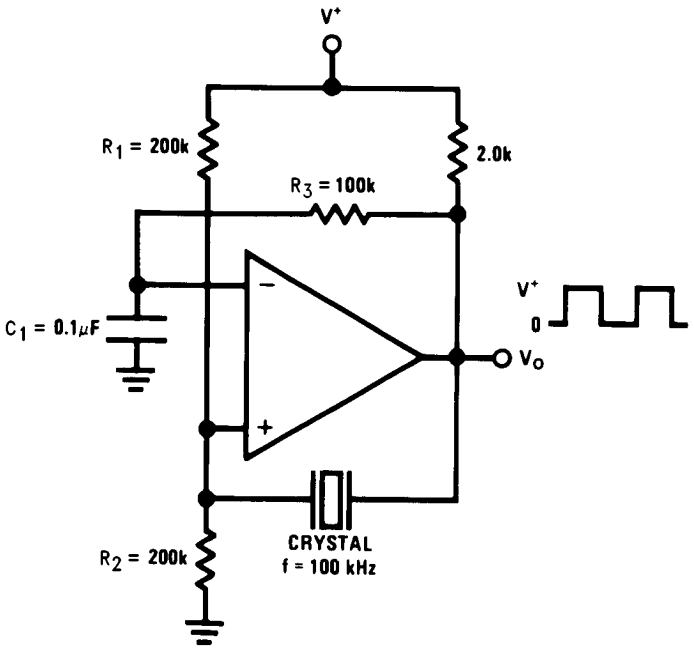


Figure 17. Crystal controlled Oscillator

PULSE GENERATOR WITH VARIABLE DUTY CYCLE

The pulse generator with variable duty cycle is just a minor modification of the basic square wave generator. Providing a separate charge and discharge path for capacitor C_1generates a variable duty cycle. One path, through R_2 and D_2 will charge the capacitor and set the pulse width (t_1). The other path, R_1 and D_1 will discharge the capacitor and set the time between pulses (t_2).

By varying resistor R_1, the time between pulses of the generator can be changed without changing the pulse width. Similarly, by varying R_2, the pulse width will be altered without affecting the time between pulses. Both controls will change the frequency of the generator. The pulse width and time between pulses can be found from:

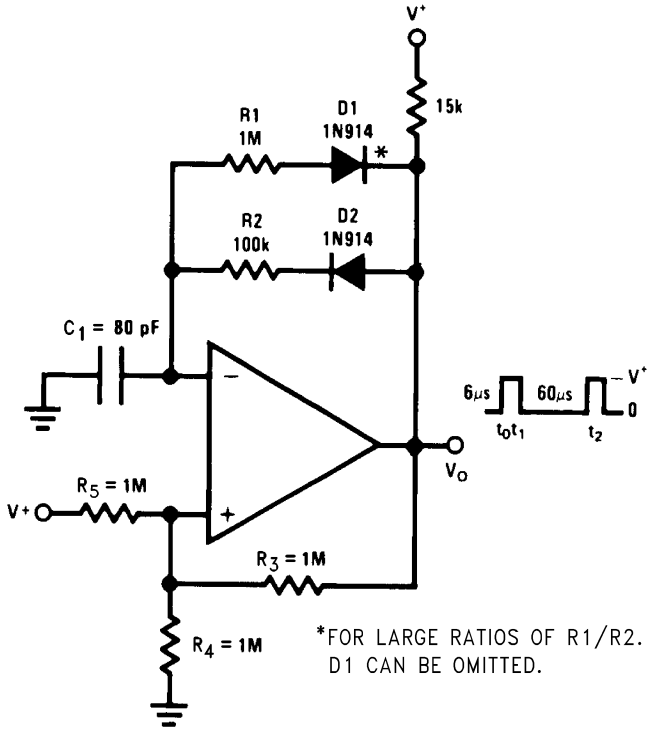


Figure 18. Pulse Generator

$$V_1 = V_{max}\left(1 - e^{-t_1/R_4C_1}\right) \quad \text{rise time}$$

$$V_1 = V_{max}\ e^{-t_2/R_5C_1} \quad \text{fall time}$$

Where

$$V_{max} = \frac{2\,V_{CC}}{3}$$

and

$$V_1 = \frac{V_{max}}{3} = \frac{V_{CC}}{3}$$

Which gives

$$\frac{1}{2} = e^{-t_1/R_4C_1}$$

t_2 is then given by:

$$\frac{1}{2} = e^{-t_2/R_5C_1} \tag{16}$$

Solving these equations for t_1 and t_2

$$t_1 = R_4C_1\ln 2 \tag{17}$$

$$t_2 = R_5C_1\ln 2 \tag{18}$$

These terms will have a slight error due to the fact that V_{max} is not exactly equal to 2/3 V_{CC} but is actually reduced by the diode drop to:

$$V_{max} = \frac{2}{3}\left(V_{CC} - V_{BE}\right) \tag{19}$$

$$\frac{1}{2(1 - V_{BE})} = e^{-t_1/R_4C_1} \quad (20)$$

$$\frac{1}{2(1 - V_{BE})} = e^{-t_2/R_5C_1} \quad (21)$$

POSITIVE PEAK DETECTOR

Positive peak detector is basically the comparator operated as a unit gain follower with a large holding capacitor from the output to ground. Additional transistor is added to the output to provide a low impedance current source. When the output of the comparator goes high, current is passed through the transistor to charge up the capacitor. The only discharge path will be the 1 MΩ resistor shunting C1 and any load that is connected to the output. The decay time can be altered simply by changing the 1 MΩ resistor. The output should be used through a high impedance follower to a avoid loading the output of the peak detector.

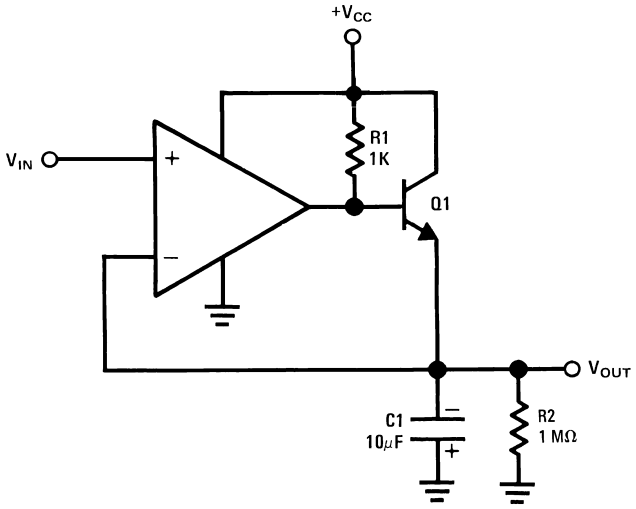


Figure 19. Positive Peak Detector

NEGATIVE PEAK DETECTOR

For the negative detector, the output transistor of the comparator acts as a low impedance current sink. The only discharge path will be the 1 MΩ resistor and any load impedance used. Decay time is changed by varying the 1 MΩ resistor.

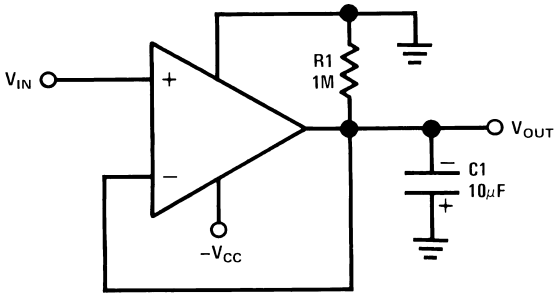


Figure 20. Negative Peak Detector

DRIVING CMOS AND TTL

The comparator's output is capable of driving CMOS and TTL Logic circuits.

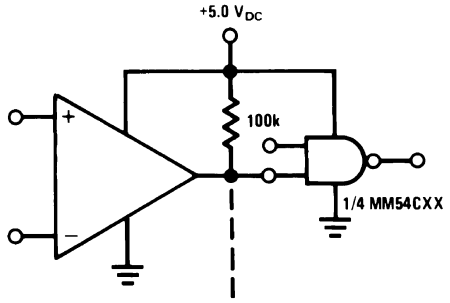


Figure 21. Driving CMOS

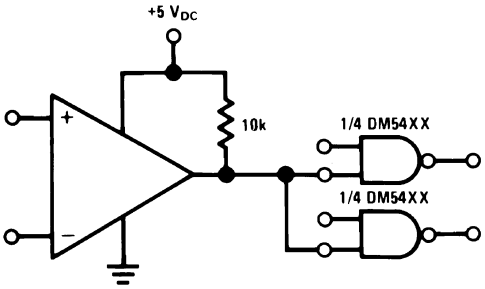


Figure 22. Driving TTL

AND GATES

The comparator can be used as three input AND gate. The operation of the gate is as follows:

The resistor divider at the inverting input establishes a reference voltage at that node. The non-inverting input is the sum of the voltages at the inputs divided by the voltage dividers. The output will go high only when all three inputs are high, casing the voltage at the non-inverting input to go above that at inverting input. The circuit values shown work for a "0" equal to ground and a "1" equal to 5V.

The resistor values can be altered if different logic levels are desired. If more inputs are required, diodes are recommended to improve the voltage margin when all but one of the inputs are high.

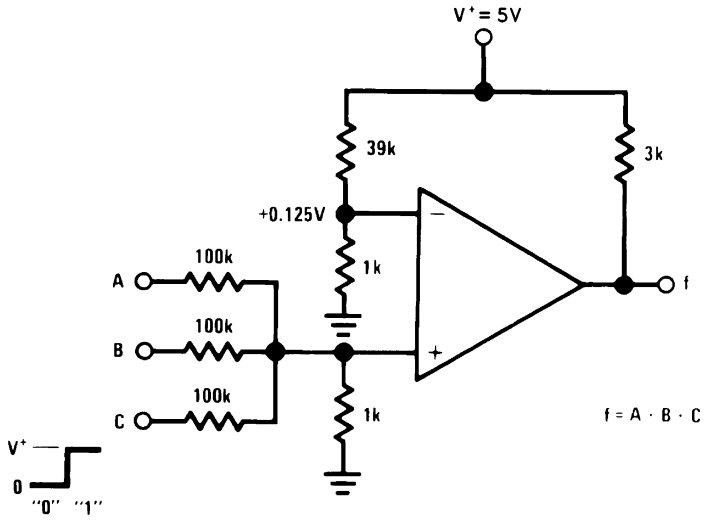


Figure 23. AND Gate

OR GATES

A three input OR gate is achieved from the basic AND gate simply by increasing the resistor value connected from the inverting input to V_{cc}, thereby reducing the reference voltage.

A logic "1" at any of the inputs will produce a logic "1" at the output.

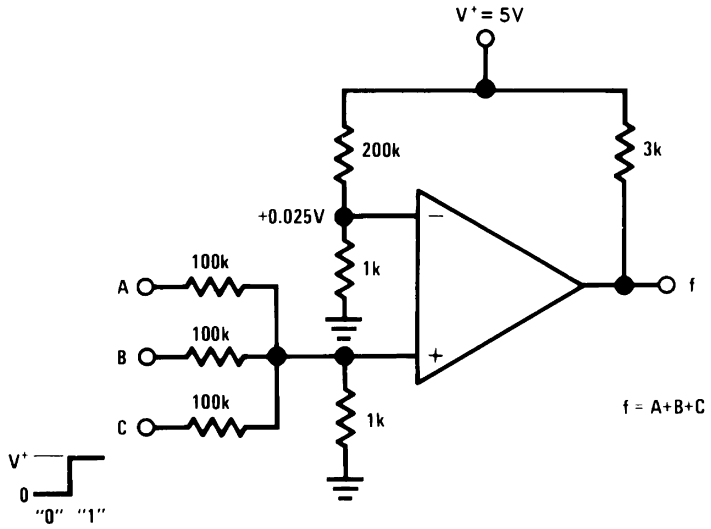


Figure 24. OR Gate

ORing THE OUTPUT

By the inherit nature of an open collector comparator, the outputs of several comparators can be tied together with a pull up resistor to V_{CC}. If one or more of the comparators outputs goes low, the output V_O will go low.

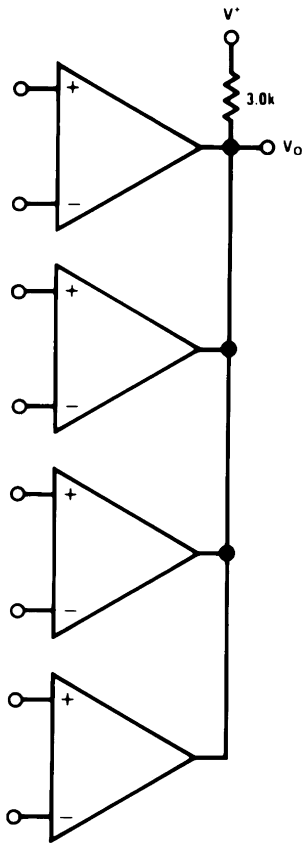


Figure 25. ORing the Outputs

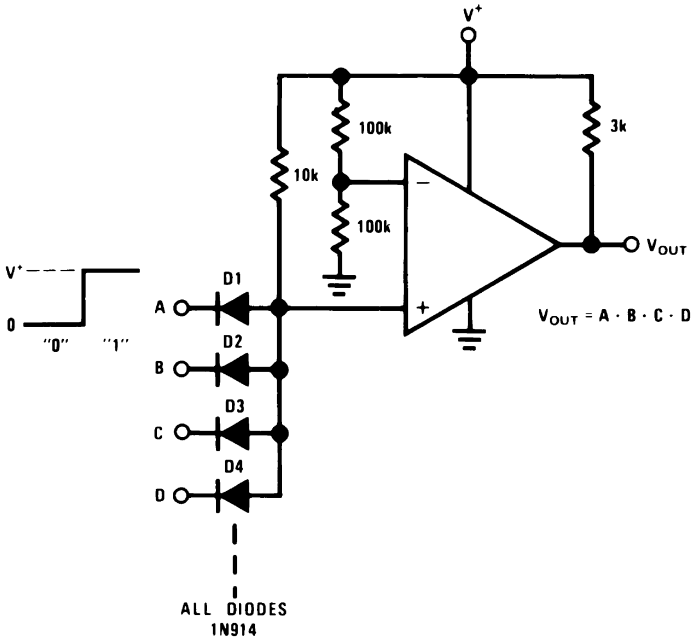


Figure 26. Large Fan-In AND Gate

Connection Diagram

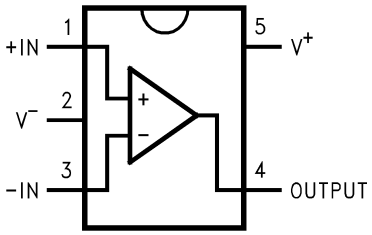


Figure 27. 5-Pin SC70/SOT23
Top View

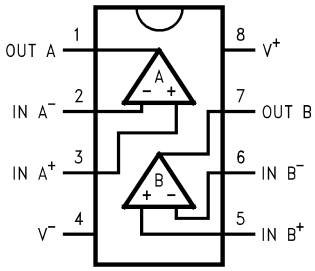


Figure 28. 8-Pin SOIC/VSSOP
Top View

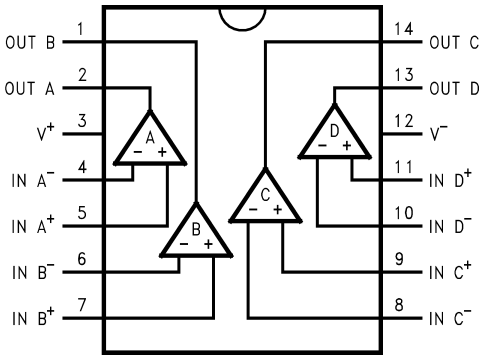


Figure 29. 14-Pin SOIC/TSSOP
Top View

REVISION HISTROY

Changes from Revision F (February 2013) to Revision G **Page**

- Changed layout of National Data Sheet to TI format 18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV331M5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	C12	
LMV331M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C12	Samples
LMV331M5X	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	C12	
LMV331M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C12	Samples
LMV331M7	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	C13	
LMV331M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C13	Samples
LMV331M7X	NRND	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 85	C13	
LMV331M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C13	Samples
LMV339M	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LMV339M	
LMV339M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV339M	Samples
LMV339MT	NRND	TSSOP	PW	14	94	TBD	Call TI	Call TI	-40 to 85	LMV339 MT	
LMV339MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV339 MT	Samples
LMV339MTX	NRND	TSSOP	PW	14	2500	TBD	Call TI	Call TI	-40 to 85	LMV339 MT	
LMV339MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV339 MT	Samples
LMV339MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV339M	Samples
LMV393M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMV 393M	
LMV393M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV 393M	Samples
LMV393MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	V393	
LMV393MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	V393	Samples
LMV393MMX	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 85	V393	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV393MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	V393	Samples
LMV393MX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMV 393M	
LMV393MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV 393M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

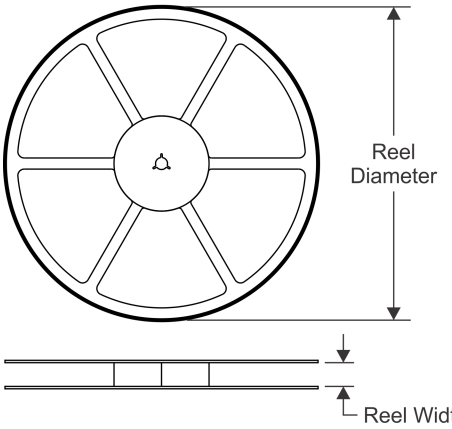
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

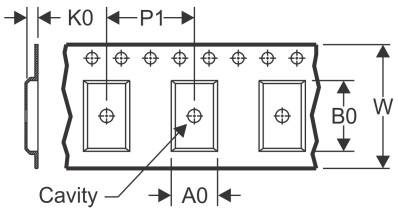
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

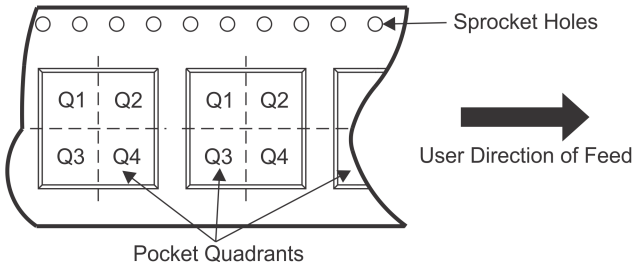


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

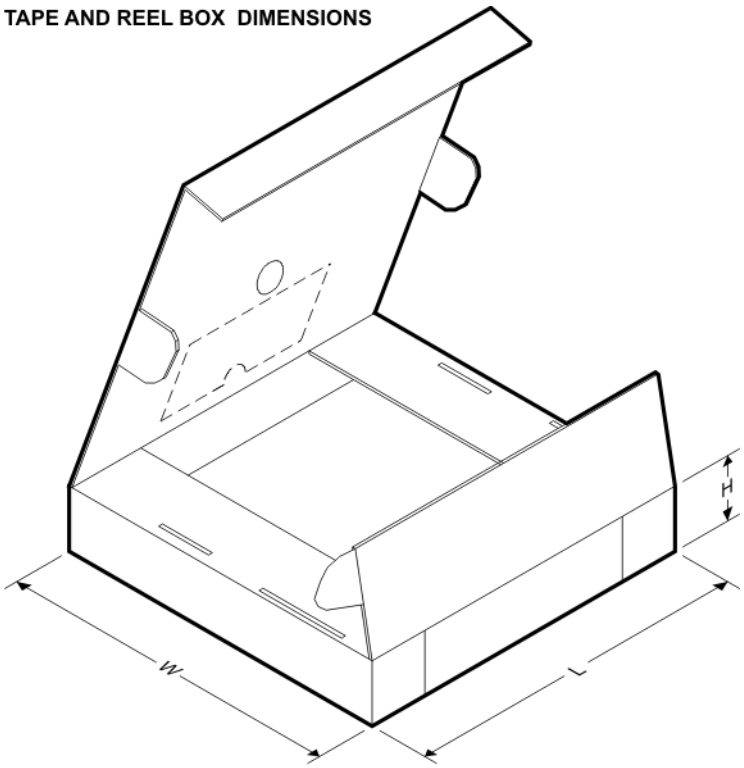
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV331M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV331M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV331M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV331M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV331M7X	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV331M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV339MTX	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LMV339MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LMV339MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV393MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV393MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV393MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV393MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV393MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV393MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

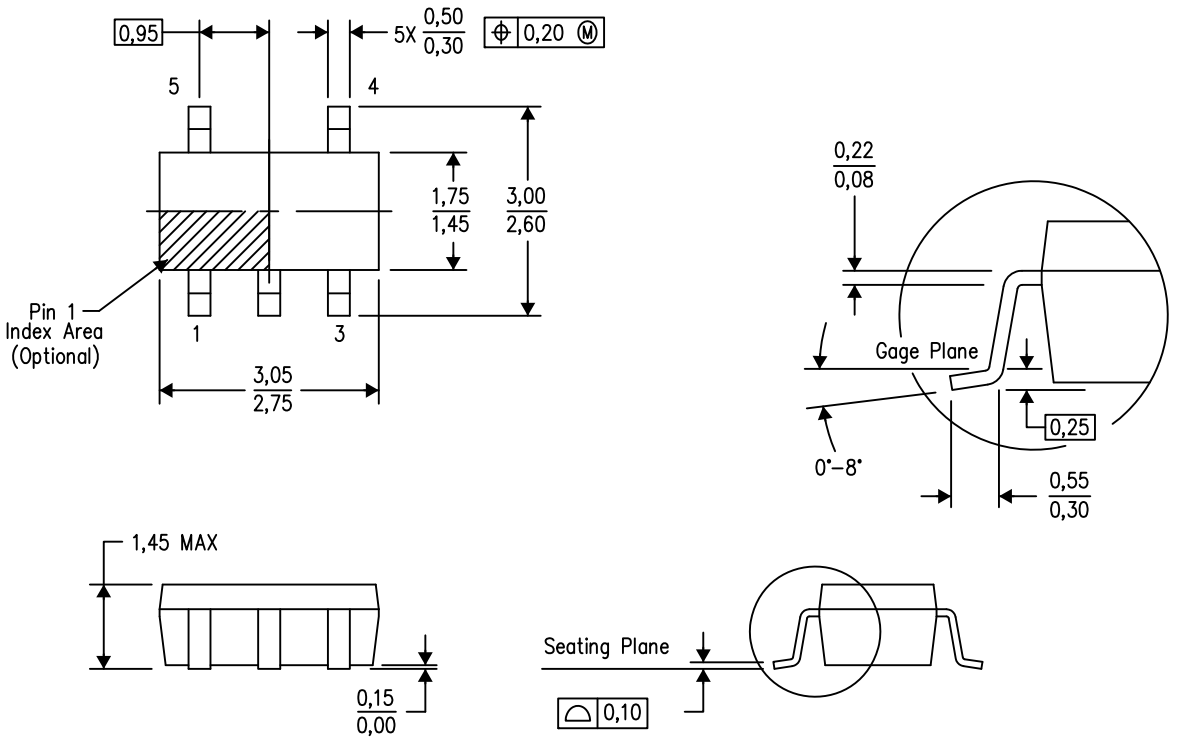
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV331M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV331M5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV331M7	SC70	DCK	5	1000	210.0	185.0	35.0
LMV331M7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV331M7X	SC70	DCK	5	3000	210.0	185.0	35.0
LMV331M7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV339MTX	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV339MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV339MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMV393MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV393MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV393MMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV393MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV393MX	SOIC	D	8	2500	367.0	367.0	35.0
LMV393MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

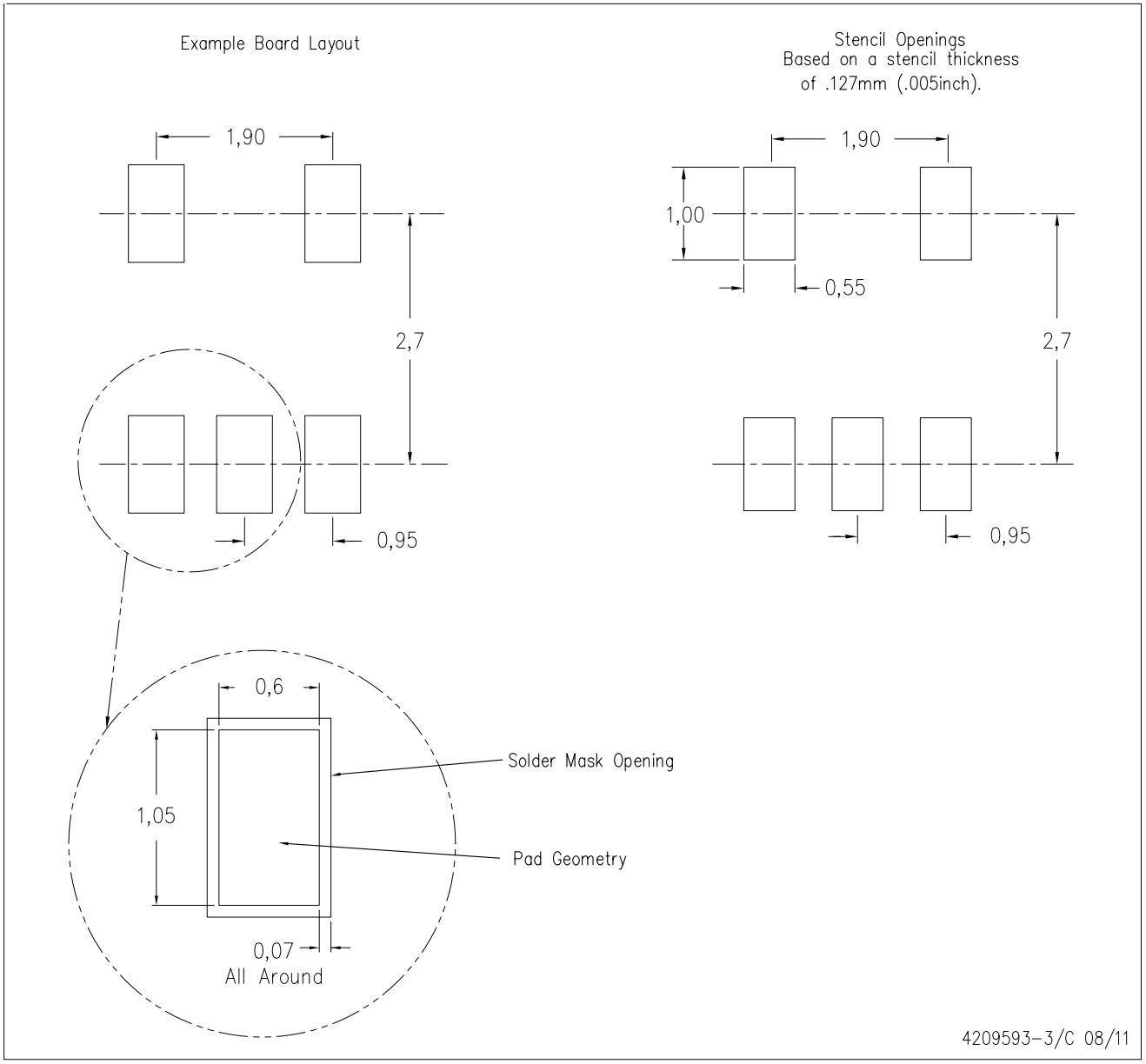
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

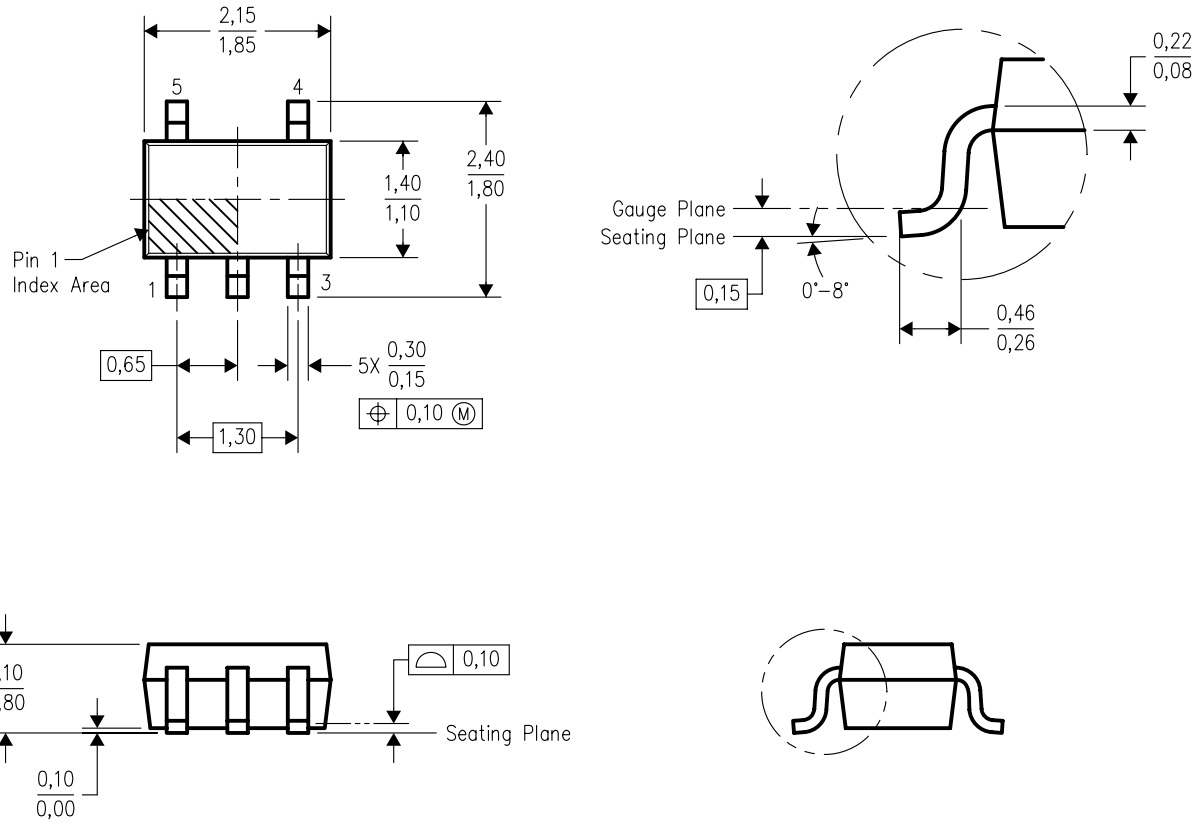
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

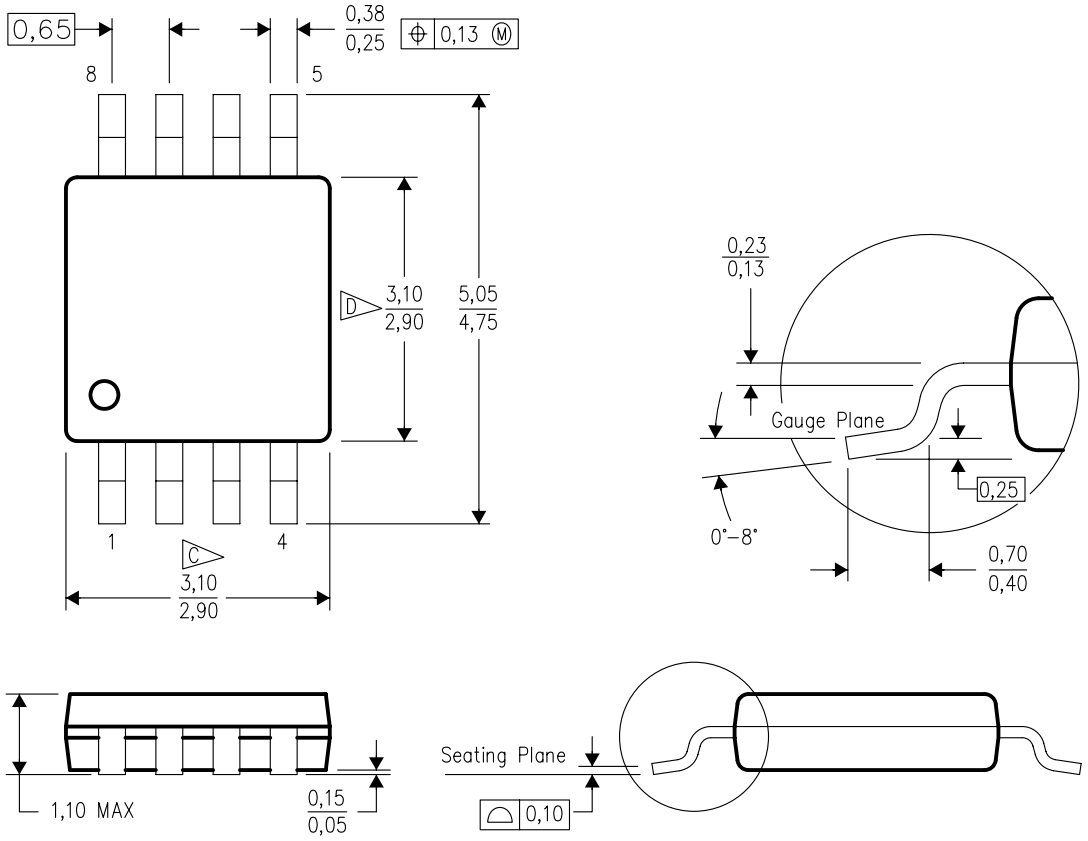
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

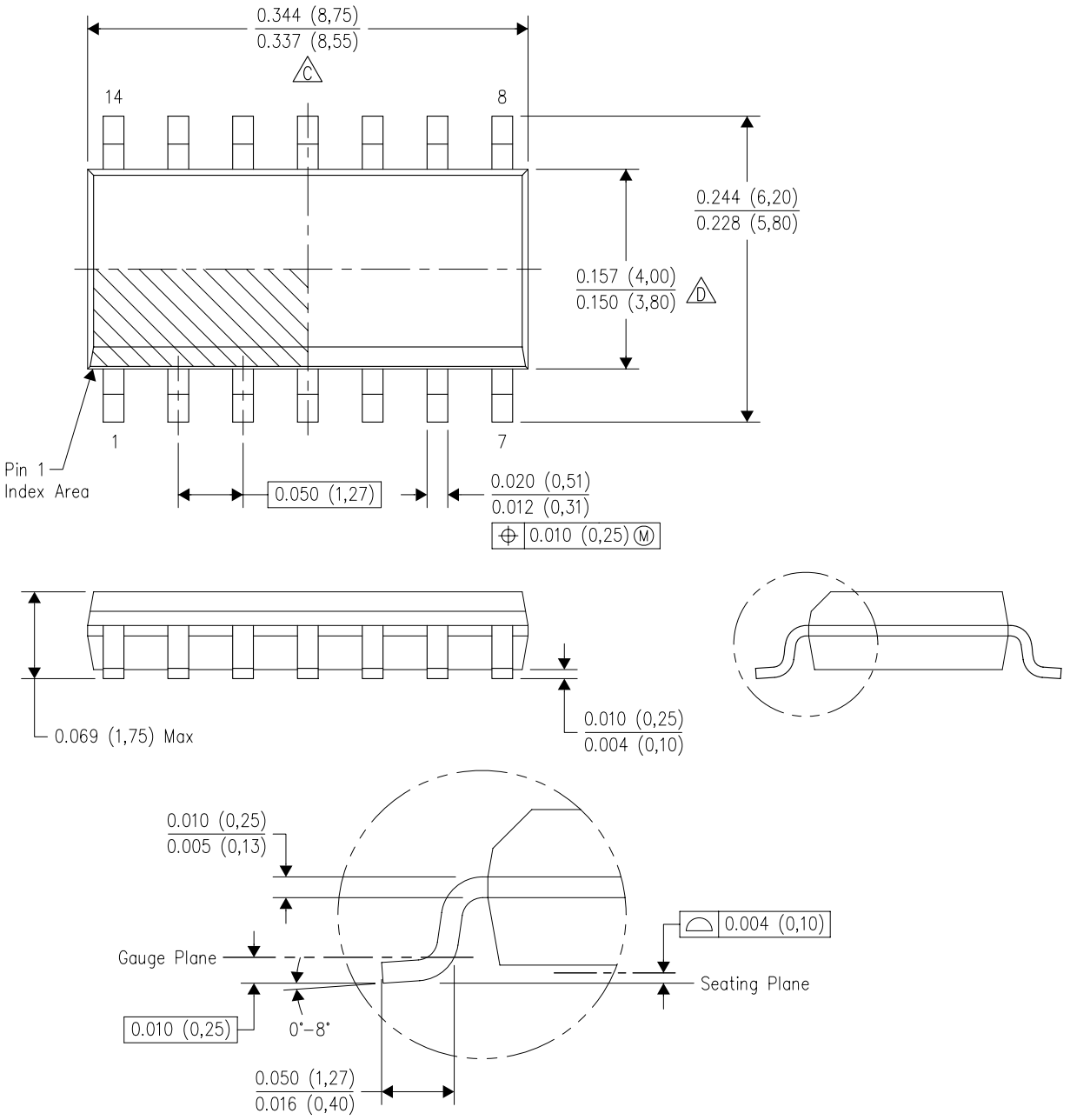
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

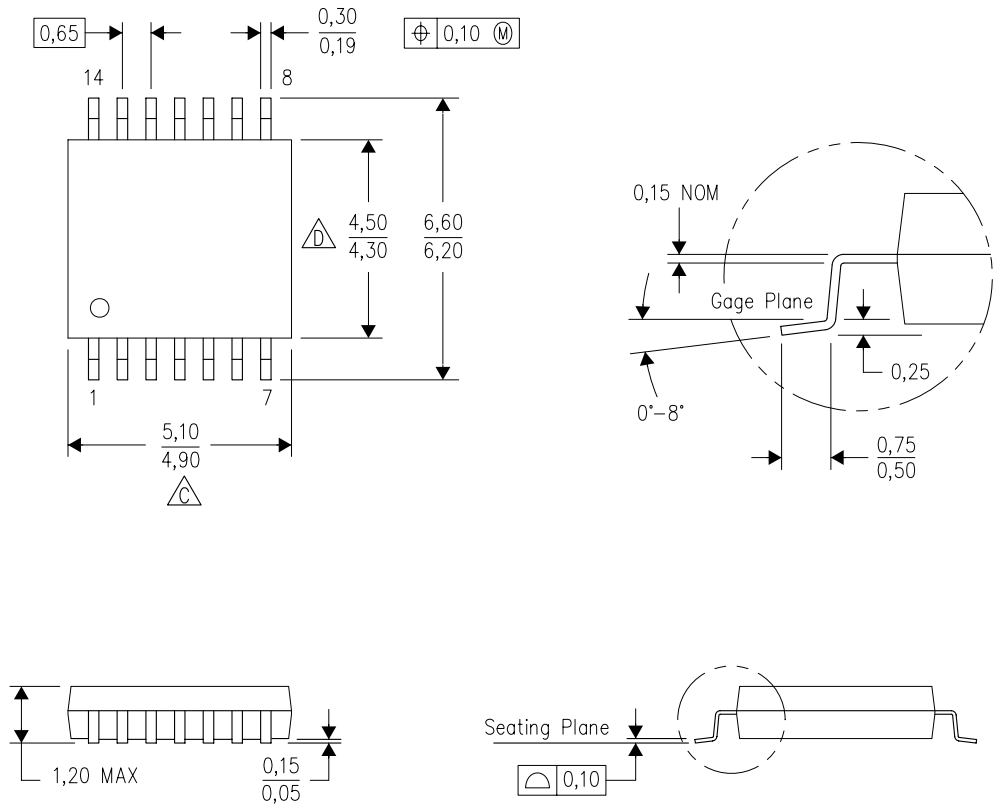
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

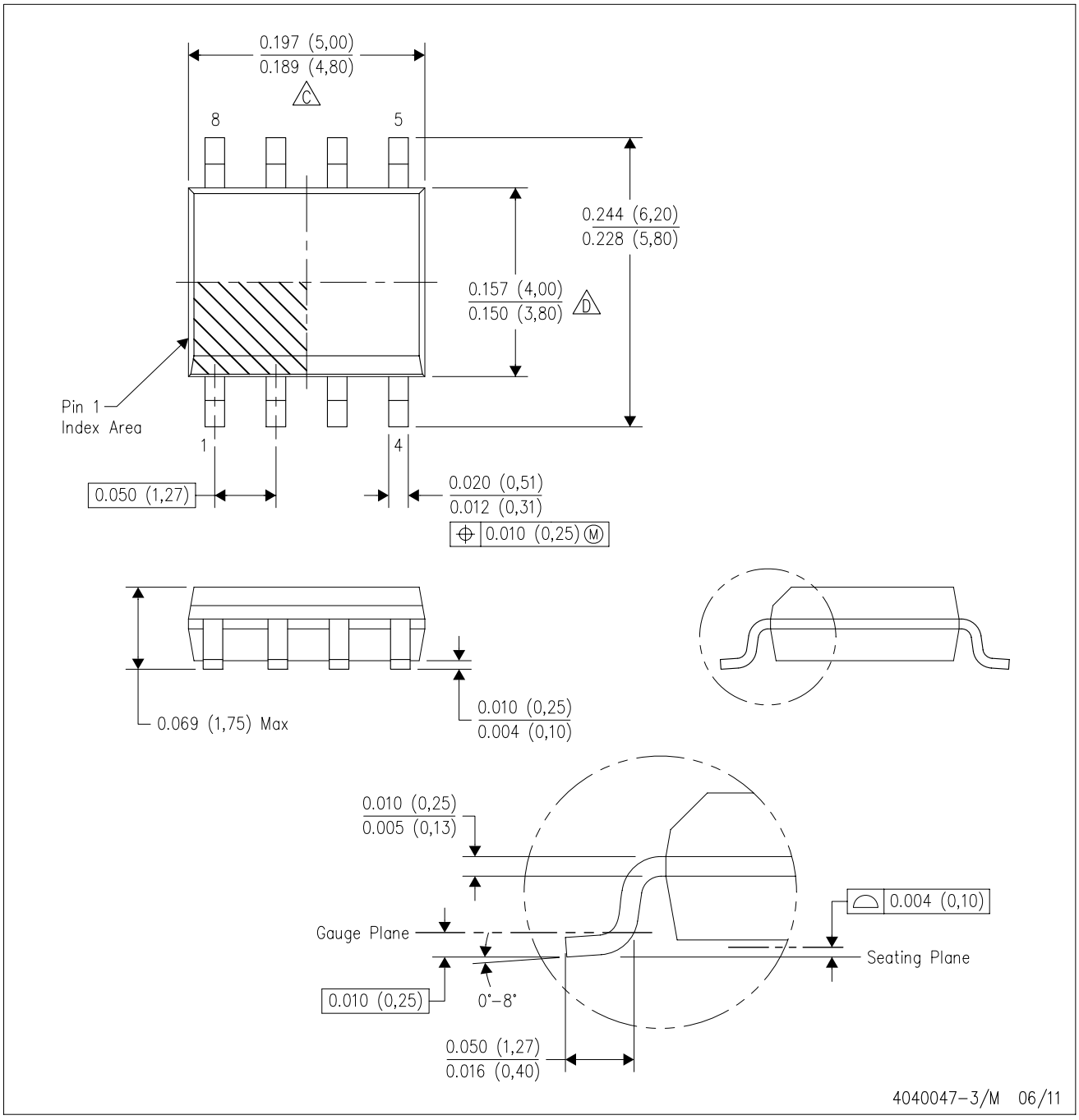
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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