- **Full Look Ahead for High-Speed Operations on Long Words**
- **Arithmetic Operating Modes:**
  - **Addition**
  - **Subtraction**
  - **Shift Operand A One Position**
  - **Magnitude Comparison**
  - **Twelve Other Arithmetic Operations**
- **Logic Function Modes:**
  - **Exclusive-OR**
  - **Comparator**
  - **AND, NAND, OR, NOR**
- **Package Options Include Plastic Small-Outline (N) Packages, Ceramic (FK) Chip Carriers, Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs, and Ceramic (JW) 600-mil DIPs**

SN54AS181B . . . JT OR JW PACKAGE
SN74AS181A . . . N OR NT PACKAGE
(TOP VIEW)

$\overline{B}0$	1	24	V_{CC}
$\overline{A}0$	2	23	$\overline{A}1$
S3	3	22	$\overline{B}1$
S2	4	21	$\overline{A}2$
S1	5	20	$\overline{B}2$
S0	6	19	$\overline{A}3$
C_n	7	18	$\overline{B}3$
M	8	17	$\overline{G}$
$\overline{F}0$	9	16	C_{n+4}
$\overline{F}1$	10	15	$\overline{P}$
$\overline{F}2$	11	14	A = B
GND	12	13	$\overline{F}3$
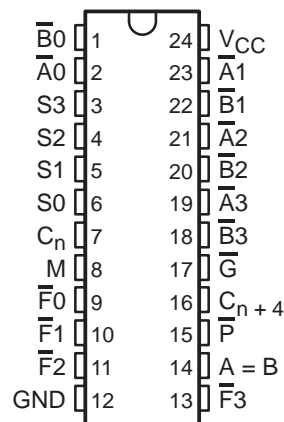
SN54AS181B . . . FK PACKAGE
(TOP VIEW)

NC – No internal connection

description

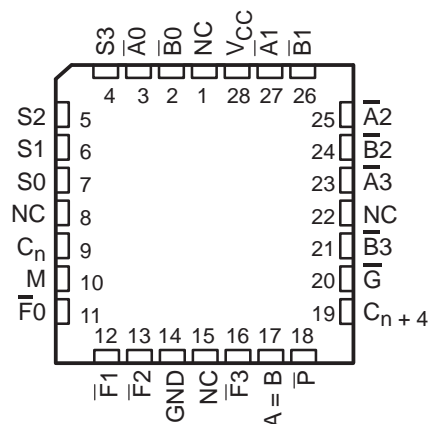The SN54AS181B and SN74AS181A arithmetic logic units (ALUs)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select (S0, S1, S2, and S3) lines and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries are enabled by applying a low-level voltage to the mode-control (M) input. A full carry look-ahead scheme is used to generate fast, simultaneous carry by means of two cascade ($\overline{G}$ and $\overline{P}$) outputs for the four bits in the package.

If high speed is not important, a ripple-carry (C_n) input and a ripple-carry (C_{n+4}) output are available. The ripple-carry delay is minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The SN54AS181B and SN74AS181A accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

Copyright © 1994, Texas Instruments Incorporated

TEXAS INSTRUMENTS

description (continued)

The SN54AS181B and SN74AS181A also can be used as comparators. The A = B output is internally decoded from the function (F0, F1, F2, F3) outputs so that when two words of equal magnitude are applied at the A and B inputs, the output assumes a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open collector so that it can be wire-AND connected to give a comparison for more than four bits. C_{n+4} also can be used to supply relative magnitude information. The ALU must be placed in the subtract mode by placing the function-select inputs S3, S2, S1, and S0 at L, H, H, and L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (Figure 1)	ACTIVE-HIGH DATA (Figure 2)
H	H	$A \geq B$	$A \leq B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leq B$	$A \geq B$

These circuits not only incorporate all of the designer's requirements for arithmetic operations, but also provide 16 possible functions of two Boolean variables without using external circuitry. These logic functions are selected by the four function-select inputs with M at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

TYPICAL ADDITION TIME
(C_L = 15 pF, R_L = 280 Ω, T_A = 25°C)

NUMBER OF BITS	ADDITION TIME USING 'S181 AND 'S182	PACKAGE COUNT		CARRY METHOD BETWEEN ALUs
		ALUs	LOOK-AHEAD CARRY GENERATORS	
1 to 4	11 ns	1		None
5 to 8	18 ns	2		Ripple
9 to 16	19 ns	3 or 4	1	Full look ahead
17 to 64	28 ns	5 to 16	2 to 5	Full look ahead

The SN54AS181B is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS181A is characterized for operation from 0°C to 70°C.

application note

An application-specific problem has been identified in the SN54AS181B device. The F0−F4 outputs exhibit voltage transients when one or more B-data inputs transition from a high to a low state. The resultant voltage transients can have an amplitude of 2 V relative to V_{OL} with a width of 5 ns at an input threshold of 1.5 V. The transient pulse occurs coincidentally with the high-to-low transition of the B-data input(s) and appears to be caused by internal coupling.

In system operations in which this device is used, it is likely that transmission-line effects minimize this anomaly. Narrow width of the voltage transient makes the pulse transparent to most circuitry; however, in certain applications, the transients can cause system errors.
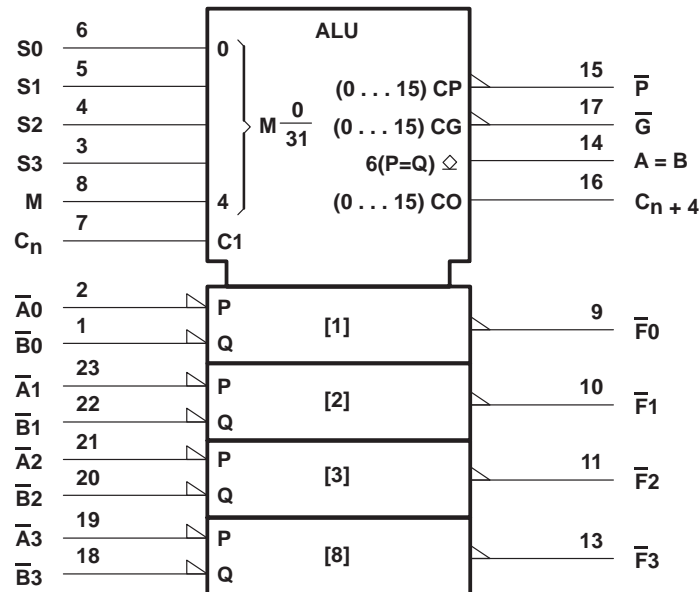
logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JT, JW, N, and NT packages.

SN54AS181B, SN74AS181A
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

logic diagram

Pin numbers shown are for the JT, JW, N, and NT packages.

signal designations

In Figures 1 and 2, the polarity indicators (◁) indicate that the associated input or output is active low with respect to the function shown inside the symbol. The symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The SN54AS181B and SN74AS181A together with the ′S182 can be used with the signal designation of either Figure 1 or Figure 2.

Figure 1
(use with Table 1)

Figure 2
(use with Table 2)

SN54AS181B, SN74AS181A
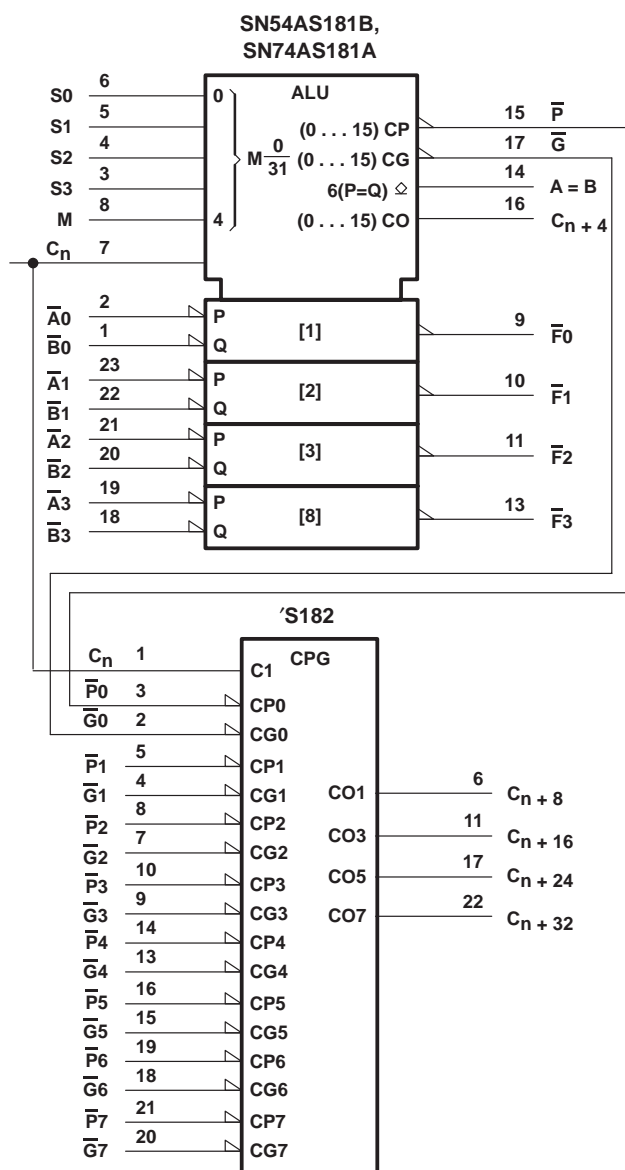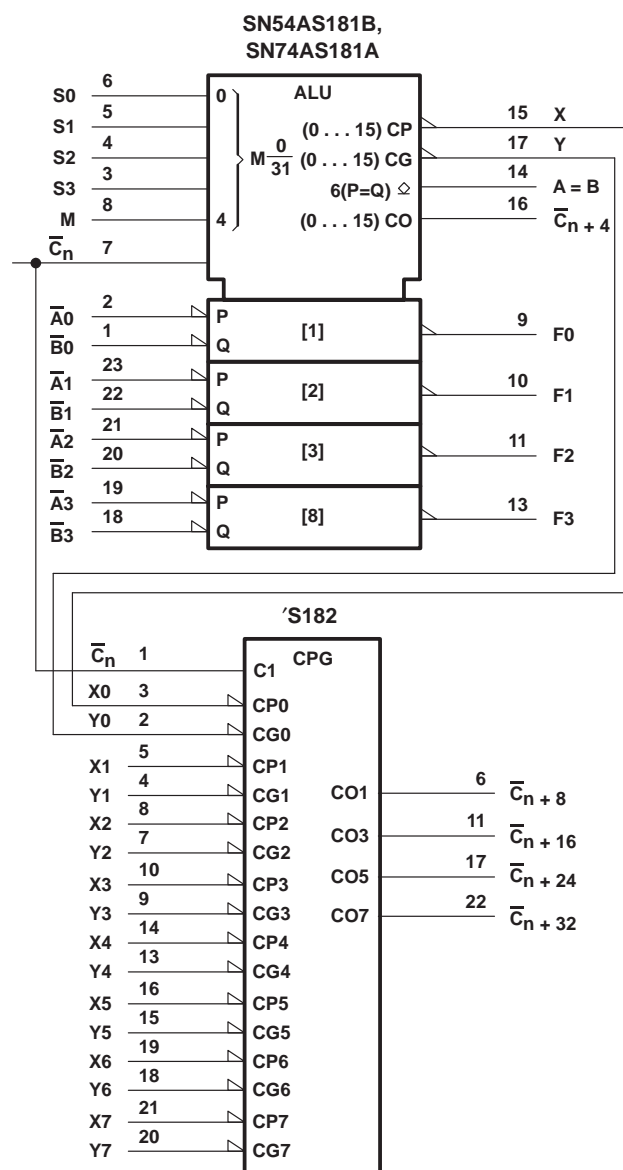# ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

Table 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A} + B$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A + B}$	$F = A$ PLUS $(A + \overline{B})$	$F = A$ PLUS $(A + \overline{B})$ PLUS 1
L	H	L	H	$F = \overline{B}$	$F = AB$ PLUS $(A + \overline{B})$	$F = AB$ PLUS $(A + \overline{B})$ PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \overline{B}$	$F = A + \overline{B}$	$F = (A + \overline{B})$ PLUS 1
H	L	L	L	$F = \overline{A}B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	$F = A\overline{B}$ PLUS (A + B)	$F = A\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	$F = A\overline{B}$ PLUS A	$F = A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A PLUS 1	F = A PLUS 1

† Each bit is shifted to the next more significant position.

Table 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A+ B) PLUS 1
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	$F = \overline{AB}$	$F = A$ PLUS $A\overline{B}$	$F = A$ PLUS $A\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	$F = (A + B)$ PLUS $A\overline{B}$	$F =(A + B)$ PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ MINUS 1	$F = A\,\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	$F = (A + \overline{B})$ PLUS AB	$F = (A + \overline{B})$ PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	$F = (A + \overline{B})$ PLUS A	$F =(A + \overline{B})$ PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

† Each bit is shifted to the next more significant position.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I .... 7 V
Off-state output voltage (A = B output only) .... 7 V
Operating free-air temperature range, T_A: SN54AS181B .... −55°C to 125°C
SN74AS181A .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS181B			SN74AS181A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A = B output only			5.5			5.5	V
I_{OH}	High-level output current	All outputs except A = B and $\overline{G}$			−2			−2	mA
		$\overline{G}$			−3			−3	
I_{OL}	Low-level output current	All outputs except $\overline{G}$			20			20	mA
		$\overline{G}$			48			48	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS181B			SN74AS181A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2			−1.2	V
V_{OH}	Any output except A = B	$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -2$ mA	$V_{CC} - 2$			$V_{CC} - 2$			V
	$\overline{G}$	$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA	2.4	3.4		2.4	3.4		
V_{OL}	Any output except $\overline{G}$	$V_{CC} = 4.5$ V	$I_{OL} = 20$ mA		0.3	0.5		0.3	0.5	V
	$\overline{G}$		$I_{OL} = 48$ mA		0.4	0.5		0.4	0.5	
I_{OH}	A = B	$V_{CC} = 4.5$ V,	$V_{OH} = 5.5$ V			0.1			0.1	mA
I_I	M	$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1			0.1	mA
	Any $\overline{A}$ or $\overline{B}$					0.3			0.3	
	Any S					0.4			0.4	
	C_n					0.6			0.6	
I_{IH}	M	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	μA
	Any $\overline{A}$ or $\overline{B}$					60			60	
	Any S					80			80	
	C_n					120			120	
I_{IL}	M	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			−0.5			−2	mA
	Any $\overline{A}$ or $\overline{B}$					−1.5			−6	
	Any S					−2			−8	
	C_n					−3			−12	
I_O‡	All outputs except A = B and $\overline{G}$	$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	−30	−45	−112	−30	−45	−112	mA
	$\overline{G}$			−30		−125	−30		−125	
I_{CC}		$V_{CC} = 5.5$ V			74	117		135	200	mA

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°$C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

switching characteristics (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX‡				UNIT
				SN54AS181B		SN74AS181A		
				MIN	MAX	MIN	MAX	
t_{PLH}	C_n	C_{n+4}		3	9	2	9	ns
t_{PHL}				2	7	2	9	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0, S1 = S2 = 0, S0 = S3 = 4.5 V (SUM mode)	2	16	2	12	ns
t_{PHL}				2	14	2	12	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	3	18	4	16	ns
t_{PHL}				3	14.5	2	16	
t_{PLH}	C_n	Any $\overline{F}$	M = 0 (SUM or DIFF mode)	3	10.5	3	9	ns
t_{PHL}				3	10	3	9	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0, S1 = S2 = 0, S0 = S3 = 4.5 V (SUM mode)	3	9.5	2	8	ns
t_{PHL}				2	7	2	7	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	3	12	2	9.5	ns
t_{PHL}				2	9	2	9	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0, S1 = S2 = 0, S0 = S3 = 4.5 V (SUM mode)	3	9.5	2	8	ns
t_{PHL}				2	7.5	2	8	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	3	12	2	10	ns
t_{PHL}				3	8.5	2	10	
t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 0, S1 = S2 = 0, S0 = S3 = 4.5 V (SUM mode)	3	11	2	9.5	ns
t_{PHL}				3	9	2	8	
t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	3	13.5	2	10.5	ns
t_{PHL}				3	11	2	10	
t_{PLH}	$\overline{A}i$ or $\overline{B}i$	$\overline{F}i$	M = 4.5 V (LOGIC mode)	3	16	2	11	ns
t_{PHL}				3	10	2	11	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	A = B	M = 0, S1 = S3 = 0, S1 = S2 = 4.5 V (DIFF mode)	2	19	4	21	ns
t_{PHL}				3	22	4	21	

† Refer to the parameter measurement information tables for the SUM-, DIFF-, and LOGIC-mode test tables.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION

SUM-MODE TEST TABLE
(Function Inputs: S0 = S3 = 4.5 V, S1 = S2 = M = 0)

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out of phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out of phase

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

DIFF-MODE TEST TABLE
(Function Inputs: S1 = S2 = 4.5 V, S0 = S3 = M = 0)

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 1)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	$\overline{A_i}$	None	$\overline{B_i}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F_i}$	In phase
t_{PLH} / t_{PHL}	$\overline{B_i}$	$\overline{A_i}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F_i}$	Out of phase
t_{PLH} / t_{PHL}	$\overline{A_i}$	None	$\overline{B_i}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In phase
t_{PLH} / t_{PHL}	$\overline{B_i}$	$\overline{A_i}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out of phase
t_{PLH} / t_{PHL}	$\overline{A_i}$	$\overline{B_i}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In phase
t_{PLH} / t_{PHL}	$\overline{B_i}$	None	$\overline{A_i}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out of phase
t_{PLH} / t_{PHL}	$\overline{A_i}$	None	$\overline{B_i}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In phase
t_{PLH} / t_{PHL}	$\overline{B_i}$	$\overline{A_i}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out of phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or any $\overline{F}$	In phase
t_{PLH} / t_{PHL}	$\overline{A_i}$	$\overline{B_i}$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out of phase
t_{PLH} / t_{PHL}	$\overline{B_i}$	None	$\overline{A_i}$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In phase

LOGIC-MODE TEST TABLE
(Function Inputs: S1 = S2 = M = 4.5 V, S0 = S3 = 0)

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 1)
		APPLY 4.5 V	APPLY GND	APPLY GND	APPLY 4.5 V		
t_{PLH} / t_{PHL}	$\overline{A_i}$	$\overline{B_i}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F_i}$	Out of phase
t_{PLH} / t_{PHL}	$\overline{B_i}$	$\overline{A_i}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F_i}$	Out of phase

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES

LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PULSE DURATIONS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES
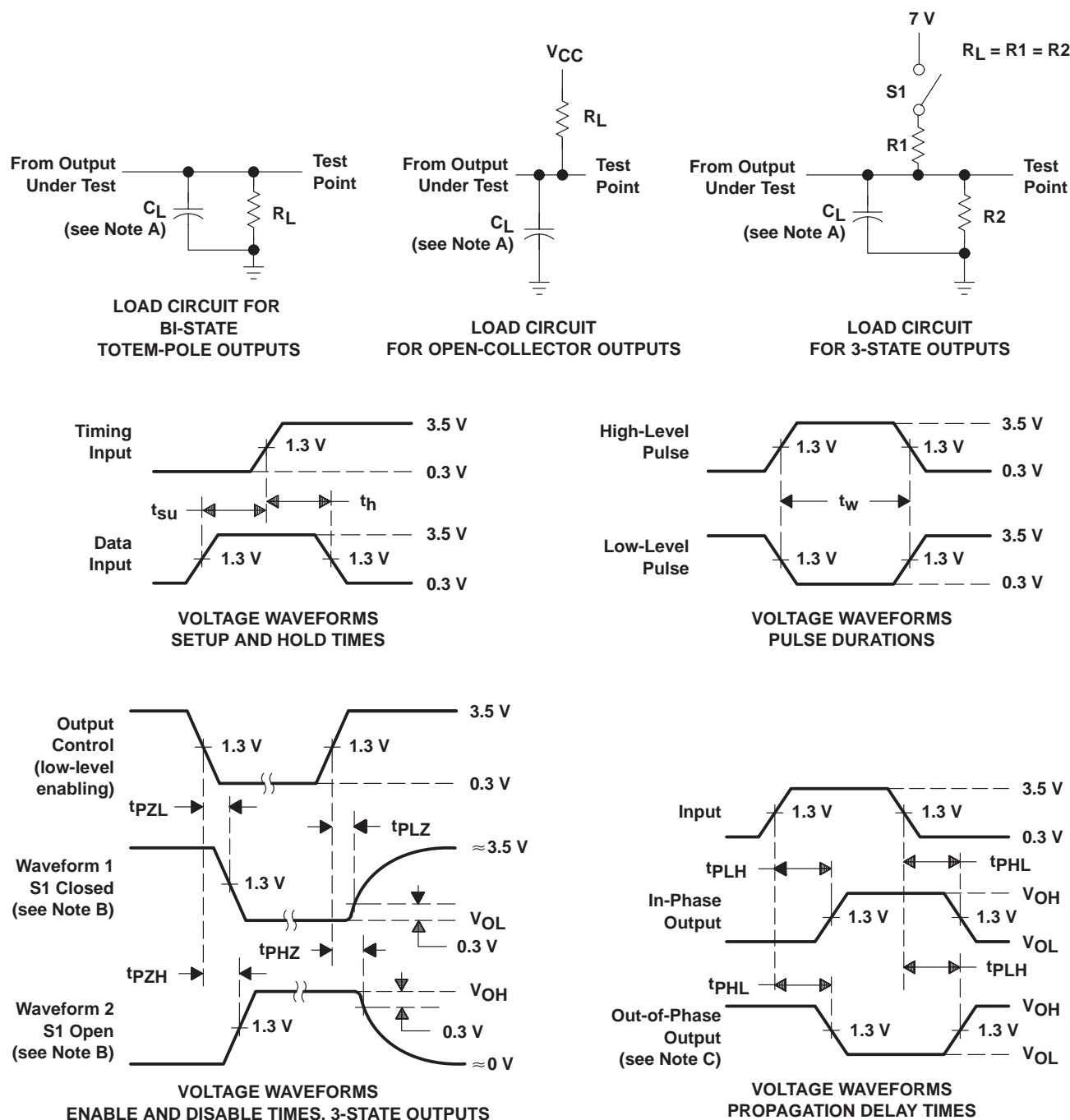
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN54AS181BJT	OBSOLETE	CDIP	JT	24		TBD	Call TI	Call TI
SN74AS181ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS181ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS181ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS181ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS181AN	OBSOLETE	PDIP	N	24		TBD	Call TI	Call TI
SN74AS181ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74AS181ANTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SNJ54AS181BFK	OBSOLETE	LCCC	FK	28		TBD	Call TI	Call TI
SNJ54AS181BJT	OBSOLETE	CDIP	JT	24		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN

DIM \ PINS **	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

A

24   13

B

1   12

0.070 (1,78)
0.030 (0,76)

0.100 (2,54) MAX   0.015 (0,38) MIN

0.320 (8,13)
0.290 (7,37)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.023 (0,58)
0.015 (0,38)

0.100 (2,54)

0.014 (0,36)
0.008 (0,20)

0°–15°

4040110/C 08/96

NOTES: A. All linear dimensions are in inches (millimeters).
  B. This drawing is subject to change without notice.
  C. This package can be hermetically sealed with a ceramic lid using glass frit.
  D. Index point is provided on cap for terminal identification.
  E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S-CQCC-N**)   LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)
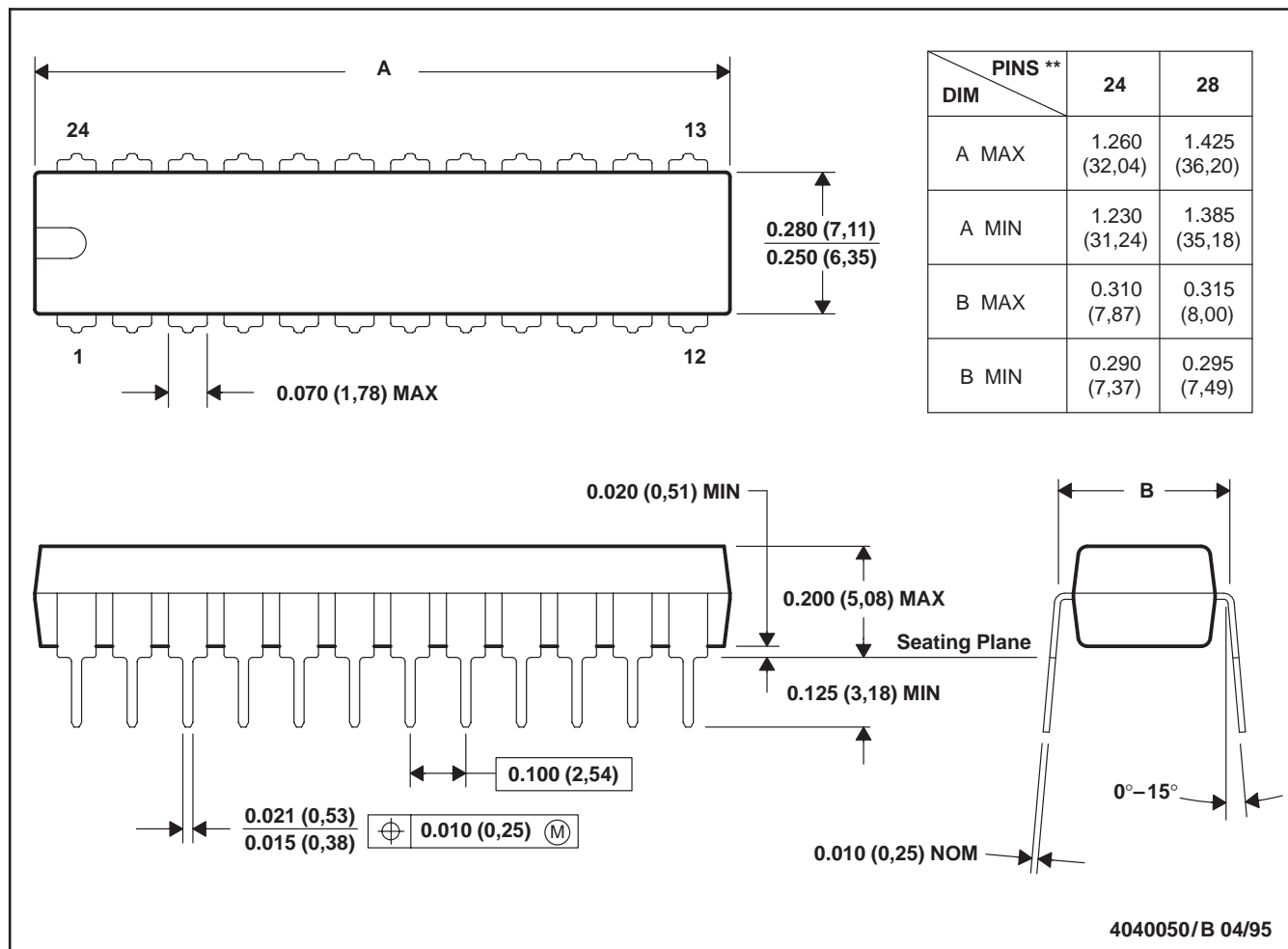
0.045 (1,14) / 0.035 (0,89)

0.050 (1,27)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MECHANICAL DATA

MPDI004 – OCTOBER 1994

NT (R-PDIP-T**)   **PLASTIC DUAL-IN-LINE PACKAGE**

24 PINS SHOWN

PINS ** DIM	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

0.280 (7,11)
0.250 (6,35)

0.070 (1,78) MAX

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)   ⊕ 0.010 (0,25) Ⓜ

0°–15°

0.010 (0,25) NOM

4040050/B 04/95
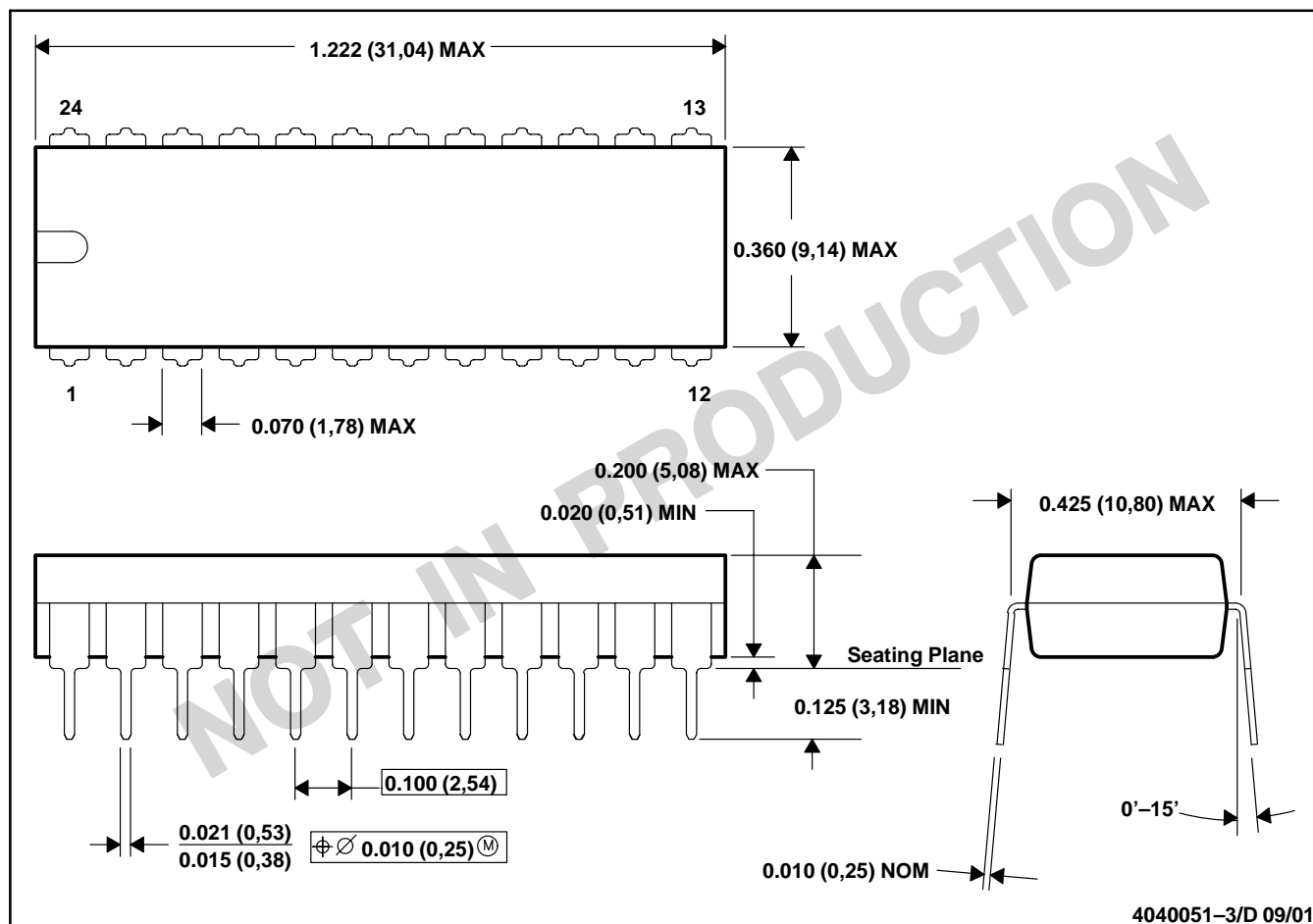
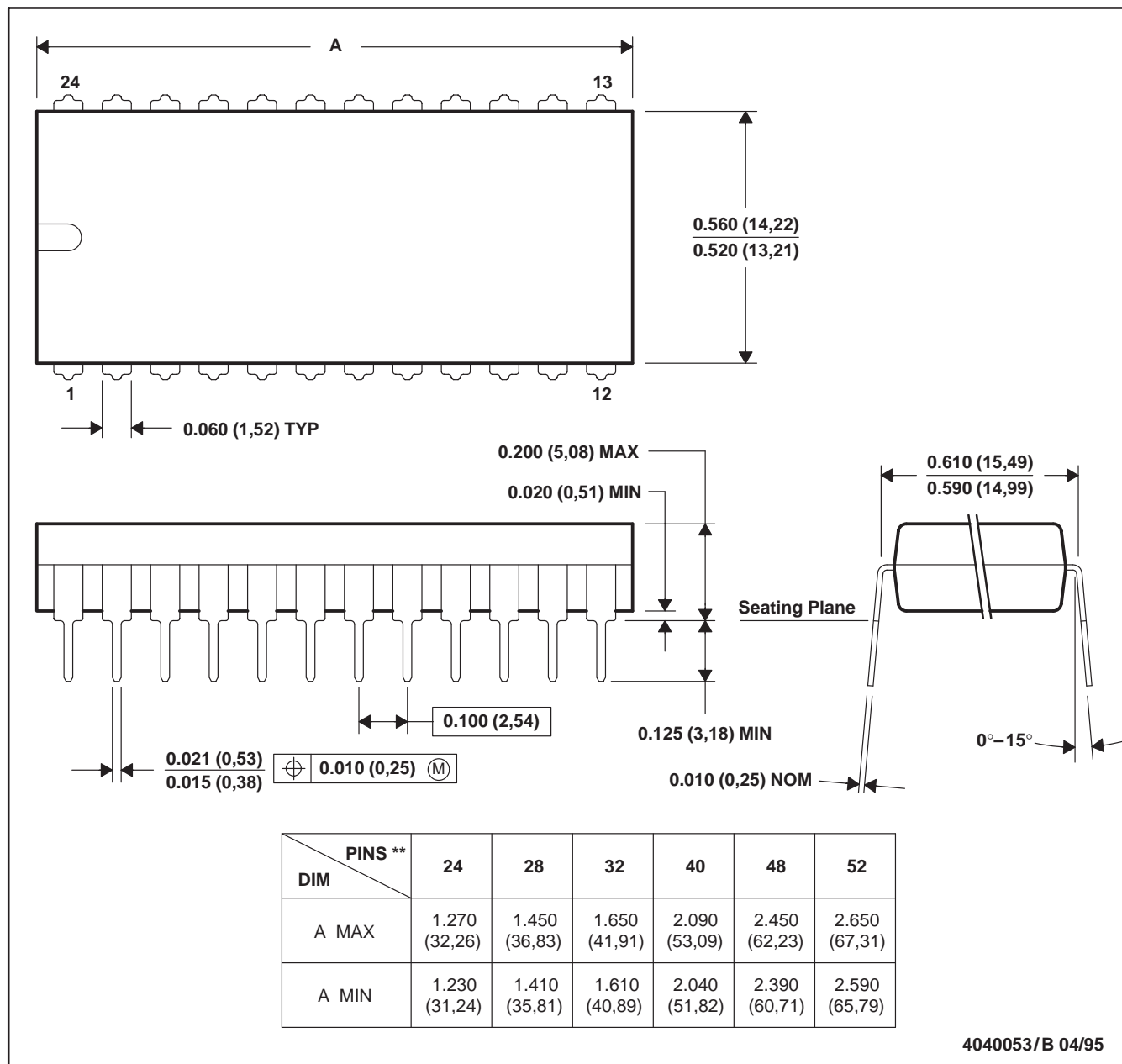NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.

N (R–PDIP–T24)   **PLASTIC DUAL–IN–LINE**

4040051–3/D 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS–010

N (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN

A

24 · · · · · · · · · · · 13

0.560 (14,22)
0.520 (13,21)

1 · · · · · · · · · · · 12

0.060 (1,52) TYP

0.200 (5,08) MAX

0.020 (0,51) MIN

0.610 (15,49)
0.590 (14,99)

Seating Plane

0.100 (2,54)

0.125 (3,18) MIN

0°–15°

0.021 (0,53)
0.015 (0,38)   ⊕ 0.010 (0,25) Ⓜ

0.010 (0,25) NOM

PINS ** DIM	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053 / B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

DW (R−PDSO−G24)   PLASTIC SMALL−OUTLINE PACKAGE

0.614 (15,60)
0.598 (15,20)

24   13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

Gauge Plane

0.010 (0,25)

0°−8°

0.004 (0,10)

Seating Plane

0.050 (1,27)
0.016 (0,40)

4040000−5/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−013 variation AD.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments

Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated