

## ICs for Consumer Electronics

Field Mixer  
SDA 9270

Data Sheet 01.96

|                          |                                                                                                                                                   |
|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>SDA 9270</b>          |                                                                                                                                                   |
| <b>Revision History:</b> | <b>Current Version: 01.96</b>                                                                                                                     |
| Previous Version:        |                                                                                                                                                   |
| Page                     | Subjects (changes since last revision)                                                                                                            |
| 24                       | HYTHL1 control bits have been increased to 6                                                                                                      |
| 25                       | HYTHL2 control bits have been increased to 6                                                                                                      |
| 25                       | HYTHH1 control bits have been increased to 6                                                                                                      |
| 25                       | HYTHH2 control bits have been increased to 6                                                                                                      |
| 27                       | Clock inputs CLL, SCA, SCAD:<br>SCA clock frequency MIN changed to 12 MHz<br>SCAD clock specification added<br>Fall/rise time specification added |
| 27                       | I <sup>2</sup> C-Bus specification extended to fast mode                                                                                          |
| 29                       | Max. average supply current: 200 mA                                                                                                               |

#### **Edition 01.96**

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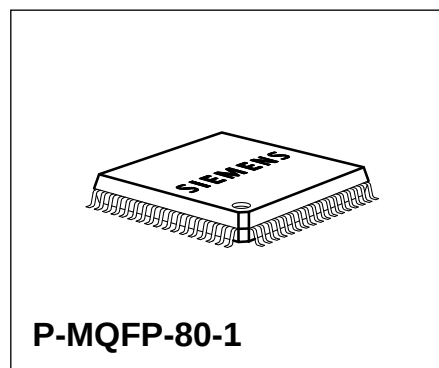
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## 1 Introduction

The Field Mixer SDA 9270 is an add-on component for the Siemens MEGAVISION IC set which enables the system to reduce large area *and* line flickering of interlaced TV standards.

### 1.1 Features

- High performance line flicker reduction algorithm
- Two input data formats (4:1:1 and 4:2:2)
- I<sup>2</sup>C-Bus control
- P-MQFP-80 package
- 5 V supply voltage



### Supported MEGAVISION features

- Multipicture (still in picture, picture in still, 9xpicture)
- Still field
- Zoom

### New MEGAVISION features

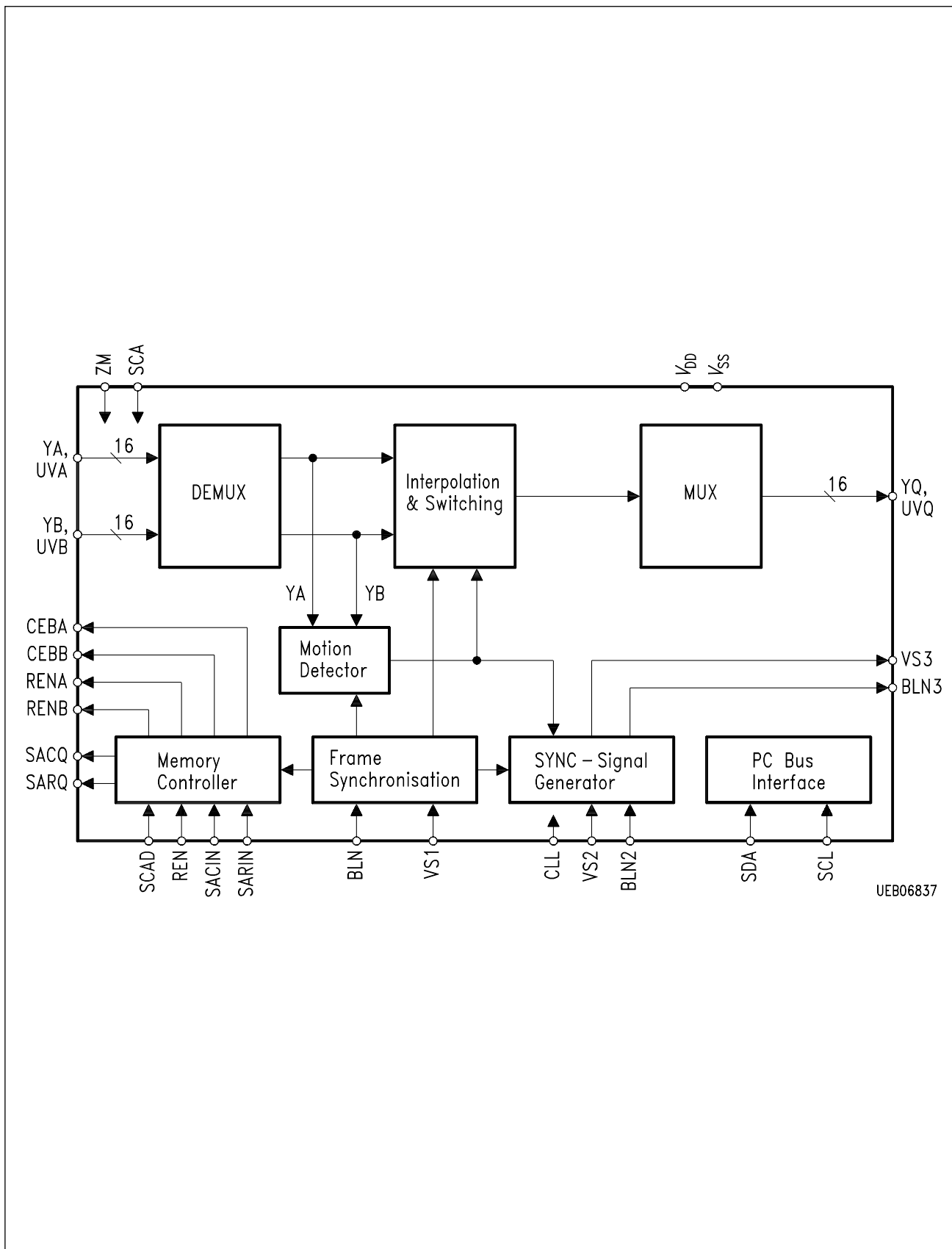
- Still frame
- Background still field

### MEGAVISION features not supported

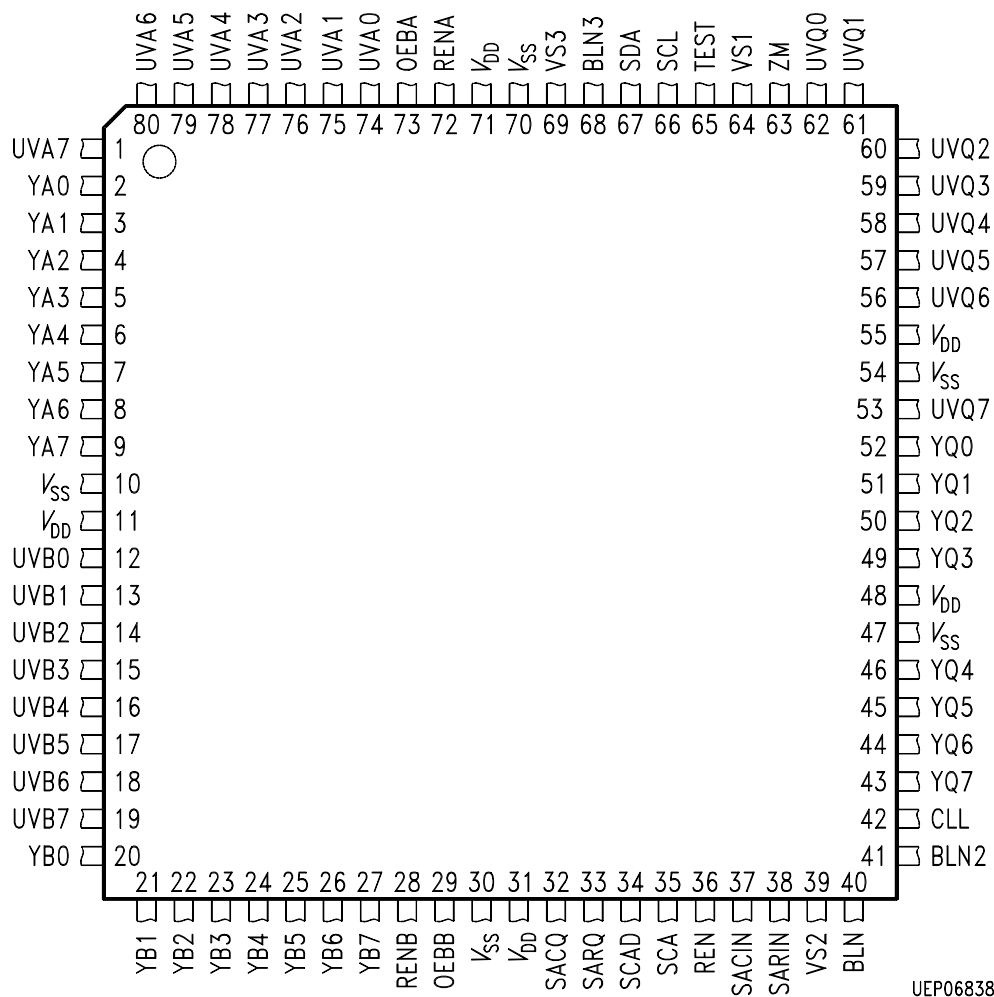
- 4:4:4
- Colored frame insertion (FRM)

| Type     | Ordering Code | Package     |
|----------|---------------|-------------|
| SDA 9270 | Q67100-H5158  | P-MQFP-80-1 |

## 1.2 Block Diagram



## 1.3 Pin Configuration



## 1.4 Pin Description

| Pin No.            | Name      | Type  | Description                                                    |
|--------------------|-----------|-------|----------------------------------------------------------------|
| 10, 30, 47, 54, 70 | $V_{SS}$  | S     | Supply voltage ( $V_{SS}$ ) for digital parts and input stages |
| 11, 31, 48, 55, 71 | $V_{DD}$  | S     | Supply voltage ( $V_{DD}$ ) for digital parts and input stages |
| 74 .. 80,1         | UVA0 .. 7 | I/TTL | Data input UV of channel A (see Data Format)                   |
| 2 .. 9             | YA0 .. 7  | I/TTL | Data input Y of channel A (see Data Format)                    |
| 12 .. 19           | UVB0 .. 7 | I/TTL | Data input UV of channel B (see Data Format)                   |
| 20 .. 27           | YB0 .. 7  | I/TTL | Data input Y of channel B (see Data Format)                    |
| 28                 | RENB      | Q/TTL | RAM enable field memory B                                      |
| 29                 | OEBB      | Q/TTL | Output enable port B of field memory B                         |
| 32                 | SACQ      | Q/TTL | Serial column address output                                   |
| 33                 | SARQ      | Q/TTL | Serial row address output                                      |
| 34                 | SCAD      | I/TTL | Serial address clock input                                     |
| 35                 | SCA       | I/TTL | Clock signal for data input                                    |
| 36                 | REN       | I/TTL | RAM enable / input from SDA 9220                               |
| 37                 | SACIN     | I/TTL | Serial column address / input from SDA 9220                    |
| 38                 | SARIN     | I/TTL | Serial row address / input from SDA 9220                       |
| 39                 | VS2       | I/TTL | 100 Hz vertical synchronization signal                         |
| 40                 | BLN       | I/TTL | Blanking signal, high level indicates active video line        |
| 41                 | BLN2      | I/TTL | Blanking signal / double line frequency                        |
| 42                 | CLL       | I/TTL | System clock                                                   |
| 43.. 46,49..52     | YQ0 .. 7  | Q/TTL | Data output Y of channel Q (see Data Format)                   |
| 53,56 .. 62        | UVQ0 ..7  | Q/TTL | Data output UV of channel Q (see Data Format)                  |
| 63                 | ZM        | I/TTL | Zoom control input (HIGH level for zoom mode)                  |
| 64                 | VS1       | I/TTL | 50 Hz vertical synchronization signal                          |
| 65                 | TEST      | I/TTL | Test pin; must be connected to $V_{SS}$ for normal operation   |
| 66                 | SCL       | I     | I <sup>2</sup> C-Bus clock line                                |
| 67                 | SDA       | IQ    | I <sup>2</sup> C-Bus data line                                 |

## Pin Description (cont'd)

| Pin No. | Name | Type  | Description                                       |
|---------|------|-------|---------------------------------------------------|
| 68      | BLN3 | Q/TTL | Blanking signal / BLN2 delayed                    |
| 69      | VS3  | Q/TTL | Vertical synchronization signal (switched raster) |
| 72      | RENA | Q/TTL | RAM enable field memory A                         |
| 73      | OEBA | Q/TTL | Output enable port B of field memory A            |

S: supply,                      I: input,                      Q: output,                      TTL: digital (TTL)

## 2 System Description

The device generates at its output an opportune sequence of 100/120 Hz fields derived by processing the field A and the field B which are stored in 2 external field memories and made available to the SDA 9270 on 2 separate input ports of 16 bit width each.

The device SDA 9270 generates also control signals for the SDA 9251 which are necessary to operate the TV - SAMs in the Frame mode, that is to write the incoming information alternatively in one or the other field memory.

Additionally the device generates a vertical sync pulse which has to be synchronized with the respective field output. A horizontal blanking signal in phase with the output data is also made available.

## 2.1 Input Data Format

The SDA 9270 accepts for the input channels A and B two different input formats (I<sup>2</sup>C-Bus : INFOR) with two possible sample frequency relations of Y : (B-Y) : (R-Y). The representation of the samples is programmable separately for luminance and chrominance signals as positive dual code or 2's complement code (I<sup>2</sup>C-Bus : INCODL, INCODC)

| Data Pin | Data Format 4:1:1<br>INFOR = 0 |                 |                 |                 | 4:2:2 Parallel<br>INFOR = 1 |                 |
|----------|--------------------------------|-----------------|-----------------|-----------------|-----------------------------|-----------------|
| Yx7      | Y <sub>07</sub>                | Y <sub>17</sub> | Y <sub>27</sub> | Y <sub>37</sub> | Y <sub>07</sub>             | Y <sub>17</sub> |
| Yx6      | Y <sub>06</sub>                | Y <sub>16</sub> | Y <sub>26</sub> | Y <sub>36</sub> | Y <sub>06</sub>             | Y <sub>16</sub> |
| Yx5      | Y <sub>05</sub>                | Y <sub>15</sub> | Y <sub>25</sub> | Y <sub>35</sub> | Y <sub>05</sub>             | Y <sub>15</sub> |
| Yx4      | Y <sub>04</sub>                | Y <sub>14</sub> | Y <sub>24</sub> | Y <sub>34</sub> | Y <sub>04</sub>             | Y <sub>14</sub> |
| Yx3      | Y <sub>03</sub>                | Y <sub>13</sub> | Y <sub>23</sub> | Y <sub>33</sub> | Y <sub>03</sub>             | Y <sub>13</sub> |
| Yx2      | Y <sub>02</sub>                | Y <sub>12</sub> | Y <sub>22</sub> | Y <sub>32</sub> | Y <sub>02</sub>             | Y <sub>12</sub> |
| Yx1      | Y <sub>01</sub>                | Y <sub>11</sub> | Y <sub>21</sub> | Y <sub>31</sub> | Y <sub>01</sub>             | Y <sub>11</sub> |
| Yx0      | Y <sub>00</sub>                | Y <sub>10</sub> | Y <sub>20</sub> | Y <sub>30</sub> | Y <sub>00</sub>             | Y <sub>10</sub> |
| UVx7     | U <sub>07</sub>                | U <sub>05</sub> | U <sub>03</sub> | U <sub>01</sub> | U <sub>07</sub>             | V <sub>07</sub> |
| UVx6     | U <sub>06</sub>                | U <sub>04</sub> | U <sub>02</sub> | U <sub>00</sub> | U <sub>06</sub>             | V <sub>06</sub> |
| UVx5     | V <sub>07</sub>                | V <sub>05</sub> | V <sub>03</sub> | V <sub>01</sub> | U <sub>05</sub>             | V <sub>05</sub> |
| UVx4     | V <sub>06</sub>                | V <sub>04</sub> | V <sub>02</sub> | V <sub>00</sub> | U <sub>04</sub>             | V <sub>04</sub> |
| UVx3     |                                |                 |                 |                 | U <sub>03</sub>             | V <sub>03</sub> |
| UVx2     |                                |                 |                 |                 | U <sub>02</sub>             | V <sub>02</sub> |
| UVx1     |                                |                 |                 |                 | U <sub>01</sub>             | V <sub>01</sub> |
| UVx0     |                                |                 |                 |                 | U <sub>00</sub>             | V <sub>00</sub> |

Yx,UVx : x : A,B

X<sub>ab</sub>: X: signal component a: sample number b: bit number

The amplitude resolution for each input signal component is 8 bit, the maximum clock frequency is 30 MHz. Consequently the SDA 9270 is dedicated for applications in high quality digital video systems. The data input stages and the internal data multiplexer operate with a special input clock (SCA). For applications in the Siemens MEGAVISION System the SCA-clock is identical with the memory output clock.

## 2.2 Output Data Format

The data format for the output channel Q will be a 4:2:2 parallel format in 2's complement code representation.

| <b>Data Pin</b> | <b>4:2:2 Parallel</b> |                 |
|-----------------|-----------------------|-----------------|
| YQ7             | Y <sub>07</sub>       | Y <sub>17</sub> |
| YQ6             | Y <sub>06</sub>       | Y <sub>16</sub> |
| YQ5             | Y <sub>05</sub>       | Y <sub>15</sub> |
| YQ4             | Y <sub>04</sub>       | Y <sub>14</sub> |
| YQ3             | Y <sub>03</sub>       | Y <sub>13</sub> |
| YQ2             | Y <sub>02</sub>       | Y <sub>12</sub> |
| YQ1             | Y <sub>01</sub>       | Y <sub>11</sub> |
| YQ0             | Y <sub>00</sub>       | Y <sub>10</sub> |
| UVQ7            | U <sub>07</sub>       | V <sub>07</sub> |
| UVQ6            | U <sub>06</sub>       | V <sub>06</sub> |
| UVQ5            | U <sub>05</sub>       | V <sub>05</sub> |
| UVQ4            | U <sub>04</sub>       | V <sub>04</sub> |
| UVQ3            | U <sub>03</sub>       | V <sub>03</sub> |
| UVQ2            | U <sub>02</sub>       | V <sub>02</sub> |
| UVQ1            | U <sub>01</sub>       | V <sub>01</sub> |
| UVQ0            | U <sub>00</sub>       | V <sub>00</sub> |

X<sub>ab</sub>:                      X: signal component                      a: sample number                      b: bit number

### **2.3 Field Interpolation and Switching**

In order to reduce the annoying line and edge flickering a frame rate upconversion is implemented. The upconversion includes a combination of interpolation algorithms which are determined via I<sup>2</sup>C-Bus and then selected automatically depending on the picture motion content.

The field interpolation and switching block accepts at its input the data of the two channels A and B, which are the combined luminance and chrominance information respectively of the field A and the field B. The field rate is 100/120 Hz.

A fallback mode which corresponds to the operating mode AABB of the original MEGAVISION system is made available. This mode is selected automatically in case of non-standard input signals carrying unstable sync informations or it can be forced via I<sup>2</sup>C-Bus.

### **2.4 Motion Detection**

The motion detection output is switched in a 25/30 Hz frame synchronous raster. As input signals for this block are accepted the luminance signal components of the input channels A and B. By comparing the two fields the motion detector generates an information about 3 possible motion content levels: LOW, MEDIUM and HIGH.

### **2.5 Field Memory Control**

The Field Mixer SDA 9270 has to provide the two external field memories – composed of TV-SAM SDA 9251 – with two pairs of control signals. One pair RENA and RENB enables the MEGAVISION system to write the incoming field A and field B information alternately into one field memory block and then into the other. A second pair of control signals OEBA and OEBA enables alternately the output back channels of field memory A and B for the noise reduction in the Picture Processor SDA 9290. Because of the timing the serial address signals SAC and SAR generated by the MSC SDA 9220 must be delayed by 4 SCAD-clock periods. This delay is implemented in the SDA 9270.

The Sync signals VS1 and BLN and the clock signal SCAD are used as timing reference signals.

### **2.6 Frame Synchronization**

In order to synchronize the data flows within field memories and Field Mixer and to coordinate the signal information with the associated deflection control the Field Mixer SDA 9270 has to generate 25 Hz picture frame sync signals.

One 25 Hz frame sync signal is necessary for generating the field memory control signals RENA, RENB, OEBA, OEBA with a pattern repetition of 25 Hz each. This signal is synchronized to the front end side video signal of the MEGAVISION block and uses therefore as input signals the 50 Hz vertical sync signal VS1 generated by the MSC SDA 9220 and the horizontal blanking signal BLN.

A second 25 Hz frame sync signal is needed in the interpolation and switching block and in the VS3 pulse generation block for assuring an output data sequence of the channel Q synchronized with the VS3 pulse. As reference signals for this second frame sync signal are used the 100 Hz vertical sync signal VS2 and the blanking signal BLN2 both generated by the MSC SDA 9220.

## 2.7 SYNC-Signal Generation

This functional block generates a couple of sync signal needed in the processing stages following the Field Mixer device. This couple includes the vertical sync signal VS3 and the horizontal blanking signal BLN3. All these signals are synchronized with the output channel Q.

## 2.8 I<sup>2</sup>C-Bus

### 2.8.1 I<sup>2</sup>C-Bus Address

|   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 1 |
|---|---|---|---|---|---|---|

### 2.8.2 I<sup>2</sup>C-Bus Format

write:

|   |   |   |   |   |   |   |   |   |   |            |   |           |   |       |   |   |
|---|---|---|---|---|---|---|---|---|---|------------|---|-----------|---|-------|---|---|
| S | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | A | Subaddress | A | Data Byte | A | ***** | A | P |
|---|---|---|---|---|---|---|---|---|---|------------|---|-----------|---|-------|---|---|

S: Start condition

A: Acknowledge

P: Stop condition

NA: Not Acknowledge

An automatical address increment function is implemented.

After switching on the IC (RES=0), all bits are set to defined states. Particularly:

| Register | Default Value   | Register | Default Value   |
|----------|-----------------|----------|-----------------|
| 00       | 00 <sub>H</sub> | 0B       | 50 <sub>H</sub> |
| 01       | 00 <sub>H</sub> | 0C       | 03 <sub>H</sub> |
| 02       | 00 <sub>H</sub> | 0D       | 0D <sub>H</sub> |
| 03       | 00 <sub>H</sub> | 0E       | 08 <sub>H</sub> |
| 04       | 40 <sub>H</sub> | 0F       | 28 <sub>H</sub> |
| 05       | F4 <sub>H</sub> | 10       | A5 <sub>H</sub> |
| 06       | 58 <sub>H</sub> | 11       | 55 <sub>H</sub> |
| 07       | 20 <sub>H</sub> | 12       | 0A <sub>H</sub> |
| 08       | F8 <sub>H</sub> | 13       | 18 <sub>H</sub> |
| 09       | 70 <sub>H</sub> | 14       | 05 <sub>H</sub> |
| 0A       | E8 <sub>H</sub> | 15       | 03 <sub>H</sub> |

## 2.8.3 I<sup>2</sup>C-Bus Commands

| Sub-add.<br>(Hex.) | Data Byte |           |           |           |           |           |           |           |
|--------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
|                    | D7        | D6        | D5        | D4        | D3        | D2        | D1        | D0        |
| 00                 | LINFRA    | PIXLIN    | WRMODE2   | WRMODE1   | WRMODE0   | NRDEL     | RASTER1   | RASTER0   |
| 01                 | 0         | INCODL    | INCODC    | INFOR     | FALLBACK  | FIWIN2    | FIWIN1    | FIWIN0    |
| 02                 | ZMMODE1   | ZMMODE0   | 0         | 0         | INTMODLL1 | INTMODLL0 | INTMODCL1 | INTMODCL0 |
| 03                 | RDMODE1   | RDMODE0   | 0         | 0         | INTMODLM1 | INTMODLM0 | INTMODCM1 | INTMODCM0 |
| 04                 | EDCONST1  | EDCONST0  | 0         | 0         | INTMODLH1 | INTMODLH0 | INTMODCH1 | INTMODCH0 |
| 05                 | CFHENA07  | CFHENA06  | CFHENA05  | CFHENA04  | CFHENA03  | CFHENA02  | CFHENA01  | CFHENA00  |
| 06                 | CFHENA17  | CFHENA16  | CFHENA15  | CFHENA14  | CFHENA13  | CFHENA12  | CFHENA11  | CFHENA10  |
| 07                 | CFHENB07  | CFHENB06  | CFHENB05  | CFHENB04  | CFHENB03  | CFHENB02  | CFHENB01  | CFHENB00  |
| 08                 | CFSCHA007 | CFSCHA006 | CFSCHA005 | CFSCHA004 | CFSCHA003 | CFSCHA002 | CFSCHA001 | CFSCHA000 |
| 09                 | CFSCHA107 | CFSCHA106 | CFSCHA105 | CFSCHA104 | CFSCHA103 | CFSCHA102 | CFSCHA101 | CFSCHA100 |
| 0A                 | CFSCHA017 | CFSCHA016 | CFSCHA015 | CFSCHA014 | CFSCHA013 | CFSCHA012 | CFSCHA011 | CFSCHA010 |
| 0B                 | CFSCHA117 | CFSCHA116 | CFSCHA115 | CFSCHA114 | CFSCHA113 | CFSCHA112 | CFSCHA111 | CFSCHA110 |
| 0C                 | CFSCHB007 | CFSCHB006 | CFSCHB005 | CFSCHB004 | CFSCHB003 | CFSCHB002 | CFSCHB001 | CFSCHB000 |
| 0D                 | CFSCHB107 | CFSCHB106 | CFSCHB105 | CFSCHB104 | CFSCHB103 | CFSCHB102 | CFSCHB101 | CFSCHB100 |
| 0E                 | CFSCHB017 | CFSCHB016 | CFSCHB015 | CFSCHB014 | CFSCHB013 | CFSCHB012 | CFSCHB011 | CFSCHB010 |

## I<sup>2</sup>C-Bus Commands (cont'd)

| Sub-add.<br>(Hex.) | Data Byte |           |           |           |           |           |           |           |
|--------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
|                    | D7        | D6        | D5        | D4        | D3        | D2        | D1        | D0        |
| <b>0F</b>          | CFSCHB117 | CFSCHB116 | CFSCHB115 | CFSCHB114 | CFSCHB113 | CFSCHB112 | CFSCHB111 | CFSCHB110 |
| <b>10</b>          | MDTHL21   | MDTHL20   | MDTHL11   | MDTHL10   | 0         | MDBLTH2   | MDBLTH1   | MDBLTH0   |
| <b>11</b>          | MDTHU21   | MDTHU20   | MDTHU11   | MDTHU10   | MDTHM21   | MDTHM20   | MDTHM11   | MDTHM10   |
| <b>12</b>          | 0         | 0         | HYTHL15   | HYTHL14   | HYTHL13   | HYTHL12   | HYTHL11   | HYTHL10   |
| <b>13</b>          | 0         | 0         | HYTHL25   | HYTHL24   | HYTHL23   | HYTHL22   | HYTHL21   | HYTHL20   |
| <b>14</b>          | 0         | 0         | HYTHH15   | HYTHH14   | HYTHH13   | HYTHH12   | HYTHH11   | HYTHH10   |
| <b>15</b>          | 0         | 0         | HYTHH25   | HYTHH24   | HYTHH23   | HYTHH22   | HYTHH21   | HYTHH20   |

## 2.8.4 Detailed Description

| Subaddress 00 |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit           | Name    | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| D7            | LINFRA  | Lines per frame:<br>0 : 625 lines per frame (default value)<br>1 : 525 lines per frame                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| D6            | PIXLIN  | Pixels per line:<br>0 : 864 pixels per line (default value)<br>1 : 858 pixels per line                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| D5...D3       | WRMODE* | Write Mode:<br>000 : Normal operation: field memory A and field memory B are written alternately (default value)<br>001 : Still picture A and B: writing is suppressed for both field memories<br>010 : Still picture A: writing is suppressed for field memory A, <b>all</b> incoming fields are written to field memory B<br>011 : Still picture A: writing is suppressed for field memory A, <b>every second</b> field is written to field memory B (Field Mode B)<br>100 : Still picture B: writing is suppressed for field memory B, <b>all</b> incoming fields are written to field memory A<br>101 : Still picture B: writing is suppressed for field memory B, <b>every second</b> field is written to field memory A (Field Mode A)<br>110 : Reserved<br>111 : Reserved |
| D2            | NRDEL   | Noise Reduction Delay:<br>conditions: 2 field memory configuration, WRMODE = 000<br>0: Data delay for recursive filtering is one frame (default value)<br>1: Data delay for recursive filtering is one field                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| D1...D0       | RASTER* | Deflection Raster control:<br>00: Control by interpolation algorithm (default value)<br>01: $\alpha\alpha\beta\beta$<br>10: $\alpha\beta\alpha\beta$<br>11: $\alpha\alpha\alpha\alpha$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

**Note:** SDA 9220 programming:

- Subaddress 00 / D7 (EXSYN): For EXSYN=1 WRMODE=100 is required.
- Subaddress 01 / D7 (FLDM), Subaddress 02 / D7 (STB): FLDM and STB should always be set to 0.
- Subaddress 00 / D1, D0 (VDM): VDM must be set to 00.

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**Subaddress 01**


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| Bit     | Name     | Function                                                                                                                                                                                                                                                                                                                                                                  |
|---------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D6      | INCODL   | Coding of luminance input data:<br>0: positive dual code (default value)<br>1: 2's complement                                                                                                                                                                                                                                                                             |
| D5      | INCODC   | Coding of chrominance input data:<br>0: positive dual code (default value)<br>1: 2's complement                                                                                                                                                                                                                                                                           |
| D4      | INFOR    | Input data format:<br>0: 4:1:1 luminance, chrominance parallel (8+4 wires) (default value)<br>1: 4:2:2 luminance, chrominance parallel (8+8 wires)                                                                                                                                                                                                                        |
| D3      | FALLBACK | Fallback mode:<br>0: Normal operation (default value)<br>1: programmed fall back mode is activated for current display                                                                                                                                                                                                                                                    |
| D2...D0 | FIWIN    | Field identification window<br>Definition of a time window. Switching from fall back mode to programmed display mode is not performed until the field identification algorithm is working in a stable condition during the programmed time.<br>000 : 7 field periods (default value)<br>001 : 15 field periods<br>: :<br>110 : 55 field periods<br>111 : 63 field periods |

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**Subaddress 02**


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| Bit    | Name     | Function                                                                                                                                                                                                                                                                                                                                                                |
|--------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D7..D6 | ZMMODE   | zoom mode (enabled only if pin ZM = 1 and RDMODE = 00)<br>00: field sequence at output Q: AABB (default value)<br>01: field sequence at output Q: ABAB<br>10: display with raster correction<br>11: Reserved                                                                                                                                                            |
| D3..D2 | INTMODLL | luminance interpolation mode, low degree of motion<br>00: field sequence AABB without interpolation ( $\alpha\alpha\beta\beta$ ) (default value)<br>01: field sequence ABAB without interpolation ( $\alpha\beta\alpha\beta$ )<br>10: Schröder algorithm ( $\alpha\beta\alpha\beta$ )<br>11: Hentschel algorithm ( $\alpha\beta\alpha\beta$ )                           |
| D1..D0 | INTMODCL | chrominance interpolation mode, low degree of motion<br>00: field sequence AABB without interpolation ( $\alpha\alpha\beta\beta$ ) (default value)<br>01: field sequence AABB without interpolation ( $\alpha\beta\alpha\beta$ )<br>10: field sequence ABAB without interpolation ( $\alpha\beta\alpha\beta$ )<br>11: linear interpolation ( $\alpha\beta\alpha\beta$ ) |

## Subaddress 03

| Bit    | Name     | Function                                                                                                                                                                                                                                                                                                                                                                      |
|--------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D7..D6 | RDMODE   | read mode<br>00: both inputs are used<br>(interpolation enabled if ZM = 0)<br>(default value)<br>01: only input A is used (without interpolation)<br>10: only input B is used (without interpolation)<br>11: Reserved                                                                                                                                                         |
| D3..D2 | INTMODLM | luminance interpolation mode, medium degree of motion<br>00: field sequence AABB without interpolation ( $\alpha\alpha\beta\beta$ )<br>(default value)<br>01: field sequence ABAB without interpolation ( $\alpha\beta\alpha\beta$ )<br>10: Schröder algorithm ( $\alpha\beta\alpha\beta$ )<br>11: Hentschel algorithm ( $\alpha\beta\alpha\beta$ )                           |
| D1..D0 | INTMODCM | chrominance interpolation mode, medium degree of motion<br>00: field sequence AABB without interpolation ( $\alpha\alpha\beta\beta$ )<br>(default value)<br>01: field sequence AABB without interpolation ( $\alpha\beta\alpha\beta$ )<br>10: field sequence ABAB without interpolation ( $\alpha\beta\alpha\beta$ )<br>11: linear interpolation ( $\alpha\beta\alpha\beta$ ) |

## Subaddress 04

| Bit    | Name     | Function                                                                                                                                                                                                                                                                                                                                                                     |
|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D7..D6 | EDCONST  | edge detector gain factor<br>00: 2<br>01: 3 (default value)<br>10: 4<br>11: 5                                                                                                                                                                                                                                                                                                |
| D3..D2 | INTMODLH | luminance interpolation mode, high degree of motion<br>00: field sequence AABB without interpolation ( $\alpha\alpha\beta\beta$ ) (default value)<br>01: field sequence ABAB without interpolation ( $\alpha\beta\alpha\beta$ )<br>10: Schröder algorithm ( $\alpha\beta\alpha\beta$ )<br>11: Hentschel algorithm ( $\alpha\beta\alpha\beta$ )                               |
| D1..D0 | INTMODCH | chrominance interpolation mode, high low degree of motion<br>00: field sequence AABB without interpolation ( $\alpha\alpha\beta\beta$ ) (default value)<br>01: field sequence AABB without interpolation ( $\alpha\beta\alpha\beta$ )<br>10: field sequence ABAB without interpolation ( $\alpha\beta\alpha\beta$ )<br>11: linear interpolation ( $\alpha\beta\alpha\beta$ ) |

## Subaddress 05

| Bit    | Name    | Function                                                                              |
|--------|---------|---------------------------------------------------------------------------------------|
| D7..D0 | CFHENA0 | Hentschel algorithm, 8-bit coefficient $a_0$ (2's complement) (default value $F4_H$ ) |

## Subaddress 06

| Bit    | Name    | Function                                                                              |
|--------|---------|---------------------------------------------------------------------------------------|
| D7..D0 | CFHENA1 | Hentschel algorithm, 8-bit coefficient $a_1$ (2's complement) (default value $58_H$ ) |

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**Subaddress 07**

| Bit    | Name    | Function                                                                                       |
|--------|---------|------------------------------------------------------------------------------------------------|
| D7..D0 | CFHENB0 | Hentschel algorithm, 8-bit coefficient $b_0$ (2's complement) (default value 20 <sub>H</sub> ) |

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**Subaddress 08**

| Bit    | Name     | Function                                                                                         |
|--------|----------|--------------------------------------------------------------------------------------------------|
| D7..D0 | CFSCHA00 | Schröder algorithm, 8-bit coefficient $a_{00}$ (2's complement) (default value F8 <sub>H</sub> ) |

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**Subaddress 09**

| Bit    | Name     | Function                                                                                         |
|--------|----------|--------------------------------------------------------------------------------------------------|
| D7..D0 | CFSCHA10 | Schröder algorithm, 8-bit coefficient $a_{10}$ (2's complement) (default value 70 <sub>H</sub> ) |

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**Subaddress 0A**

| Bit    | Name     | Function                                                                                         |
|--------|----------|--------------------------------------------------------------------------------------------------|
| D7..D0 | CFSCHA01 | Schröder algorithm, 8-bit coefficient $a_{01}$ (2's complement) (default value E8 <sub>H</sub> ) |

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**Subaddress 0B**

| Bit    | Name     | Function                                                                                         |
|--------|----------|--------------------------------------------------------------------------------------------------|
| D7..D0 | CFSCHA11 | Schröder algorithm, 8-bit coefficient $a_{11}$ (2's complement) (default value 50 <sub>H</sub> ) |

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**Subaddress 0C**

| Bit    | Name     | Function                                                                                         |
|--------|----------|--------------------------------------------------------------------------------------------------|
| D7..D0 | CFSCHB00 | Schröder algorithm, 8-bit coefficient $b_{00}$ (2's complement) (default value 03 <sub>H</sub> ) |

## Subaddress 0D

| Bit    | Name     | Function                                                                                            |
|--------|----------|-----------------------------------------------------------------------------------------------------|
| D7..D0 | CFSCHB10 | Schröder algorithm, 8-bit coefficient $b_{10}$ (2's complement)<br>(default value 0D <sub>H</sub> ) |

## Subaddress 0E

| Bit    | Name     | Function                                                                                            |
|--------|----------|-----------------------------------------------------------------------------------------------------|
| D7..D0 | CFSCHB01 | Schröder algorithm, 8-bit coefficient $b_{01}$ (2's complement)<br>(default value 08 <sub>H</sub> ) |

## Subaddress 0F

| Bit    | Name     | Function                                                                                            |
|--------|----------|-----------------------------------------------------------------------------------------------------|
| D7..D0 | CFSCHB11 | Schröder algorithm, 8-bit coefficient $b_{11}$ (2's complement)<br>(default value 28 <sub>H</sub> ) |

## Subaddress 10

| Bit    | Name   | Function                                                                                                   |
|--------|--------|------------------------------------------------------------------------------------------------------------|
| D7..D6 | MDTHL2 | threshold for low degree of motion (small blocks)<br>00: 0<br>01: 64<br>10: 128 (default value)<br>11: 192 |
| D5..D4 | MDTHL1 | threshold for low degree of motion (large blocks)<br>00: 0<br>01: 64<br>10: 128 (default value)<br>11: 192 |
| D2..D0 | MDBLTH | threshold in front of the blocking module<br>000: 4<br>001: 8<br>: :<br>111: 32<br>(default value 101)     |

## Subaddress 11

| Bit    | Name   | Function                                                                                                        |
|--------|--------|-----------------------------------------------------------------------------------------------------------------|
| D7..D6 | MDTHU2 | threshold for high degree of motion (small blocks)<br>00: 384<br>01: 512 (default value)<br>10: 640<br>11: 768  |
| D5..D4 | MDTHU1 | threshold for high degree of motion (large blocks)<br>00: 384<br>01: 512 (default value)<br>10: 640<br>11: 768  |
| D3..D2 | MDTHM2 | threshold for second field difference (small blocks)<br>00: 64<br>01: 128 (default value)<br>10: 192<br>11: 256 |
| D1..D0 | MDTHM1 | threshold for second field difference (large blocks)<br>00: 64<br>01: 128 (default value)<br>10: 192<br>11: 256 |

## Subaddress 12

| Bit    | Name   | Function                                                                                                                                      |
|--------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| D5..D0 | HYTHL1 | hysteresis threshold, low degree of motion (large blocks)<br>000000: 1<br>000001: 1<br>000010: 2<br>:<br>111111: 63<br>(default value 001010) |

## Subaddress 13

| Bit    | Name   | Function                                                                                                                                      |
|--------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| D5..D0 | HYTHL2 | hysteresis threshold, low degree of motion (small blocks)<br>000000: 1<br>000001: 1<br>000010: 2<br>:<br>111111: 63<br>(default value 011000) |

## Subaddress 14

| Bit    | Name   | Function                                                                                                                                       |
|--------|--------|------------------------------------------------------------------------------------------------------------------------------------------------|
| D5..D0 | HYTHH1 | hysteresis threshold, high degree of motion (large blocks)<br>000000: 1<br>000001: 1<br>000010: 2<br>:<br>111111: 63<br>(default value 000101) |

## Subaddress 15

| Bit    | Name   | Function                                                                                                                                       |
|--------|--------|------------------------------------------------------------------------------------------------------------------------------------------------|
| D5..D0 | HYTHH2 | hysteresis threshold, high degree of motion (small blocks)<br>000000: 1<br>000001: 1<br>000010: 2<br>:<br>111111: 63<br>(default value 000011) |

### 3 Electrical Characteristics

#### 3.1 Absolute Maximum Ratings

| Parameter                       | Symbol    | Limit Values |                  | Unit | Remark                                                                                 |
|---------------------------------|-----------|--------------|------------------|------|----------------------------------------------------------------------------------------|
|                                 |           | min.         | max.             |      |                                                                                        |
| Operating temperature           | $T_A$     | 0            | 70               | °C   |                                                                                        |
| Storage temperature             | $T_{stg}$ | – 65         | 125              | °C   |                                                                                        |
| Junction temperature            | $T_j$     |              | 125              | °C   |                                                                                        |
| Soldering temperature           | $T_S$     |              | 260              | °C   |                                                                                        |
| Soldering time                  | $t_S$     |              | 10               | s    |                                                                                        |
| Input voltage                   | $V_I$     | – 0.3 V      | $V_{DD} + 0.3$ V | V    | $V_{CC}$ respectively                                                                  |
| Output voltage                  | $V_Q$     | – 0.3 V      | $V_{DD} + 0.3$ V | V    | $V_{CC}$ respectively                                                                  |
| Supply voltages                 | $V_S$     | – 0.3        | 6                | V    |                                                                                        |
| Supply voltage<br>Differentials | V         | – 0.25       | 0.25             | V    | between any internally non-connected supply pins of the same kind, see Pin Description |
| Total power dissipation         | $P_{tot}$ |              | 1                | W    |                                                                                        |
| ESD protection                  | ESD       | – 2          | 2                | kV   | MIL STD 883C method 3015.6, 100 pF, 1500 $\Omega$                                      |
| Latch-up protection             |           | – 100        | 100              | mA   | all inputs/outputs                                                                     |

All voltages listed are referenced to ground (0 V,  $V_{SS}$ ) except where noted.

**Note:** Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the operational sections of this specification is not implied.

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

### 3.2 Recommended Operating Conditions

| Parameter           | Symbol               | Limit Values |      |      | Unit | Test Conditions |
|---------------------|----------------------|--------------|------|------|------|-----------------|
|                     |                      | min.         | typ. | max. |      |                 |
| Supply voltages     | $V_{DD}$<br>$V_{CC}$ | 4.5          | 5    | 5.5  | V    |                 |
| Ambient temperature | $T_A$                | 0            | 25   | 70   | °C   |                 |

#### All TTL Inputs

|                          |          |       |  |          |   |  |
|--------------------------|----------|-------|--|----------|---|--|
| High-level input voltage | $V_{IH}$ | 2.0 V |  | $V_{DD}$ | 1 |  |
| Low-level input voltage  | $V_{IL}$ | 0     |  | 0.8      | V |  |

#### All TTL outputs

|                           |          |     |  |     |   |                            |
|---------------------------|----------|-----|--|-----|---|----------------------------|
| High-level output voltage | $V_{QH}$ | 2.4 |  |     | V | $I_{QH} = -2.0 \text{ mA}$ |
| Low-level output voltage  | $V_{QL}$ |     |  | 0.4 | V | $I_{QL} = 3.0 \text{ mA}$  |

#### Clock TTL Inputs CLL, SCA, SCAD

|                     |           |    |    |    |     |                                       |
|---------------------|-----------|----|----|----|-----|---------------------------------------|
| Clock frequency     |           | 12 | 27 | 30 | MHz |                                       |
| Low time            | $t_{WL}$  | 10 |    |    | ns  | Rise/fall time<br>$\leq 5 \text{ ns}$ |
| High time           | $t_{WH}$  | 10 |    |    | ns  |                                       |
| Rise time           | $t_{TLH}$ |    |    | 5  | ns  |                                       |
| Fall time           | $t_{THL}$ |    |    | 5  | ns  |                                       |
| SCA - CLL skew time | $t_{SK}$  | 0  |    | 15 | ns  | Diagram<br>on page 22                 |

#### I<sup>2</sup>C Bus (all values are referred to min( $V_{IH}$ ) and max( $V_{IL}$ ))

|                                            |              |     |  |          |     |  |
|--------------------------------------------|--------------|-----|--|----------|-----|--|
| High-level input voltage                   | $V_{IH}$     | 3 V |  | $V_{DD}$ | 1   |  |
| Low-level input voltage                    | $V_{IL}$     | 0   |  | 1.5      | V   |  |
| SCL clock frequency                        | $f_{SCL}$    | 0   |  | 400      | kHz |  |
| Inactive time before start of transmission | $t_{BUF}$    | 1.3 |  |          | μs  |  |
| Set-up time start condition                | $t_{SU;STA}$ | 0.6 |  |          | μs  |  |
| Hold time start condition                  | $t_{HD;STA}$ | 0.6 |  |          | μs  |  |
| SCL low time                               | $t_{LOW}$    | 1.3 |  |          | μ   |  |
| SCL high time                              | $t_{HIGH}$   | 0.6 |  |          | μs  |  |
| Set-up time DATA                           | $t_{SU;DAT}$ | 100 |  |          | ns  |  |

### 3.2 Recommended Operating Conditions (cont'd)

| Parameter                  | Symbol              | Limit Values |      |      | Unit          | Test Conditions                    |
|----------------------------|---------------------|--------------|------|------|---------------|------------------------------------|
|                            |                     | min.         | typ. | max. |               |                                    |
| Hold time DATA             | $t_{\text{HD;DAT}}$ | 0            |      |      | $\mu\text{s}$ |                                    |
| SDA/SCL rise times         | $t_{\text{R}}$      |              |      | 300  | ns            | $f_{\text{SCL}} = 400 \text{ kHz}$ |
| SDA/SCL fall times         | $t_{\text{F}}$      |              |      | 300  | ns            |                                    |
| Set-up time stop condition | $t_{\text{SU;STO}}$ | 0.6          |      |      | $\mu\text{s}$ |                                    |
| Low-level output current   | $I_{\text{OL}}$     |              |      | 3    | mA            |                                    |

**Note:** Under this conditions the functions given in the circuit description are fulfilled. Nominal conditions specify mean values expected over the production spread and are the proposed values for interface and application. If not stated otherwise, nominal values will apply at  $T_{\text{A}} = 25 \text{ }^{\circ}\text{C}$  and the nominal supply voltage.

### 3.3 Characteristics (Assuming Recommended Operating Conditions)

| Parameter              | Symbol | Limit Values |      | Unit | Remark                         |
|------------------------|--------|--------------|------|------|--------------------------------|
|                        |        | min.         | max. |      |                                |
| Average supply current | $I_S$  |              | 200  | mA   | All $V_{CC}$ and $V_{DD}$ pins |

#### All Digital Inputs (including I/O inputs)

|                       |       |      |    |    |                                       |
|-----------------------|-------|------|----|----|---------------------------------------|
| Input capacitance     | $C_I$ |      | 10 | pF | Not tested;<br>max. 7 pF for SCA, CLL |
| Input leakage current | $I_I$ | - 10 | 10 | μA |                                       |

#### TTL Inputs: YA, YB, UVA, UVB (referenced to SCA)

|                 |          |   |  |    |  |
|-----------------|----------|---|--|----|--|
| Set-up time     | $t_{SU}$ | 7 |  | ns |  |
| Input hold time | $t_{IH}$ | 6 |  | ns |  |

#### TTL Inputs: REN, SACIN, SARIN (referenced to SCAD)

|                 |          |   |  |    |  |
|-----------------|----------|---|--|----|--|
| Set-up time     | $t_{SU}$ | 7 |  | ns |  |
| Input hold time | $t_{IH}$ | 6 |  | ns |  |

#### TTL Inputs: BLN, BLN2, VS1, VS2, ZM (referenced to CLL)

**Note:** For BLN a jitter of  $\pm 1$  CLL is allowed

|                 |          |   |  |    |  |
|-----------------|----------|---|--|----|--|
| Set-up time     | $t_{SU}$ | 7 |  | ns |  |
| Input hold time | $t_{IH}$ | 6 |  | ns |  |

#### TTL Outputs: YQ, UVQ (referenced to CLL)

|            |          |   |    |    |               |
|------------|----------|---|----|----|---------------|
| Hold time  | $t_{QH}$ | 6 |    | ns |               |
| Delay time | $t_{QD}$ |   | 25 | ns | $C_L = 30$ pF |

#### TTL Outputs: VS3, BLN3 (referenced to CLL)

|            |          |   |    |    |               |
|------------|----------|---|----|----|---------------|
| Hold time  | $t_{QH}$ | 6 |    | ns |               |
| Delay time | $t_{QD}$ |   | 25 | ns | $C_L = 30$ pF |

#### TTL Outputs: RENA, RENB, SACQ, SARQ (referenced to SCAD)

|            |          |   |    |    |               |
|------------|----------|---|----|----|---------------|
| Hold time  | $t_{QH}$ | 6 |    | ns |               |
| Delay time | $t_{QD}$ |   | 20 | ns | $C_L = 50$ pF |

**3.3 Characteristics** (Assuming Recommended Operating Conditions) (cont'd)

| Parameter | Symbol | Limit Values |      | Unit | Remark |
|-----------|--------|--------------|------|------|--------|
|           |        | min.         | max. |      |        |

**TTL Outputs: OEBA, OEBC (referenced to SCAD)**

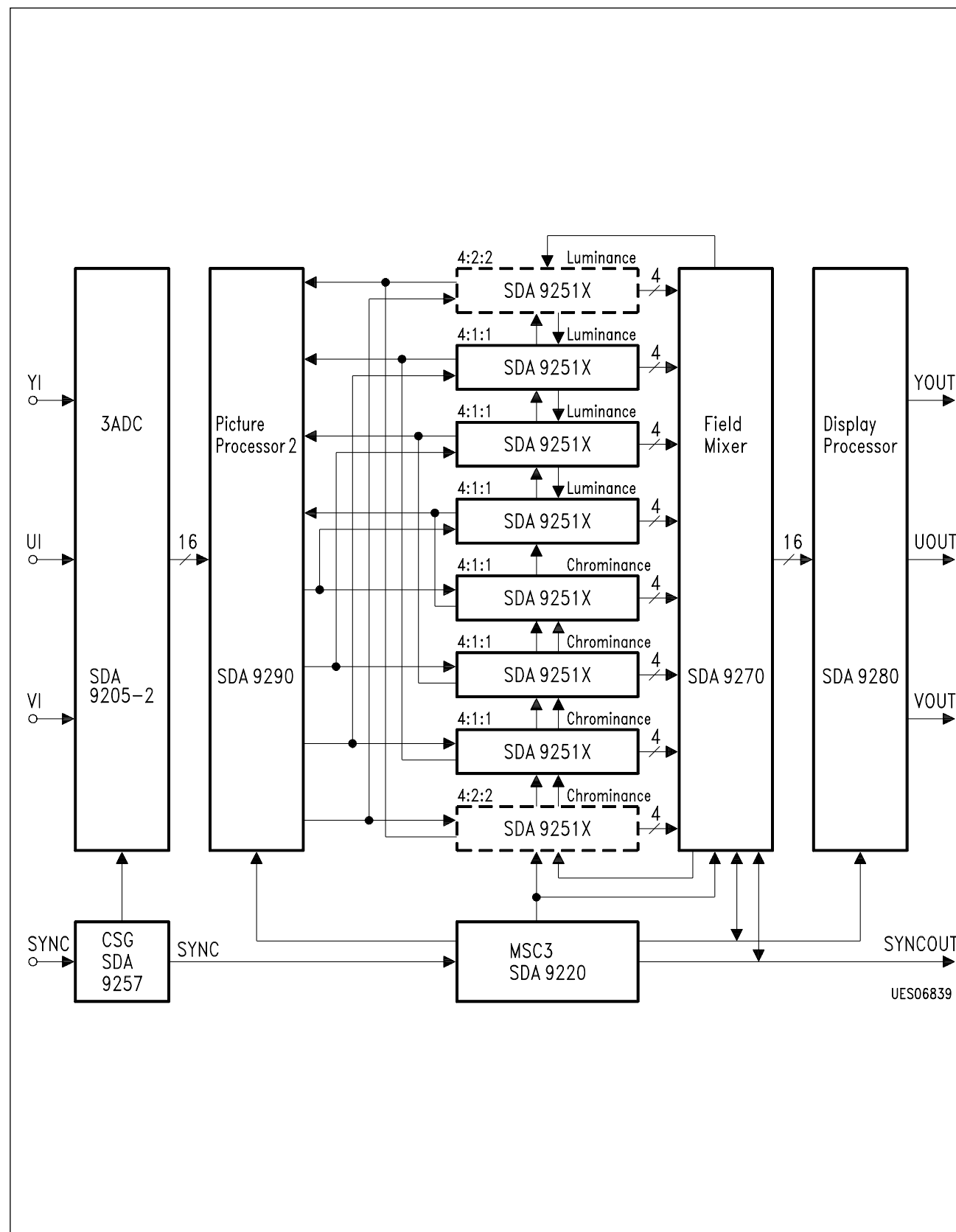
|            |          |   |    |    |                       |
|------------|----------|---|----|----|-----------------------|
| Hold time  | $t_{QH}$ | 6 |    | ns |                       |
| Delay time | $t_{QD}$ |   | 20 | ns | $C_L = 30 \text{ pF}$ |

**Input/Output: SDA (referenced to SCL; Open Drain Output)**

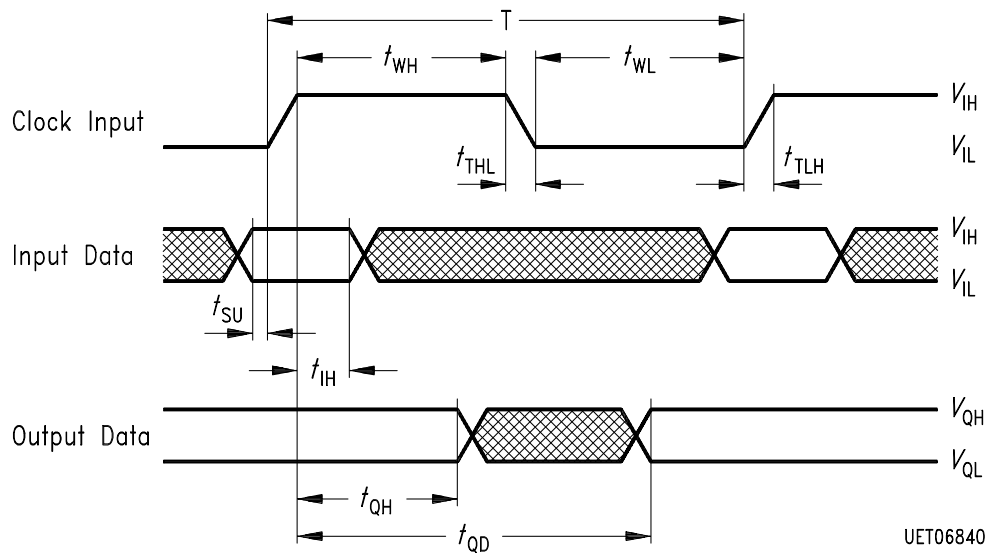
|                          |          |  |     |   |                          |
|--------------------------|----------|--|-----|---|--------------------------|
| Low-level output voltage | $V_{OL}$ |  | 0.5 | V | at $I_{OL} = \text{max}$ |
|--------------------------|----------|--|-----|---|--------------------------|

**Note:** The listed characteristics are ensured over the operating range of the integrated circuit.

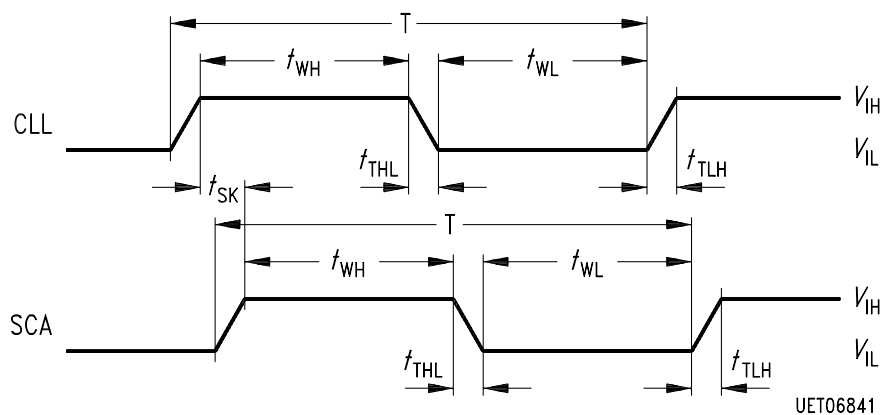
## 4 Application Information



## 5 Waveforms



**Timing Diagram Data Input/Output Referenced to the Clock**

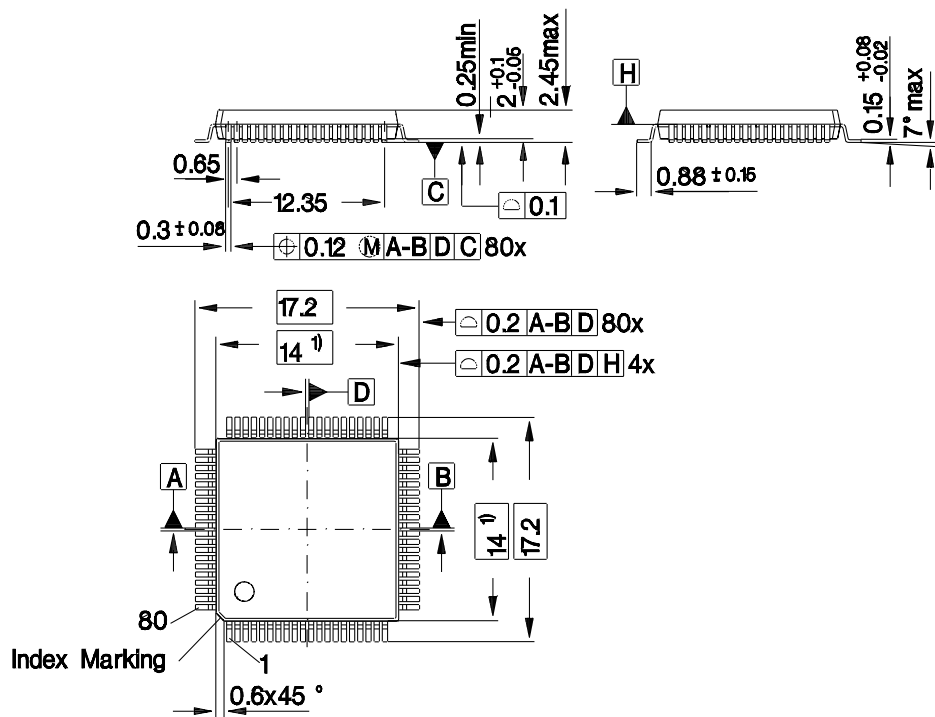


**Timing Diagram Clock Skew SCA - CLL**

## 6 Package Outlines

**P-MQFP-80-1**

(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM05249

## Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

