

5V/12V Synchronous Buck PWM DC-DC and Linear Power Controller

General Description

The RT9218 is a dual output with one synchronous buck PWM and one linear controller. The part is proposed to generate logic-supply voltages for PC based systems. The high-performance device includes internal soft-start, frequency-compensation networks, power good signaling with specific sequence, and it comes all of the logic control, output adjustment, power monitoring and protection functions into a small footprint package. The part is operated at fixed 300kHz frequency providing an optimum compromise between efficiency, external component size, and cost. The linear controller is implemented to drive an external MOSFET for regulation and it's adjustable by setting external resistors. Moreover the specific internal PGOOD sequence and indicator is also implemented to conform to Intel® new platform requirement on FSB_VTT power plane. An adjustable over-current protection (OCP) is proposed to monitor the voltage drop across the RDS(ON) of the lower MOSFET for synchronous buck PWMDC-DC controller.

Ordering Information

RT9218	□	□
	Package Type	
	S : SOP-14	
	Operating Temperature Range	
	P : Pb Free with Commercial Standard	
	G : Green (Halogen Free with Commercial Standard)	

Note :

RichTek Pb-free and Green products are :

- ▶RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶Suitable for use in SnPb or Pb-free soldering processes.
- ▶100% matte tin (Sn) plating.

Features

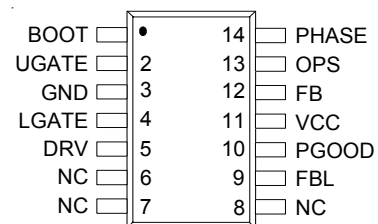
- Operating with 5V or 12V Supply Voltage
- Drives All Low Cost N-MOSFETs
- Voltage Mode PWM Control
- 300kHz Fixed Frequency Oscillator
- Fast Transient Response :
 - ▶High-Speed GM Amplifier
 - ▶Full 0 to 100% Duty Ration
- Internal Soft-Start
- Power Good Indicator
- Adaptive Non-Overlapping Gate Driver
- Over-Current Fault Monitor on MOSFET, No Current Sense Resistor Required
- Specific power good indicator for Intel® Grantsdale FSB_VTT power sequence
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- Graphic Card
- Motherboard, Desktop Servers
- IA Equipments
- Telecomm Equipments
- High Power DC-DC Regulators

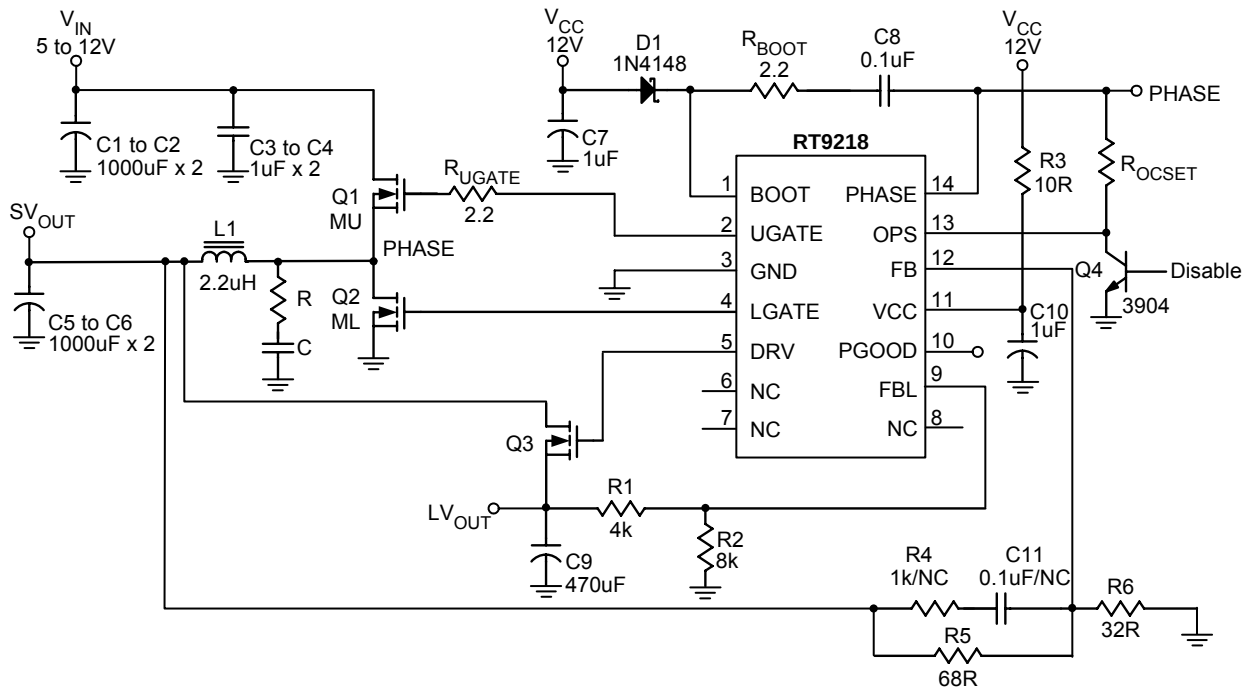
Pin Configurations

(TOP VIEW)



SOP-14

Typical Application Circuit



$$SV_{OUT} = V_{REF} \times \left(1 + \frac{R_5}{R_6}\right)$$

$$LV_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

V_{REF} : Internal reference voltage
(0.8V $\pm$ 2%)

Functional Pin Description

UGATE (Pin 2)

Upper gate driver output. Connect to gate of the high-side power N-MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.

BOOT (Pin 1)

Bootstrap supply pin for the upper gate driver. Connect the bootstrap capacitor between BOOT pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.

PHASE (Pin 14)

Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.

OPS (OCSET, POR and Shut-Down) (Pin 13)

This pin provides multi-function of the over-current setting, UGATE turn-on POR sensing, and shut-down features. Connecting a resistor (R_{OCSET}) between OPS and PHASE pins sets the over-current trip point.

Pulling the pin to ground resets the device and all external MOSFETs are turned off allowing the output voltage power rails to float.

This pin is also used to detect V_{IN} in power on stage and issues an internal POR signal.

LGATE (Pin 4)

Lower gate drive output. Connect to gate of the low-side power N-MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.

FB (Pin 12)

Switcher feedback voltage. This pin is the inverting input of the error amplifier. FB senses the switcher output through an external resistor divider network.

VCC (Pin 11)

Connect this pin to a well-decoupled 5V or 12V bias supply. It is also the positive supply for the lower gate driver, LGATE.

GND (Pin 3)

Both signal and power ground for the IC. All voltage levels are measured with respect to this pin. Ties the pin directly to the low-side MOSFET source and ground plane with the lowest impedance.

DRV (Pin 5)

Connect this pin to the base/gate of an external transistor/MOSFET. This pin provides the drive for the linear regulator's pass transistor/MOSFET.

FBL (Pin 9)

Linear regulator feedback voltage. This pin is the inverting input of the error amplifier and protection monitor. Connect this pin to the external resistor divider network of the linear regulator.

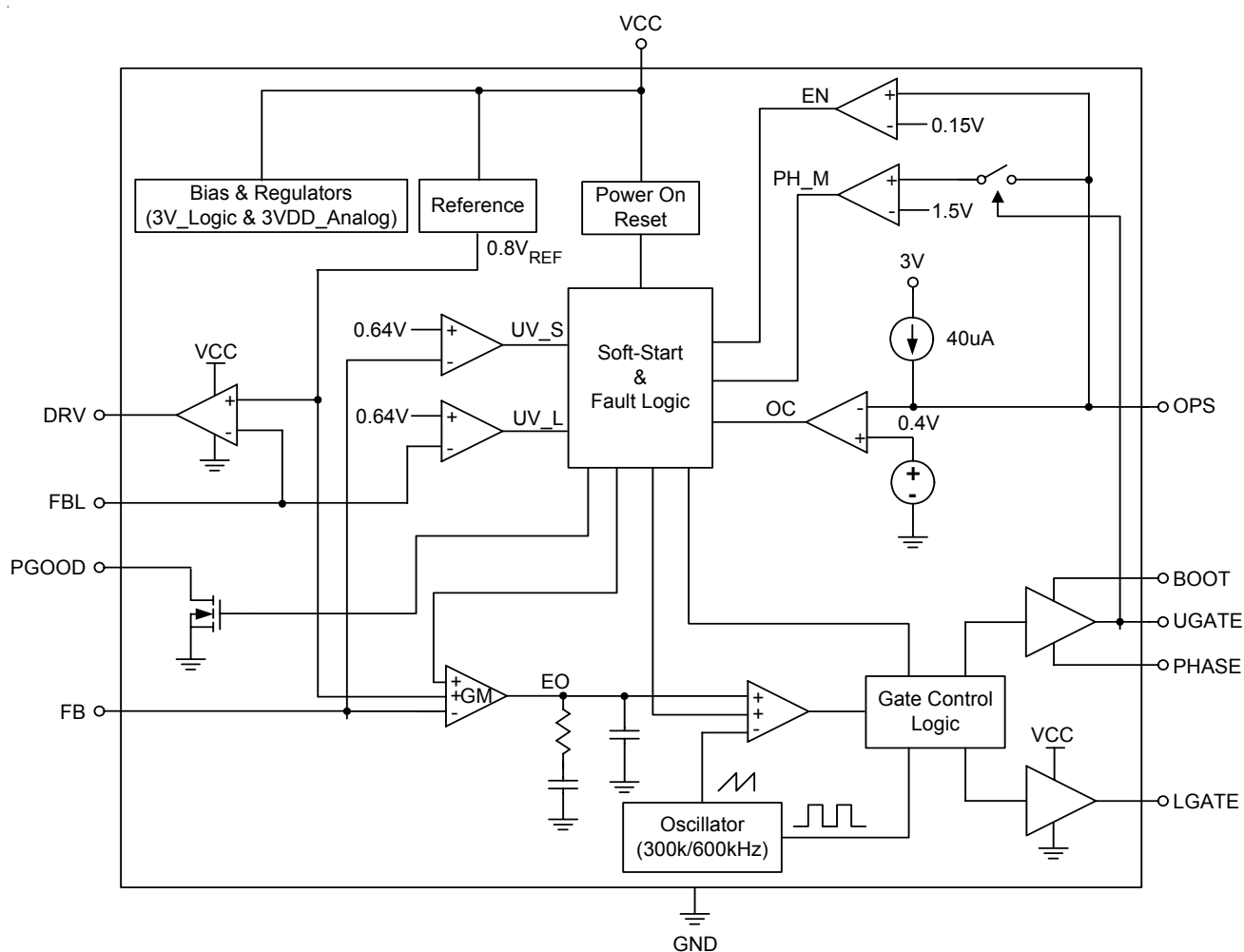
PGOOD (Pin 10)

PGOOD is an open-drain output used to indicate that the regulator is within normal operating voltage ranges and it's implemented with a specific sequence as following chart.

NC (Pin 6,7,8)

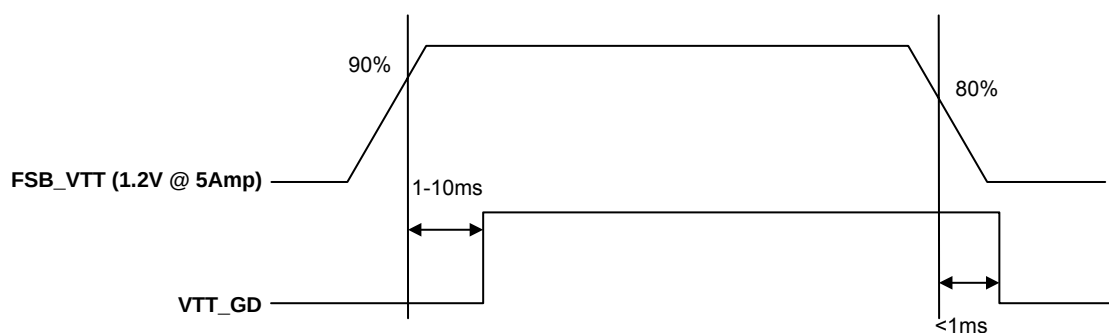
No internal connection.

Function Block Diagram



Timing Diagram

Specific Power Sequence for LDO



Absolute Maximum Ratings (Note 1)

• Supply Voltage, V_{CC}	16V
• BOOT, $V_{BOOT} - V_{PHASE}$	16V
• PHASE to GND	
DC	–5V to 15V
< 200ns	–10V to 30V
• BOOT to PHASE	15V
• BOOT to GND	
DC	–0.3V to $V_{CC}+15V$
< 200ns	–0.3V to 42V
• UGATE	$V_{PHASE} - 0.3V$ to $V_{BOOT} + 0.3V$
• LGATE	GND – 0.3V to $V_{VCC} + 0.3V$
• Input, Output or I/O Voltage	GND – 0.3V to 7V
• Package Thermal Resistance (Note 4)	
SOP-14, θ_{JA}	127.67°C/W
• Junction Temperature	150°C
• Lead Temperature (Soldering, 10 sec.)	260°C
• Storage Temperature Range	–40°C to 150°C
• ESD Susceptibility (Note 2)	
HBM (Human Body Mode)	2kV
MM (Machine Mode)	200V

Recommended Operating Conditions (Note 3)

• Supply Voltage, V_{CC}	5V $\pm$ 5%, 12V $\pm$ 10%
• Junction Temperature Range	–40°C to 125°C
• Ambient Temperature Range	–40°C to 85°C

Electrical Characteristics

($V_{CC} = 5V/12V$, $T_A = 25^\circ C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
V_{CC} Supply Current						
Nominal Supply Current	I_{CC}	UGATE and LGATE Open	--	6	15	mA
Power-On Reset						
POR Threshold	V_{CCRTTH}	V_{CC} Rising	--	4.1	4.5	V
Hysteresis	V_{CCHYS}		0.35	0.5	--	V
Switcher Reference						
Reference Voltage	V_{REF}	$V_{CC} = 12V$	0.784	0.8	0.816	V
Oscillator						
Free Running Frequency	f_{OSC}	$V_{CC} = 12V$	250	300	350	kHz
Ramp Amplitude	ΔV_{OSC}		--	1.5	--	V_{P-P}

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Error Amplifier (GM)						
E/A Transconductance	g_m		--	0.2	--	ms
Open Loop DC Gain	A_O		--	90	--	dB
Linear Regulator						
DRV Driver Source	I_{DS}	$V_{DRV} = 6V$	--	1.4	--	mA
Reference Voltage	V_{REFREG}	$V_{CC} = 12V$	0.784	0.8	0.816	V
PWM Controller Gate Drivers ($V_{CC} = 12V$)						
Upper Gate Source	I_{UGATE}	$V_{BOOT} - V_{PHASE} = 12V$ $V_{UGATE} - V_{PHASE} = 6V$	0.6	1	--	A
Upper Gate Sink	R_{UGATE}	$V_{BOOT} - V_{PHASE} = 12V$ $V_{UGATE} - V_{PHASE} = 1V$	--	4	--	Ω
Lower Gate Source	I_{LGATE}	$V_{CC} = 12V, V_{LGATE} = 6V$	0.6	1	--	A
Lower Gate Sink	R_{LGATE}	$V_{CC} = 12V, V_{LGATE} = 1V$	--	3	4	Ω
Dead Time	T_{DT}		--	--	100	ns
Protection						
FB Under-Voltage Trip	$\Delta FBUVT$	FB Falling	70	75	80	%
FBL Under-Voltage Trip	$\Delta FBLUVT$	FB and FBL Falling	70	75	80	%
OC Current Source	I_{OC}	$V_{PHASE} = 0V$	--	40	--	μA
Soft-Start Interval	T_{SS}		--	3.5	--	ms
Power Good						
Power Good Rising Threshold		$V_{CC} = 12V$	--	90	--	%
Power Good Hysteresis		$V_{CC} = 12V$	--	10	--	%
PG Sink Capability		$V_{CC} = 12V, 1mA$	--	0.2	0.4	V
Power Good Rising Delay		$V_{CC} = 12V$	1	3	10	ms
Power Good Falling Delay		$V_{CC} = 12V$	--	15	--	us

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

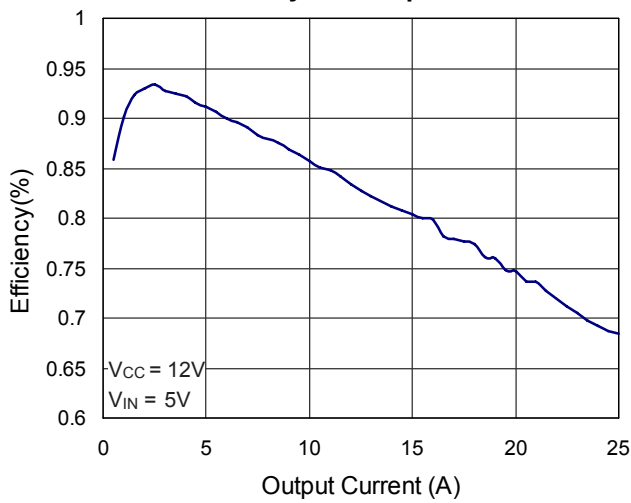
Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

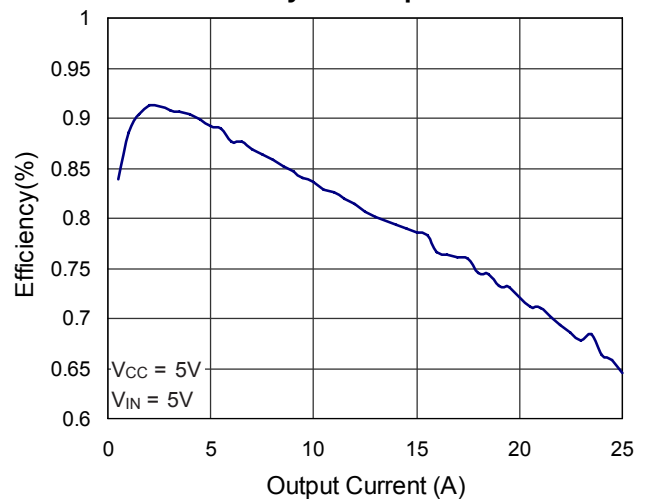
Typical Operating Characteristics

($V_{OUT} = 2.5V$, unless otherwise specified)

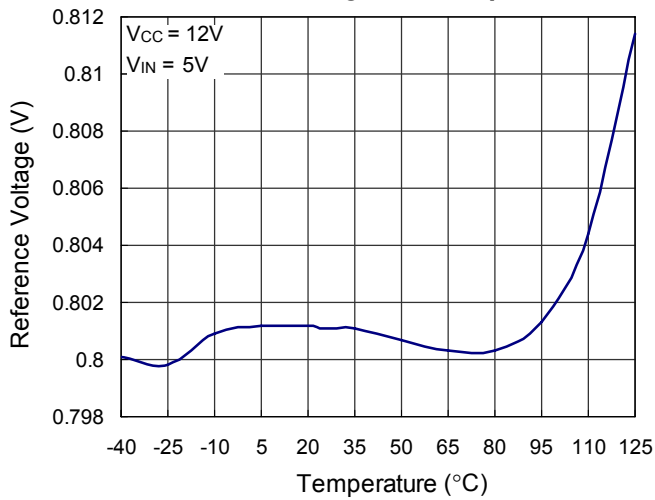
Efficiency vs. Output Current



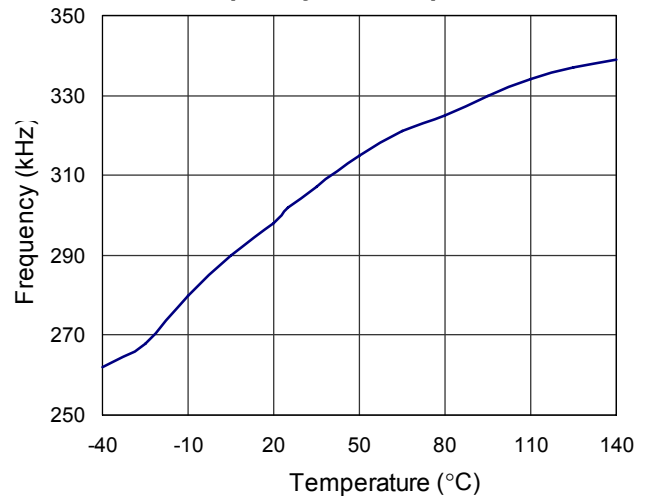
Efficiency vs. Output Current



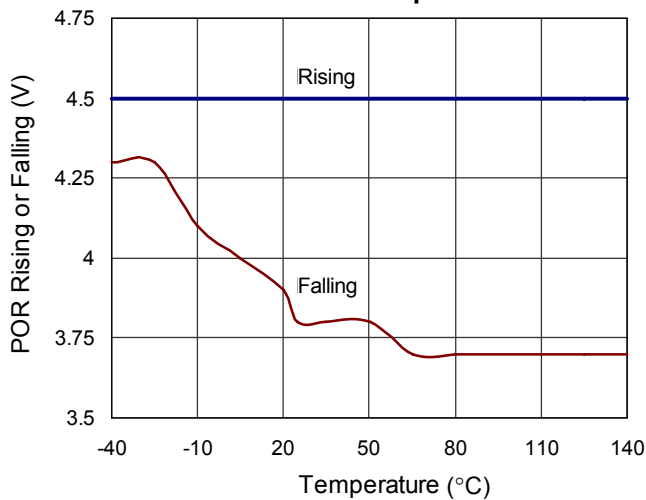
Reference Voltage vs. Temperature



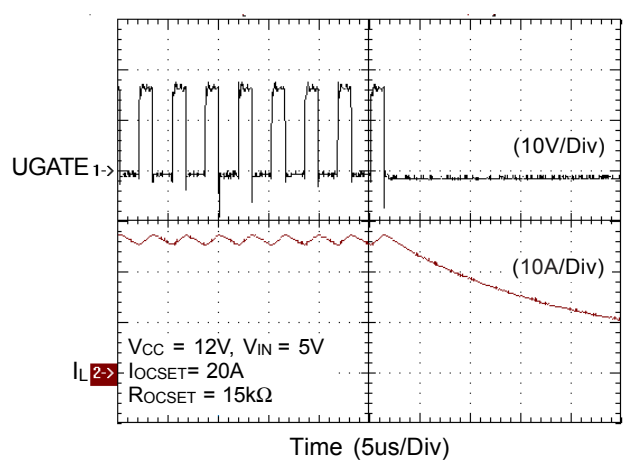
Frequency vs. Temperature

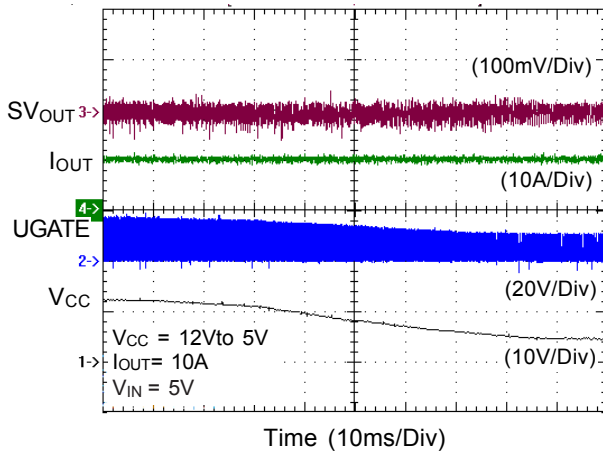
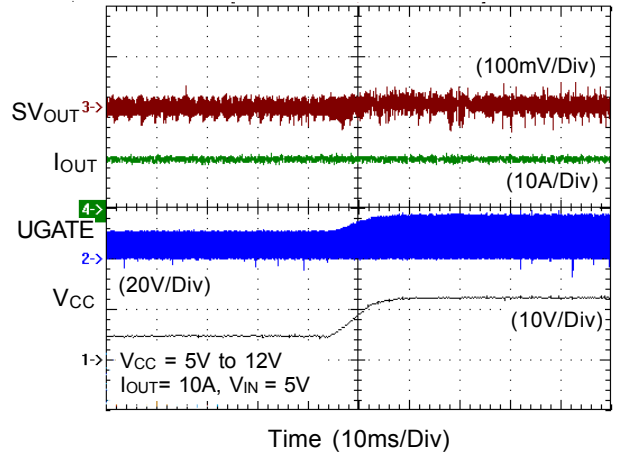


POR vs. Temperature

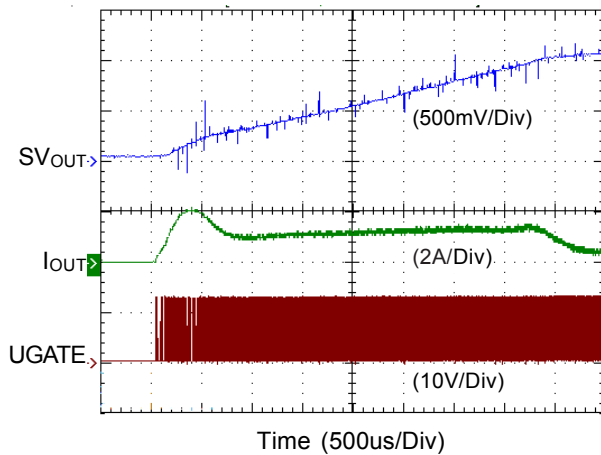


OCP

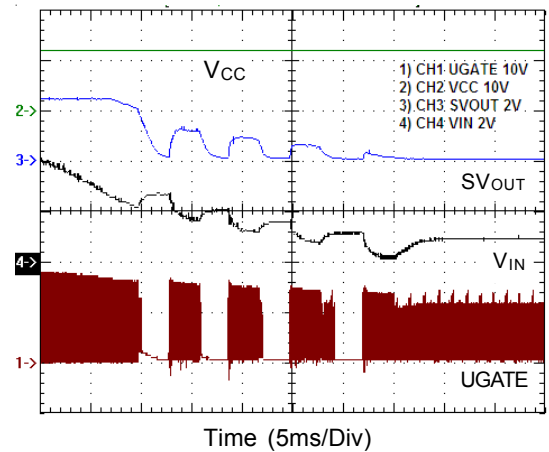


V_{CC} SwitchingV_{CC} Switching

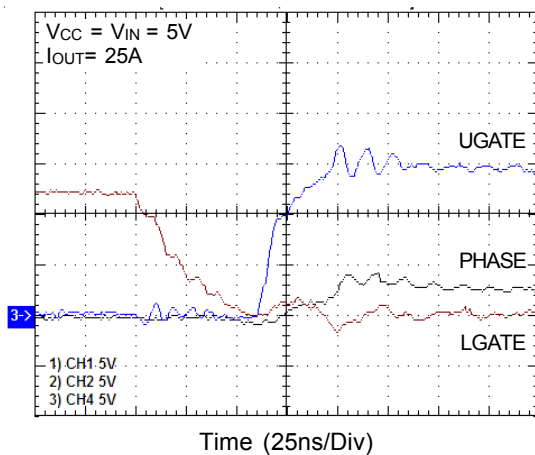
Power On



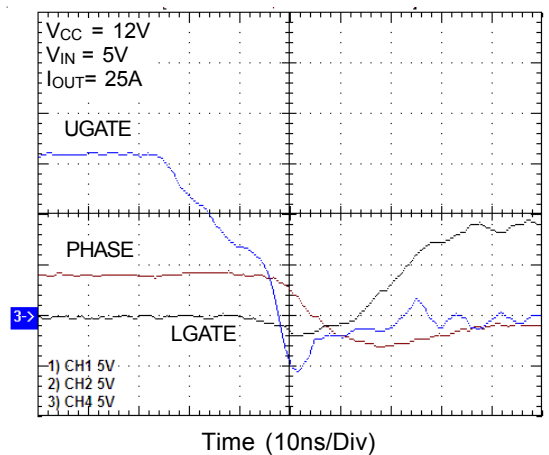
Power Off



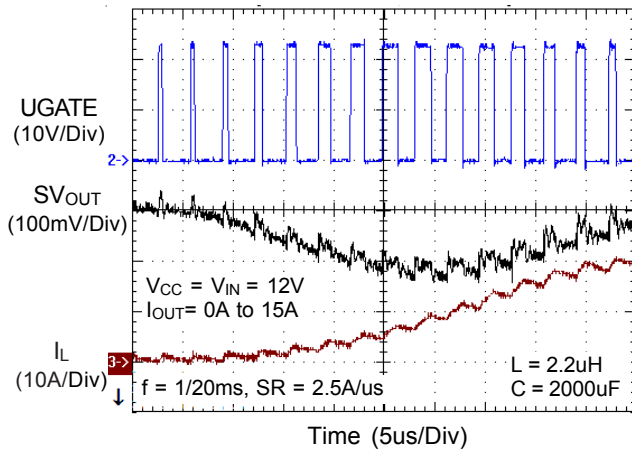
Dead Time (Rising)



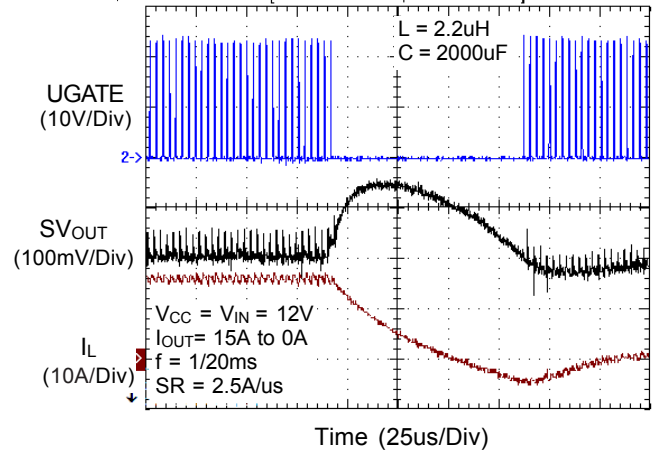
Dead Time (Falling)



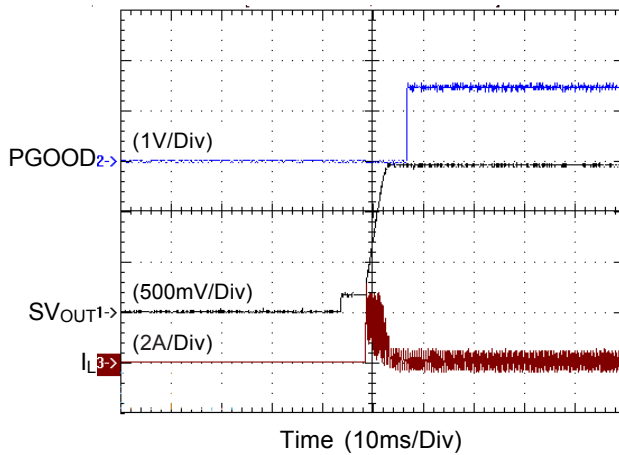
Transient Response (Rising)



Transient Response (Falling)



Soft Start & PGOOD



Application Information

Inductor Selection

The selection of output inductor is based on the considerations of efficiency, output power and operating frequency. Low inductance value has smaller size, but results in low efficiency, large ripple current and high output ripple voltage. Generally, an inductor that limits the ripple current (ΔI_L) between 20% and 50% of output current is appropriate. Figure 1 shows the typical topology of synchronous step-down converter and its related waveforms.

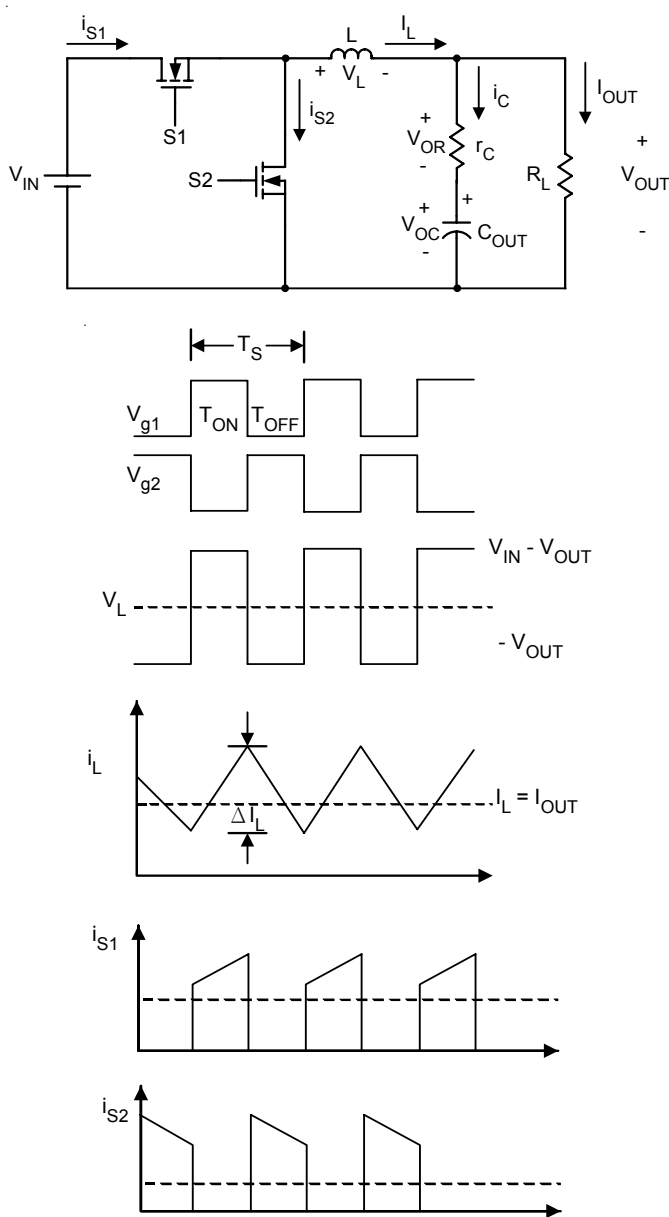


Figure 1. The waveforms of synchronous step-down converter

According to Figure 1 the ripple current of inductor can be calculated as follows :

$$V_{IN} - V_{OUT} = L \frac{\Delta I_L}{\Delta t}; \quad \Delta t = \frac{D}{f_s}; \quad D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times f_s \times \Delta I_L} \quad (1)$$

Where :

V_{IN} = Maximum input voltage

V_{OUT} = Output Voltage

Δt = S1 turn on time

ΔI_L = Inductor current ripple

f_s = Switching frequency

D = Duty Cycle

r_C = Equivalent series resistor of output capacitor

Output Capacitor

The selection of output capacitor depends on the output ripple voltage requirement. Practically, the output ripple voltage is a function of both capacitance value and the equivalent series resistance (ESR) r_C . Figure 2 shows the related waveforms of output capacitor.

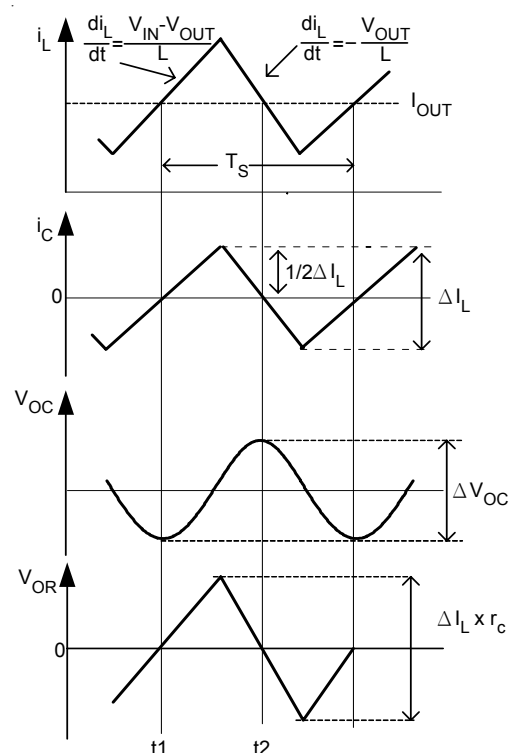


Figure 2. The related waveforms of output capacitor

The AC impedance of output capacitor at operating frequency is quite smaller than the load impedance, so the ripple current (ΔI_L) of the inductor current flows mainly through output capacitor. The output ripple voltage is described as :

$$\Delta V_{OUT} = \Delta V_{OR} + \Delta V_{OC} \quad (2)$$

$$\Delta V_{OUT} = \Delta I_L \times r_c + \frac{1}{C_O} \int_{t_1}^{t_2} i_c dt \quad (3)$$

$$\Delta V_{OUT} = \Delta I_L \times \Delta I_L \times r_c + \frac{1}{8} \frac{V_{OUT}}{C_{OL}} (1-D) T_S^2 \quad (4)$$

where ΔV_{OR} is caused by ESR and ΔV_{OC} by capacitance. For electrolytic capacitor application, typically 90 to 95% of the output voltage ripple is contributed by the ESR of output capacitor. So Equation (4) could be simplified as :

$$\Delta V_{OUT} = \Delta I_L \times r_c \quad (5)$$

Users could connect capacitors in parallel to get calculated ESR.

Input Capacitor

The selection of input capacitor is mainly based on its maximum ripple current capability. The buck converter draws pulsewise current from the input capacitor during the on time of S1 as shown in Figure 1. The RMS value of ripple current flowing through the input capacitor is described as :

$$I_{rms} = I_{OUT} \sqrt{D(1-D)} \quad (A) \quad (6)$$

The input capacitor must be cable of handling this ripple current. Sometime, for higher efficiency the low ESR capacitor is necessarily.

PWM Loop Stability

RT9218 is a voltage mode buck converter using the high gain error amplifier with transconductance (OTA, Operational Transconductance Amplifier).

The transconductance :

$$GM = \frac{dI_{OUT}}{dV_m}$$

The mid-frequency gain :

$$dV_{OUT} = dI_{OUT} Z_{OUT} = GM dV_{IN} Z_{OUT}$$

$$G = \frac{dV_{OUT}}{dV_{IN}} = GM Z_{OUT}$$

Z_{OUT} is the shut impedance at the output node to ground (see Figure 3 and Figure 4),

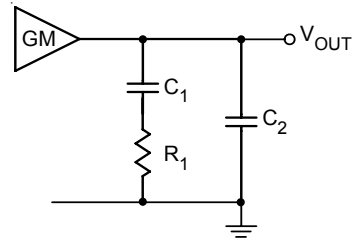


Figure 3. A Type 2 error-amplifier with shut network to ground

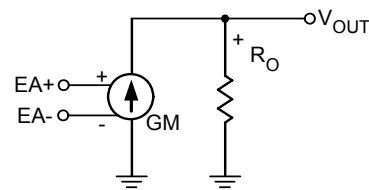


Figure 4. Equivalent circuit

Pole and Zero :

$$F_P = \frac{1}{2\pi \times R_1 C_2}; \quad F_Z = \frac{1}{2\pi \times R_1 C_1}$$

We can see the open loop gain and the Figure 3 whole loop gain in Figure 5.

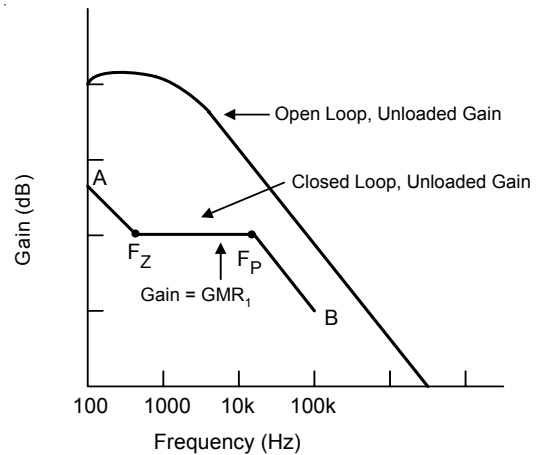


Figure 5. Gain with the Figure 2 circuit

RT9218 internal compensation loop :

$$GM = 0.2ms, R_1 = 75k\Omega, C_1 = 2.5nF, C_2 = 10pF$$

OPS (Over Current Setting, VIN_POR and Shutdown)

1.OCP

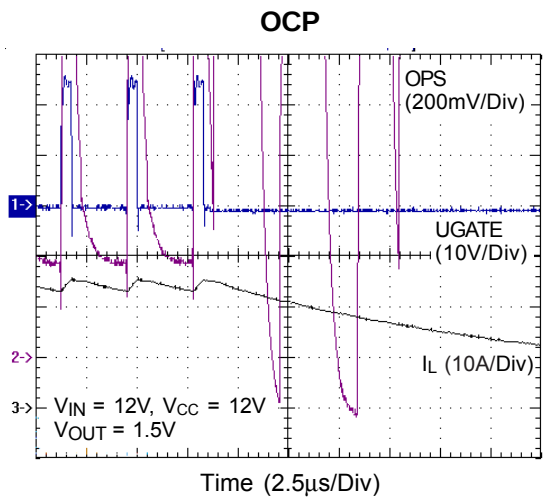
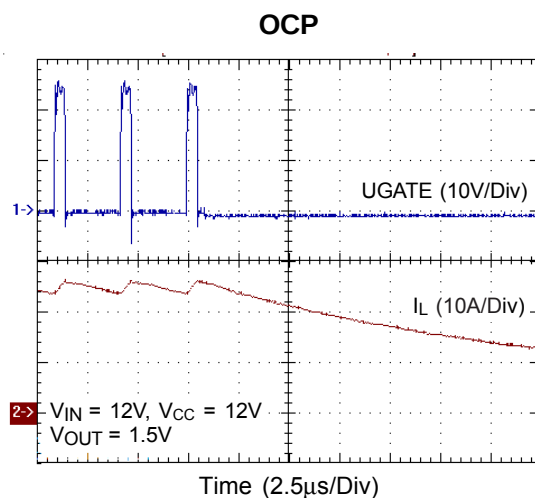
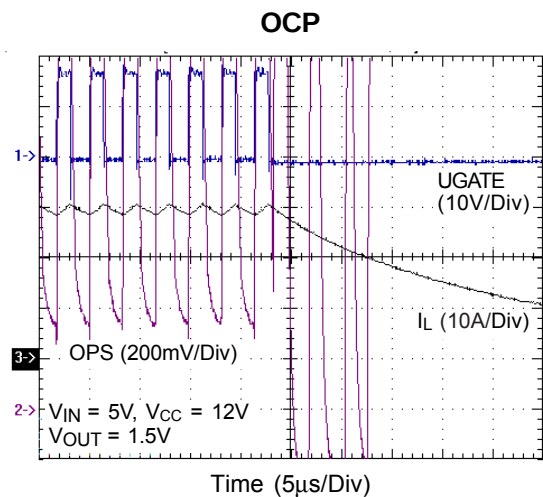
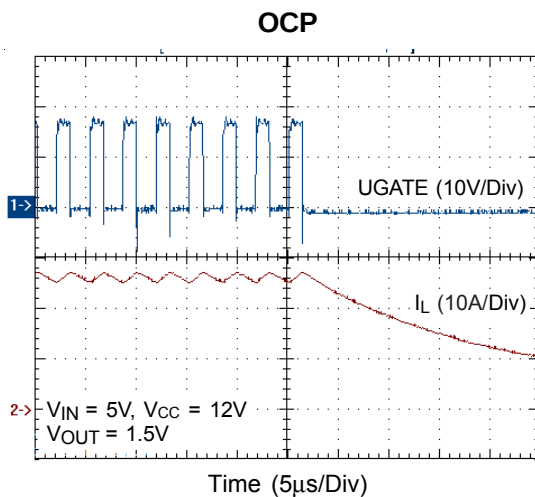
Sense the low-side MOSFET's $R_{DS(ON)}$ to set over-current trip point.

Connecting a resistor (R_{OCSET}) from this pin to the source of the upper MOSFET and the drain of the lower MOSFET sets the over-current trip point. R_{OCSET} , an internal $40\mu A$ current source, and the lower MOSFET on resistance, $R_{DS(ON)}$, set the converter over-current trip point (I_{OCSET}) according to the following equation :

$$I_{OCSET} = \frac{40\mu A \times R_{OCSET} - 0.4V}{R_{DS(ON)} \text{ of the lower MOSFET}}$$

OPS pin function is similar to RC charging or discharging circuit, so the over-current trip point is very sensitive to parasitic capacitance (ex. shut-down MOSFET) and the duty ratio.

Below Figures say those effect. And test conditions are $R_{ocset} = 15k\Omega$ (over -current trip point = 20.6A), Low-side MOSFET is IR3707.



Under Voltage Protection

The voltage at FB and FBL pin is monitored and protected against UV (under voltage). The UV threshold is the FB or FBL under 75%. UV detection has 30 μ s triggered delay. When OC or UV_FBL is trigged, a hiccup restart sequence will be initialized, as shown in Figure 7 Only 4 times of trigger are allowed to latch off. Hiccup is disabled during soft-start interval, but UV_FB has some difference from OC and UV_FBL, it will always trigger V_{IN} power sensing after 4 times hiccup, as shown in Figure 8.

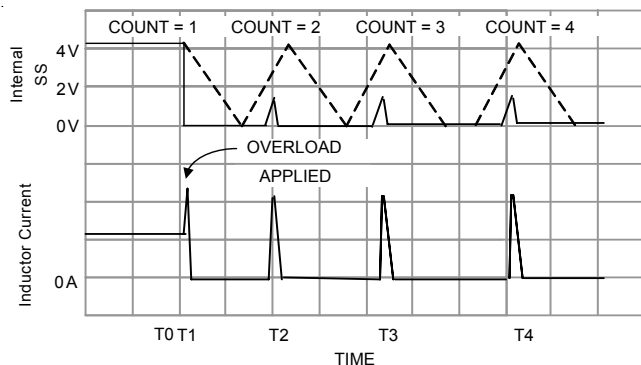


Figure 7. UV and OC trigger hiccup mode

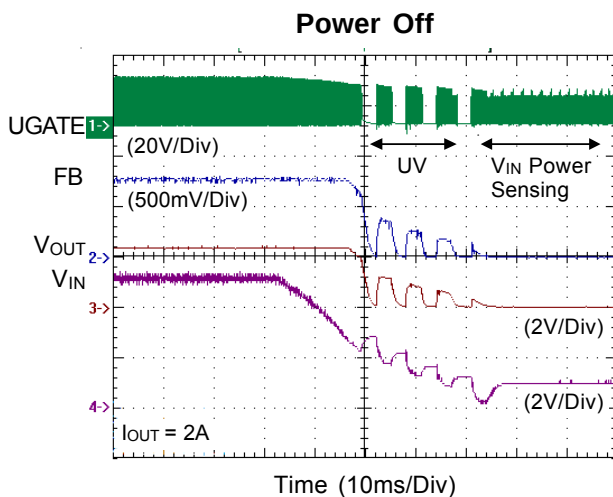


Figure 8, UV_FB trigger V_{IN} power sensing

LDO Power Sequence

In VGA field, the MOSFET of LV_{OUT} is sourced by external voltage not by SV_{OUT} .

This connection may trigger UV protection to shutdown RT9218, but using the typical application circuit won't have this issue. See figure 9 using OPS pin to control the power sequence.

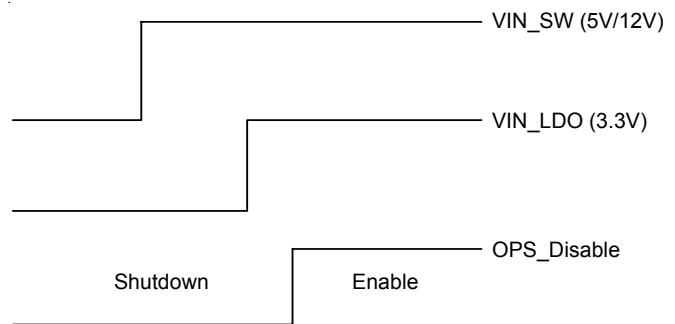


Figure 9. LDO power sequence

PWM Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise, that results in over-voltage stress on devices. Careful component placement layout and printed circuit design can minimize the voltage spikes induced in the converter. Consider, as an example, the turn-off transition of the upper MOSFET prior to turn-off, the upper MOSFET was carrying the full load current. During turn-off, current stops flowing in the upper MOSFET and is picked up by the low side MOSFET or schottky diode. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selections, layout of the critical components, and use shorter and wider PCB traces help in minimizing the magnitude of voltage spikes.

There are two sets of critical components in a DC-DC converter using the RT9218. The switching power components are most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bypass current.

The power components and the PWM controller should be placed firstly. Place the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power switches. Place the output inductor and output capacitors between the MOSFETs and the load. Also locate the PWM controller near by MOSFETs.

A multi-layer printed circuit board is recommended.

Figure 10 shows the connections of the critical components in the converter. Note that the capacitors C_{IN} and C_{OUT} each of them represents numerous physical capacitors. Use a dedicated grounding plane and use vias to ground all critical components to this layer. Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE node, but it is not necessary to oversize this particular island. Since the PHASE node is subjected to very high dV/dt voltages, the stray capacitance formed between these island and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal routing. The PCB traces between the PWM controller and the gate of MOSFET and also the traces connecting source of MOSFETs should be sized to carry 2A peak currents.

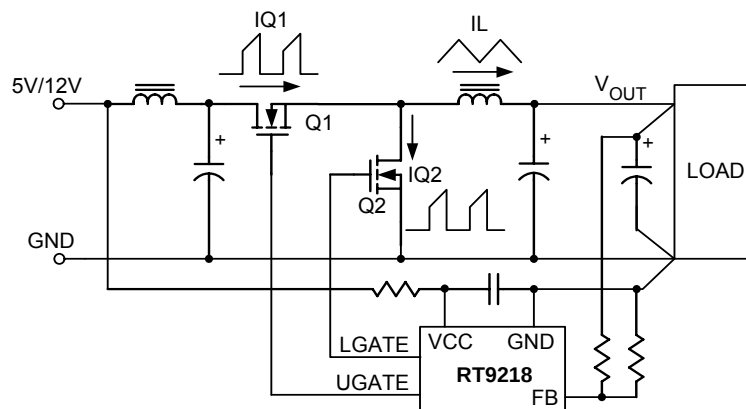
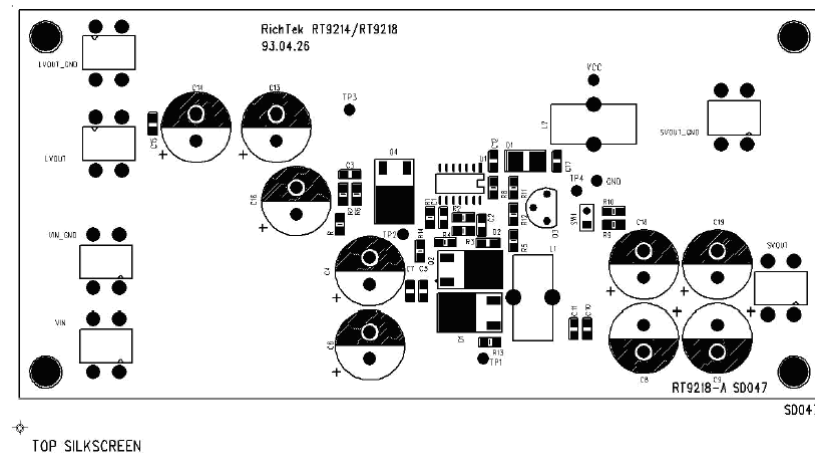
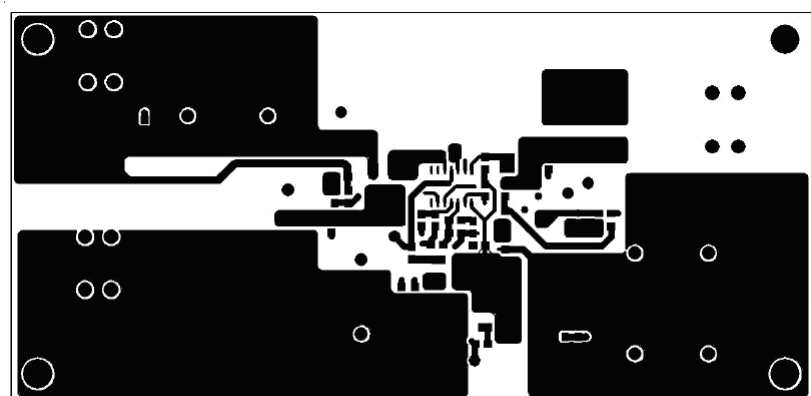


Figure 10. The connections of the critical components in the converter

Below PCB gerber files are our test board for your reference :

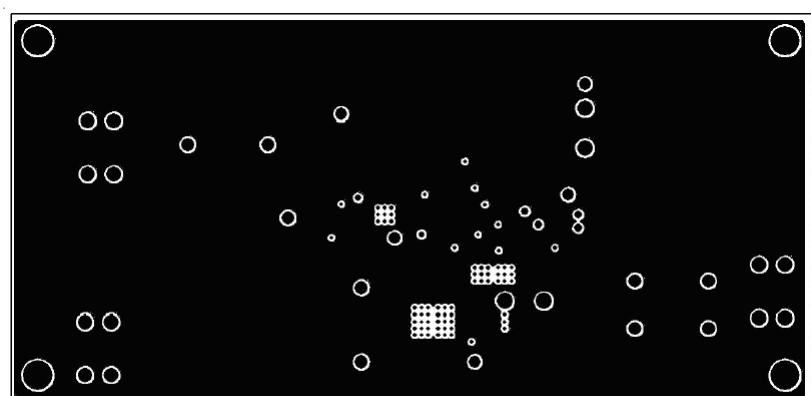




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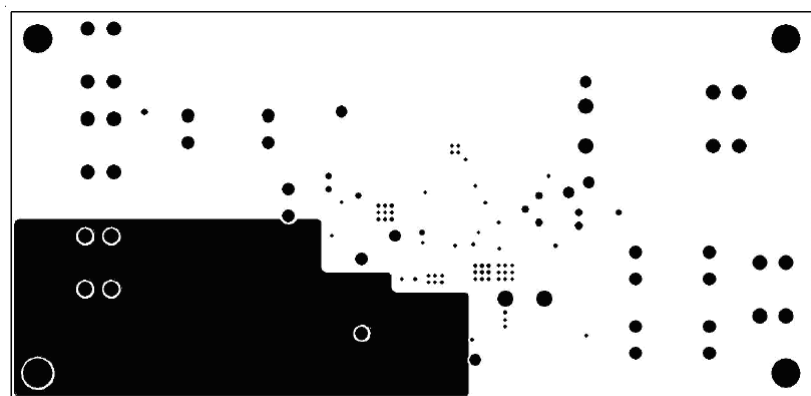
L1 COMPONENT SIDE



S0047



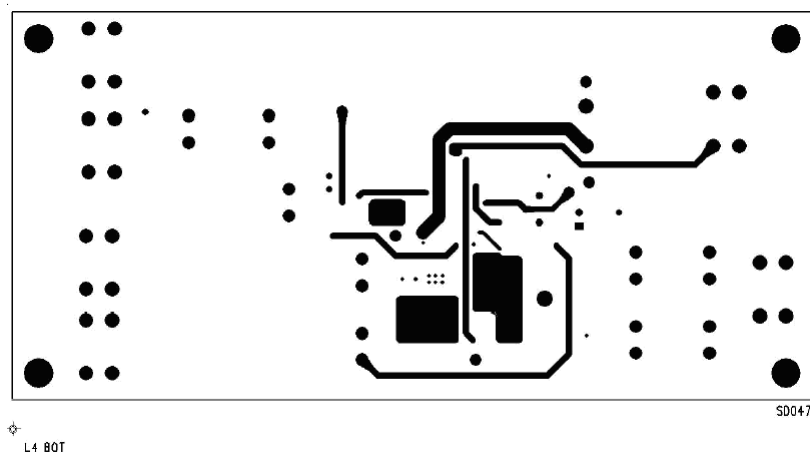
L2 GND



S0047



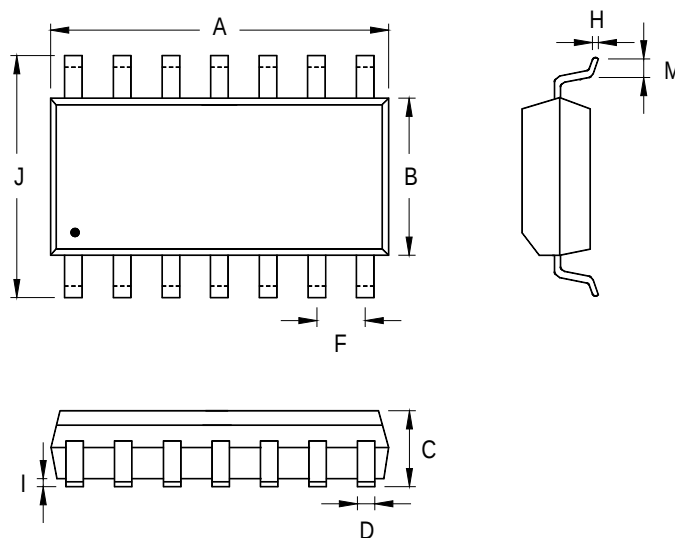
L3 POWER



According to our test experience, you must still notice two items to avoid noise coupling :

- 1.The ground plane should not be separated.
- 2.V_{CC} rail adding the LC filter is recommended.

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	8.534	8.738	0.336	0.344
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

14-Lead SOP Plastic Package

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