

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

**TC74VHC240F,TC74VHC240FT,TC74VHC240FK
TC74VHC244F,TC74VHC244FT,TC74VHC244FK****Octal Bus Buffer****TC74VHC240F/FT/FK**

Inverted, 3-State Outputs

TC74VHC244F/FT/FK

Non-Inverted, 3-State Outputs

The TC74VHC240 and 244 are advanced high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The 74VHC240 is an inverting 3-state buffer having two active-low output enables. The TC74VHC244 is a non-inverting 3-state buffer, and has two active-low output enables.

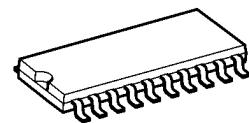
These devices are designed to be used with 3-state memory address drivers, etc.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

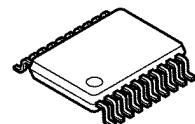
- High speed: $t_{pd} = 3.9$ ns (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4 \mu A$ (max) at $T_a = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 5.5 V
- Low noise: $V_{OLP} = 0.8$ V (max)
- Pin and function compatible with 74ALS240/244

TC74VHC240F, TC74VHC244F



SOP20-P-300-1.27A

TC74VHC240FT, TC74VHC244FT



TSSOP20-P-0044-0.65A

TC74VHC240FK, TC74VHC244FK



VSSOP20-P-0030-0.50

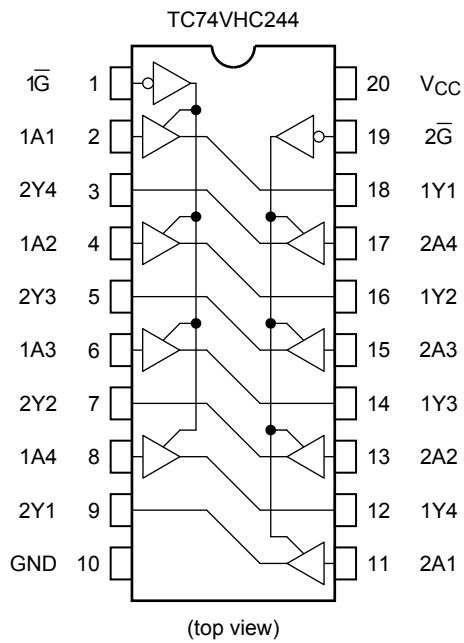
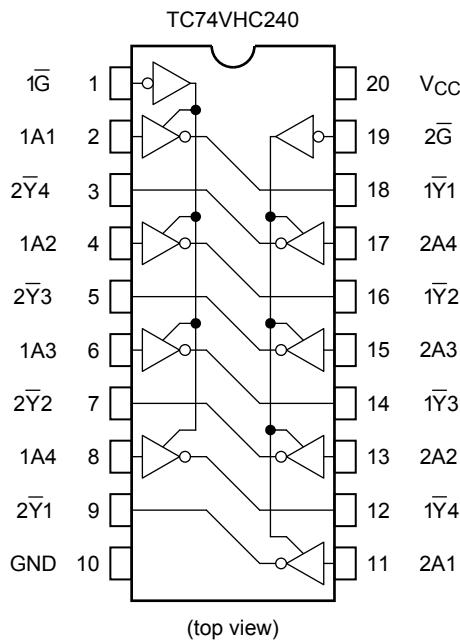
Weight

SOP20-P-300-1.27A : 0.22 g (typ.)

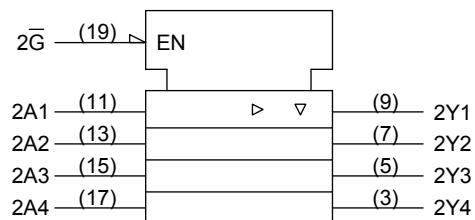
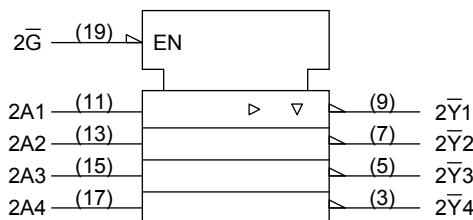
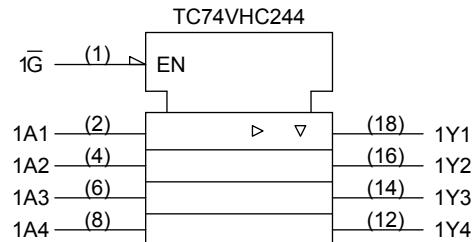
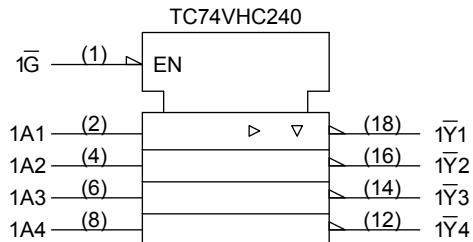
TSSOP20-P-0044-0.65A : 0.08 g (typ.)

VSSOP20-P-0030-0.50 : 0.03 g (typ.)

Pin Assignment



IEC Logic Symbol



Truth Table

Inputs		Outputs	
\bar{G}	A_n	Y_n	\bar{Y}_n
L	L	L	H
L	H	H	L
H	X	Z	Z

X: Don't care

Z: High impedance

Y_n : TC74VHC244

\bar{Y}_n : TC74VHC240

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	–0.5 to 7.0	V
DC input voltage	V_{IN}	–0.5 to 7.0	V
DC output voltage	V_{OUT}	–0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	–20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{STG}	–65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{OPR}	–40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V _{CC} (V)	Ta = 25°C			Ta = -40 to 85°C		Unit
					Min	Typ.	Max	Min	Max	
High-level input voltage	V _{IH}	—	—	2.0	1.50	—	—	1.50	—	V
				3.0 to 5.5	V _{CC} × 0.7	—	—	V _{CC} × 0.7	—	
Low-level input voltage	V _{IL}	—	—	2.0	—	—	0.50	—	0.50	V
				3.0 to 5.5	—	—	V _{CC} × 0.3	—	V _{CC} × 0.3	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
		V _{IN} = V _{IH} or V _{IL}	I _{OH} = -4 mA	3.0	2.58	—	—	2.48	—	V
				4.5	3.94	—	—	3.80	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
		V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	I _{OL} = 4 mA	3.0	—	—	0.36	—	0.44	V
				4.5	—	—	0.36	—	0.44	
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND	0 to 5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	4.0	—	40.0	μA	

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
		V _{CC} (V)	C _L (pF)	Min	Typ.	Max	Min	Max		
Propagation delay time (TC74VHC240)	t _{pLH}	—	3.3 ± 0.3	15	—	5.3	7.5	1.0	9.0	
				50	—	7.8	11.0	1.0	12.5	
	t _{pHL}		5.0 ± 0.5	15	—	3.6	5.5	1.0	6.5	
				50	—	5.1	7.5	1.0	8.5	
	t _{pLH}	—	3.3 ± 0.3	15	—	5.8	8.4	1.0	10.0	
				50	—	8.3	11.9	1.0	13.5	
	t _{pHL}		5.0 ± 0.5	15	—	3.9	5.5	1.0	6.5	
				50	—	5.4	7.5	1.0	8.5	
3-state output enable time	t _{pZL}	R _L = 1 kΩ	3.3 ± 0.3	15	—	6.6	10.6	1.0	12.5	
				50	—	9.1	14.1	1.0	16.0	
	t _{pZH}		5.0 ± 0.5	15	—	4.7	7.3	1.0	8.5	
				50	—	6.2	9.3	1.0	10.5	
3-state output disable time	t _{pLZ}	R _L = 1 kΩ	3.3 ± 0.3	50	—	10.3	14.0	1.0	16.0	
			5.0 ± 0.5	50	—	6.7	9.2	1.0	10.5	
Output to output skew	t _{osLH}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	C _{IN}	—		—	4	10	—	10	pF	
Output capacitance	C _{OUT}	—		—	6	—	—	—	pF	
Power dissipation capacitance (Note 2)	C _{PD}	TC74VHC240		—	17	—	—	—	pF	
		TC74VHC244		—	19	—	—	—		

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

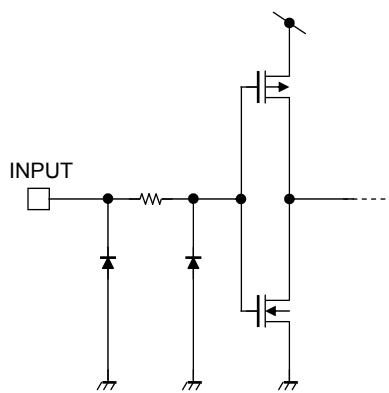
Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

Noise Characteristics (input: $t_r = t_f = 3$ ns)

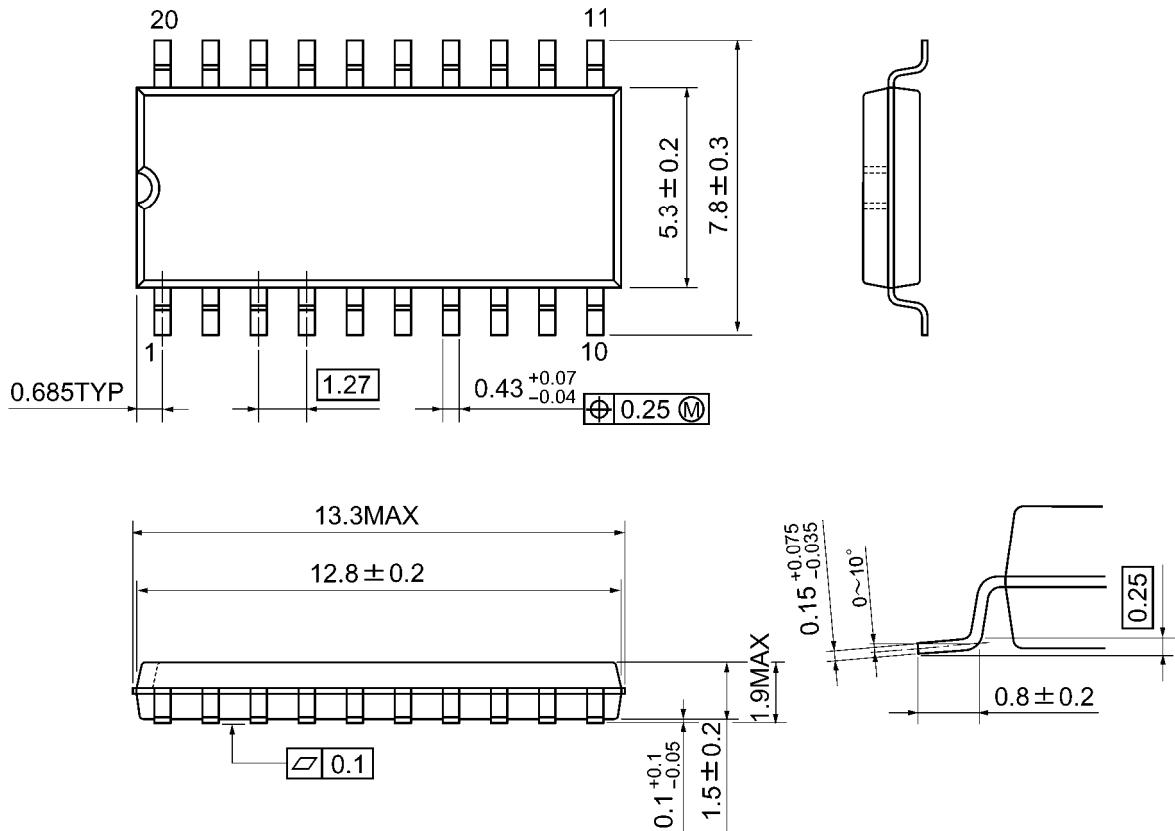
Characteristics	Symbol	Test Condition			Ta = 25°C		Unit
		V _{CC} (V)	Typ.	Limit	V		
Quiet output maximum dynamic V _{OL}	V _{OLP}	C _L = 50 pF	5.0	0.5	0.8		V
Quiet output minimum dynamic V _{OL}	V _{OLV}	C _L = 50 pF	5.0	-0.5	-0.8		V
Minimum high level dynamic input voltage	V _{IHD}	C _L = 50 pF	5.0	—	3.5		V
Maximum low level dynamic input voltage	V _{ILD}	C _L = 50 pF	5.0	—	1.5		V

Input Equivalent Circuit

Package Dimensions

SOP20-P-300-1.27A

Unit: mm

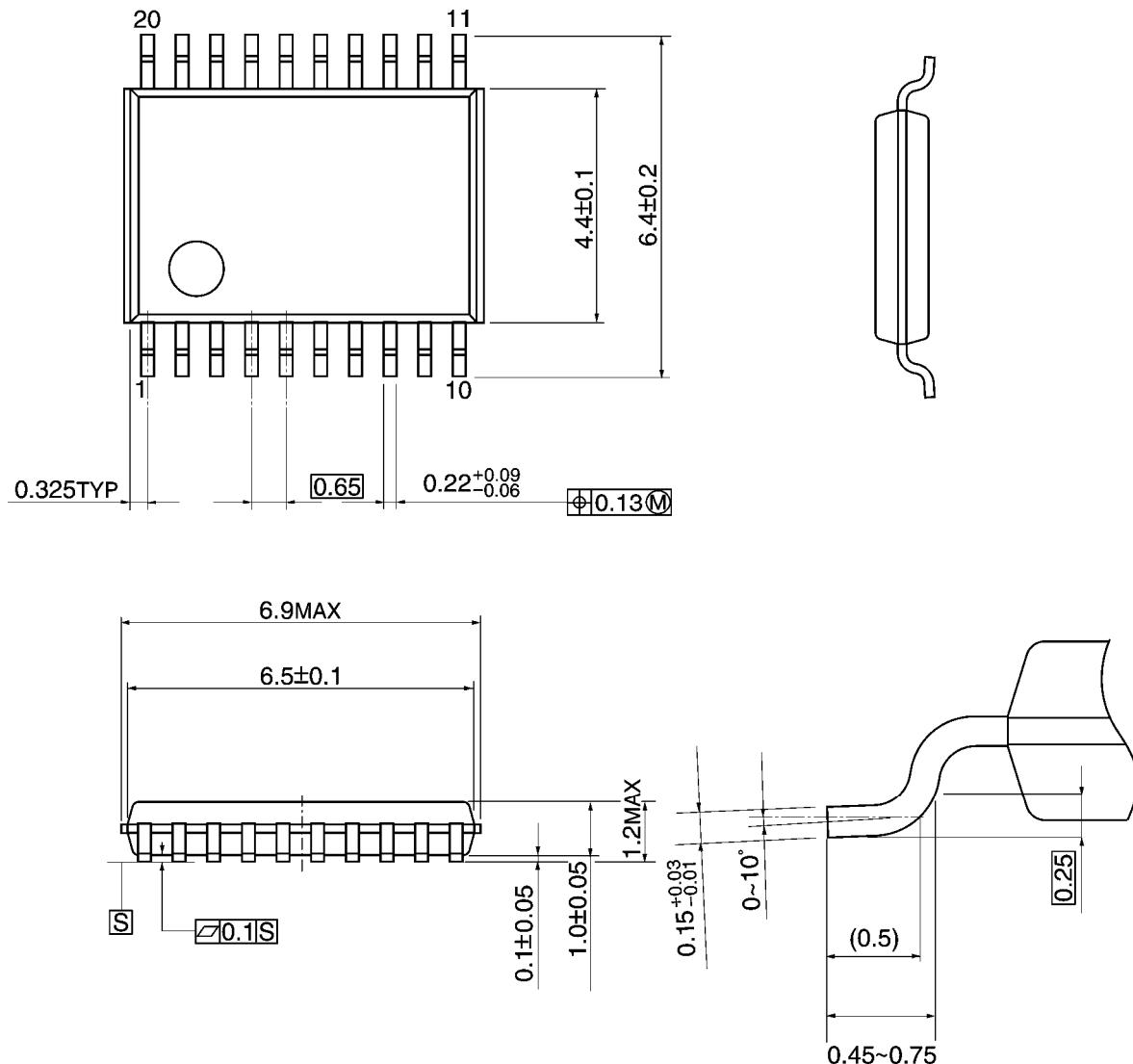


Weight: 0.22 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm

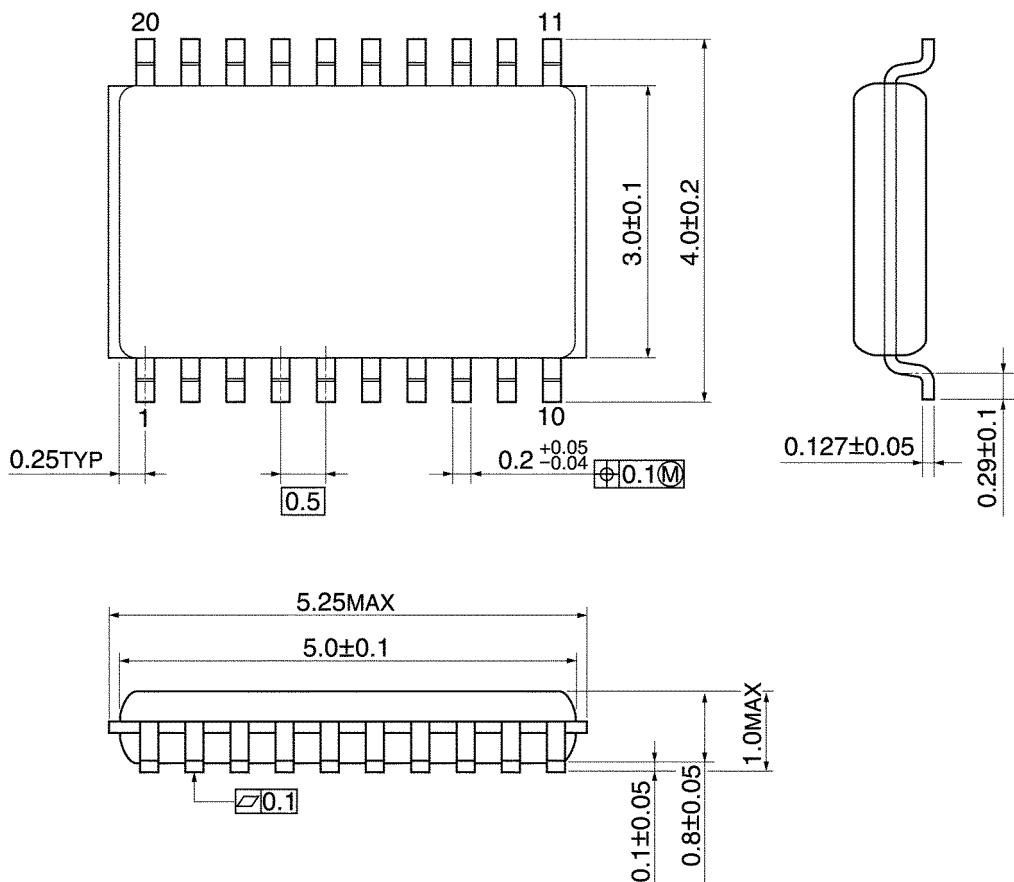


Weight: 0.08 g (typ.)

Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

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