R8C/15 Group

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0078-0010Z
Rev.0.10
Mar 4, 2004

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 20-pin plastic molded SSOP or SDIP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.
The data flash ROM (1 KB X 2 blocks) is embedded.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Outline

Table 1.1 lists the performance outline of this MCU.

Table 1.1 Performance Outline

Item		Performance
CPU	Number of Basic Instructions	89 instructions
	Shortest Instruction Execution Time	50ns(f(XIN)=20MHz, VCC=3.0 to 5.5V) 100ns(f(XIN)=10MHz, VCC=2.7 to 5.5V)
	Operation Mode	Single-chip
	Memory Space	1Mbyte
	Memory Capacity	See **Table 1.2 Product List**
Peripheral Function	Port	Input/Output : 13 pins (including LED drive port), Input : 2 pin
	LED drive port	I/O port: 4 pins, max. 20 mA
	Timer	Timer X: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel (Circuits of input capture and output compare)
	Serial I/O	1 channel Clock synchronous, UART
	Chip-select clock synchronous serial I/O (SSUA)	1 channel
	A-D Converter	10-bit A-D converter: 1 circuit, 4 channels
	Watchdog Timer	15 bits x 1 channel (with prescaler) Reset start selectable, Count source protection mode
	Interrupt	Internal: 9 sources, External: 4 sources, Software: 4 sources, Priority level: 7 levels
	Clock Generating Circuit	2 circuits Main clock generation circuit (Equipped with a built-in feedback resistor) Ring oscillator (high speed, low speed) On High-speed ring oscillator the frequency adjustment function is usable.
	Oscillation Stop Detection Function	Stop detection of main clock oscillation
	Voltage Detection Circuit	Included
	Power on Reset Circuit	Included
Electric Characteristics	Supply Voltage	VCC=3.0 to 5.5V (f(XIN)=20MHz) VCC=2.7 to 5.5V (f(XIN)=10MHz)
	Power Consumption	TBD (VCC=5V, f(XIN)=20MHz) TBD (VCC=3V, f(XIN)=10MHz) TBD (VCC=3V, wait mode) TBD (VCC=3V, stop mode)
Flash Memory	Program/Erase Supply Voltage	VCC=2.7 to 5.5V
	Program and Erase Endurance	10000 times (Data area) 100 times (Program area)
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (Option(1))
Package		20-pin plastic mold SSOP 20-pin plastic mold SDIP

NOTES:
1. All options are on request basis.

1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

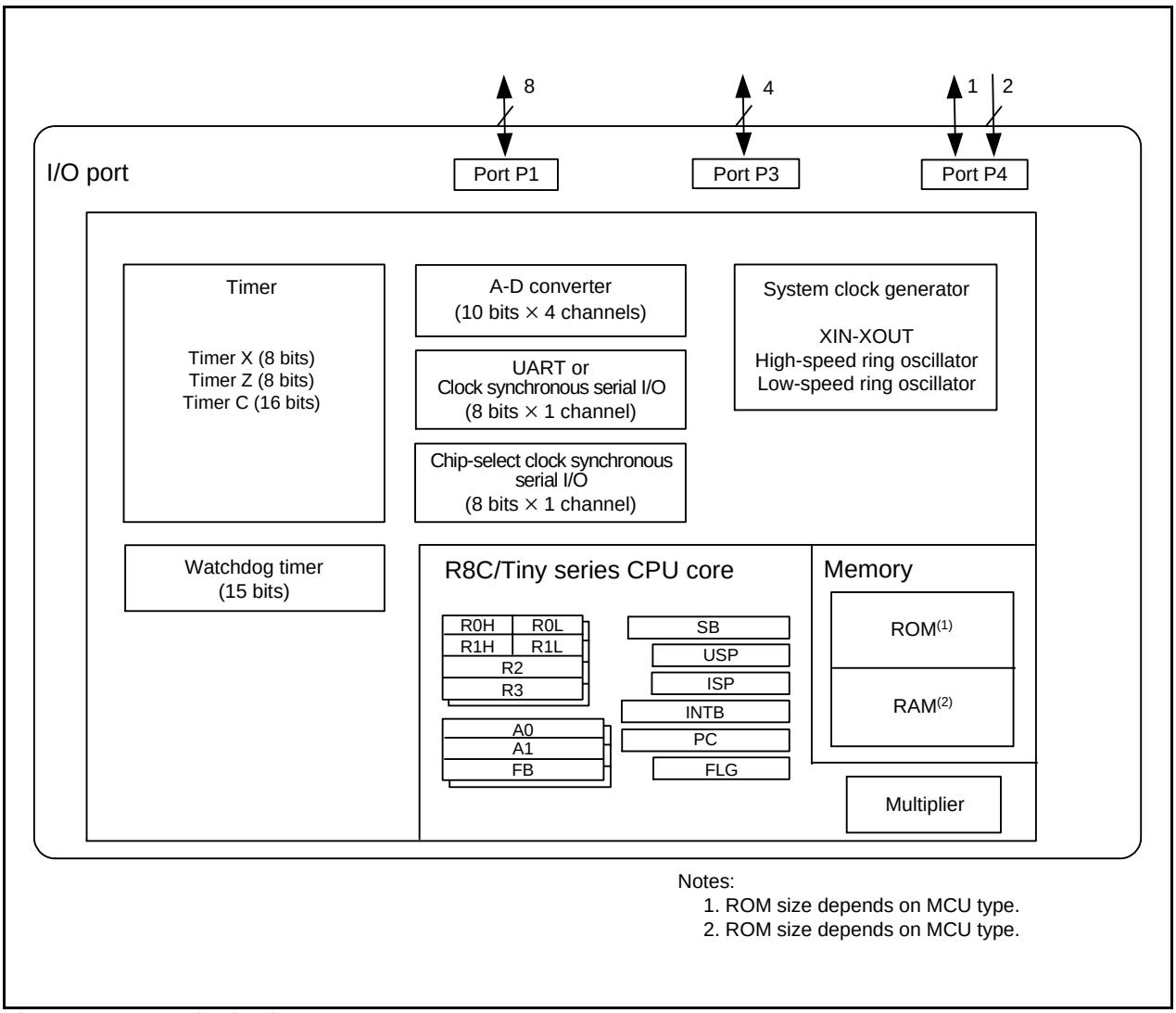


Figure 1.1 Block Diagram

1.4 Product List

Table 1.2 lists the products.

Table 1.2 Product List **As of Mar. 2004**

Type No.	ROM capacity		RAM capacity	Package type	Remarks
R5F21152SP (D)	8K bytes	1K bytes X 2	512 bytes	20P2F-A	Flash memory version
R5F21153SP (D)	12K bytes	1K bytes X 2	768 bytes	20P2F-A	
R5F21154SP (D)	16K bytes	1K bytes X 2	1K bytes	20P2F-A	
R5F21152DSP (D)	8K bytes	1K bytes X 2	512 bytes	20P2F-A	D version
R5F21153DSP (D)	12K bytes	1K bytes X 2	768 bytes	20P2F-A	
R5F21154DSP (D)	16K bytes	1K bytes X 2	1K bytes	20P2F-A	
R5F21152DD (P)	8K bytes	1K bytes X 2	512 bytes	20P4B	Flash memory version
R5F21153DD (P)	12K bytes	1K bytes X 2	768 bytes	20P4B	
R5F21154DD (P)	16K bytes	1K bytes X 2	1K bytes	20P4B	
R5F21152DDD (P)	8K bytes	1K bytes X 2	512 bytes	20P4B	D version
R5F21153DDD (P)	12K bytes	1K bytes X 2	768 bytes	20P4B	
R5F21154DDD (P)	16K bytes	1K bytes X 2	1K bytes	20P4B	

(D): Under development, (P): Planning

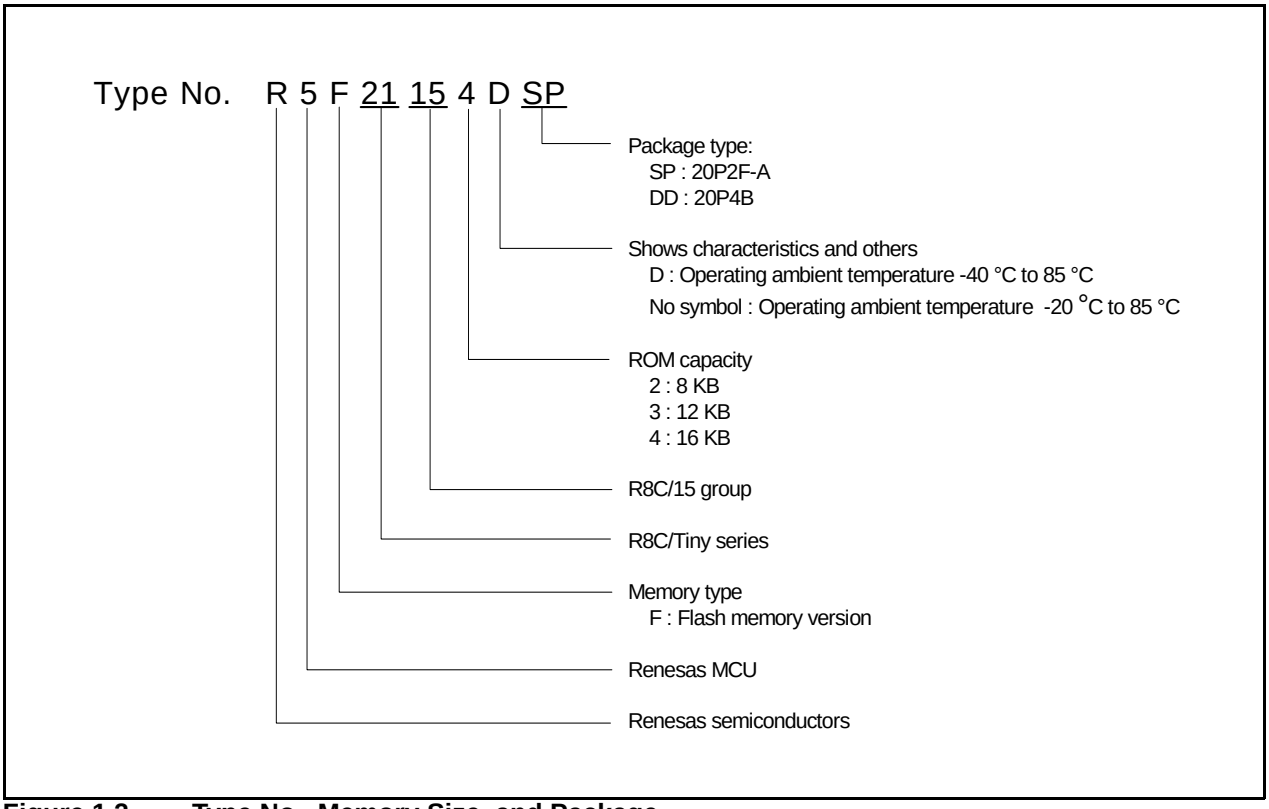


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Configuration

Figure 1.3 shows the 20P2F-A package pin configuration (top view) and Figure 1.4 shows the 20P4B package pin configuration (top view).

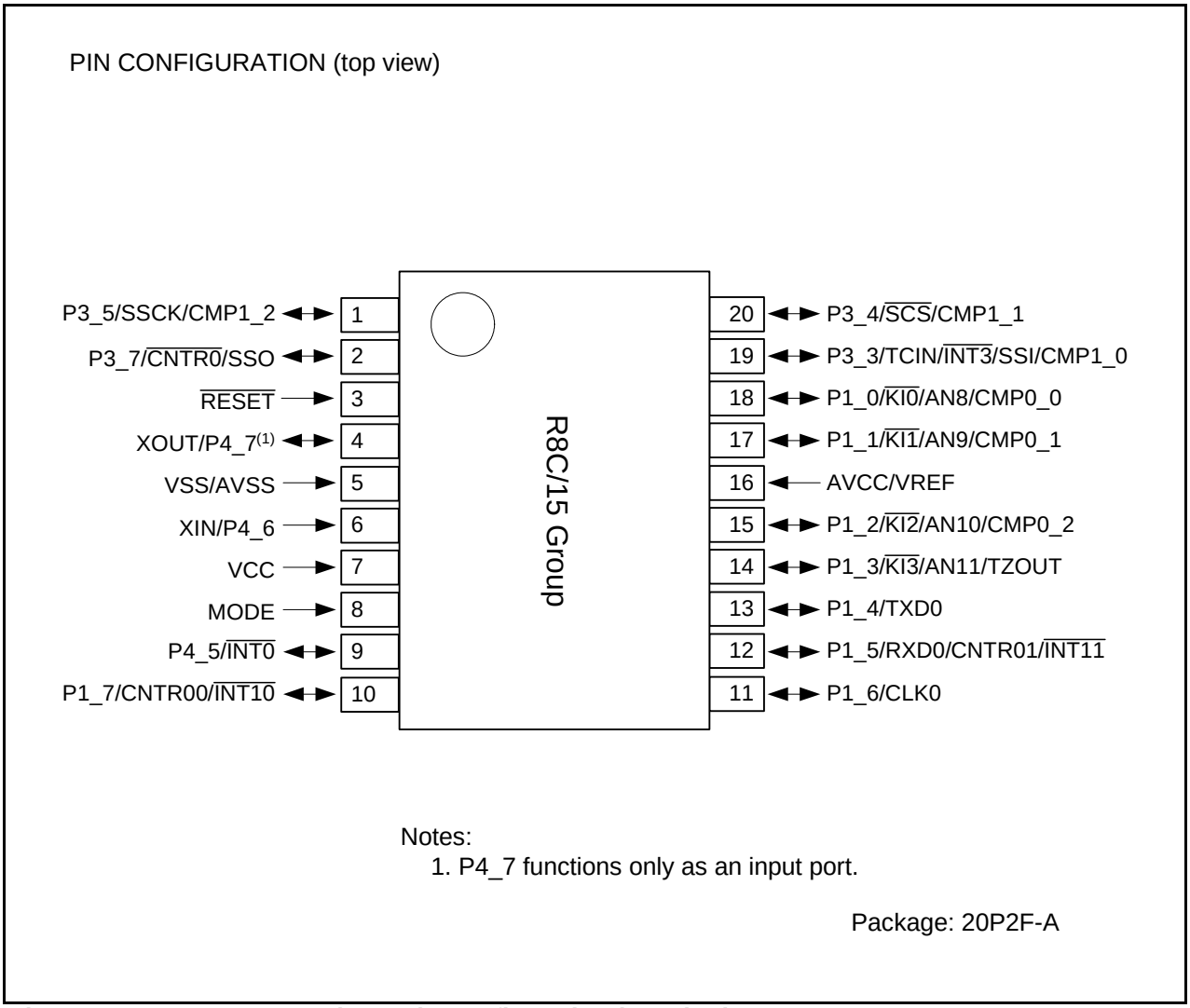
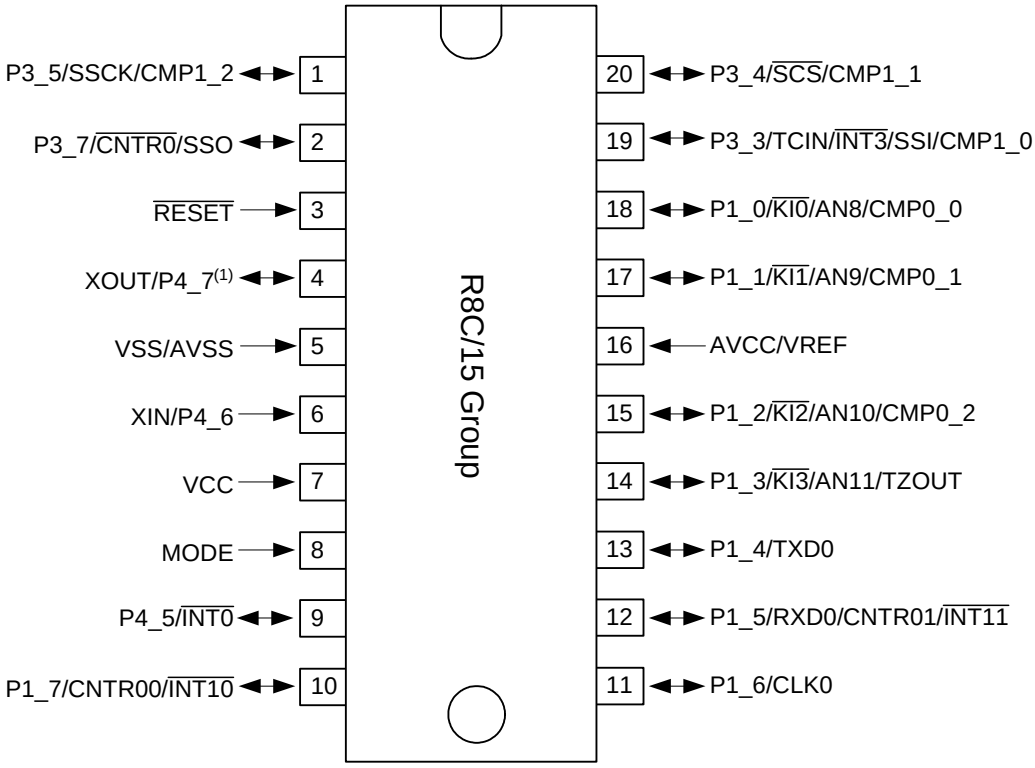


Figure 1.3 20P2F-A Package Pin Configuration (top view)

PIN CONFIGURATION (top view)



Notes:
1. P4_7 functions only as an input port.

Package: 20P4B

Figure 1.4 20P4B Package Pin Configuration (top view)

1.6 Pin Description

Table 1.3 shows the pin description

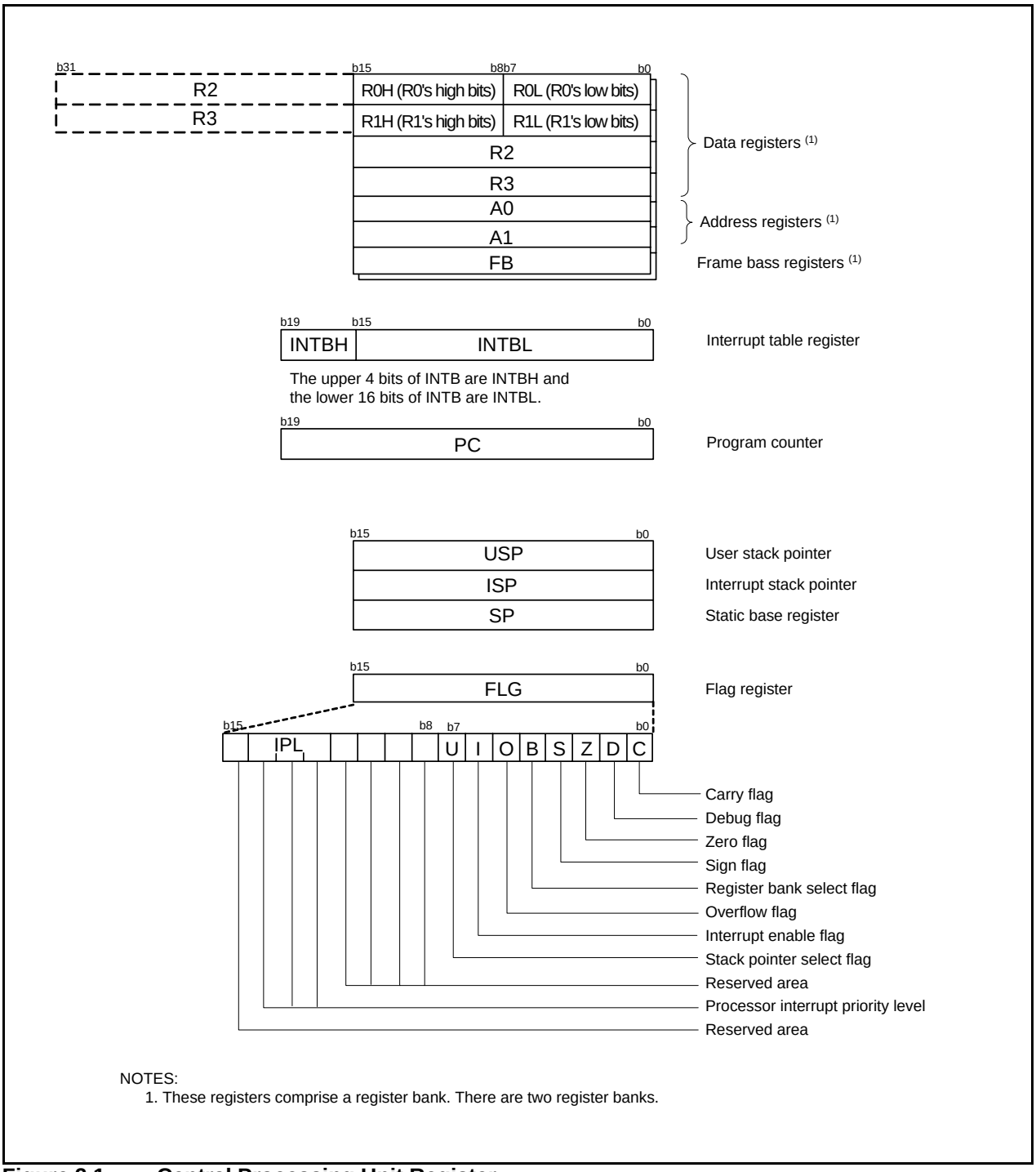
Table 1.3 Pin Description

Signal name	Pin name	I/O type	Function
Power supply input	VCC VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Reset input	$\overline{\text{RESET}}$	I	"L" on this input resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Main clock input	XIN	I	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
INT interrupt input	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	These are INT interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	These are key input interrupt input pins.
Timer X	CNTR0	I/O	This is the timer X I/O pin.
	$\overline{\text{CNTR0}}$	O	This is the timer X output pin.
Timer Z	TZOUT	O	This is the timer Z output pin.
Timer C	TCIN	I	This is the timer C input pin.
	CMP0_0 to CMP0_3, CMP1_0 to CMP1_3	O	These are the timer C output pins.
Serial interface	CLK0	I/O	This is a transfer clock I/O pin.
	RXD0	I	These are serial data input pins.
	TXD0	O	These are serial data output pins.
SSUA	SSI	I/O	This is a data I/O pin.
	$\overline{\text{SCS}}$	I/O	This is a chip-select signal I/O pin.
	SSCK	I/O	This is a clock I/O pin.
	SSO	I/O	This is a data I/O pin.
Reference voltage input	VREF	I	This is a reference voltage input pin for A-D converter.
A-D converter	AN8 to AN11	I	These are analog input pins for A-D converter.
I/O port	P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5	I/O	These are CMOS I/O ports. Each port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P1_0 to P1_7 also function as LED drive ports.
Input port	P4_6, P4_7	I	These are input only pins.

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.



NOTES:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.
The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.
In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.
Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.
Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is cleared to “0” when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.
The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

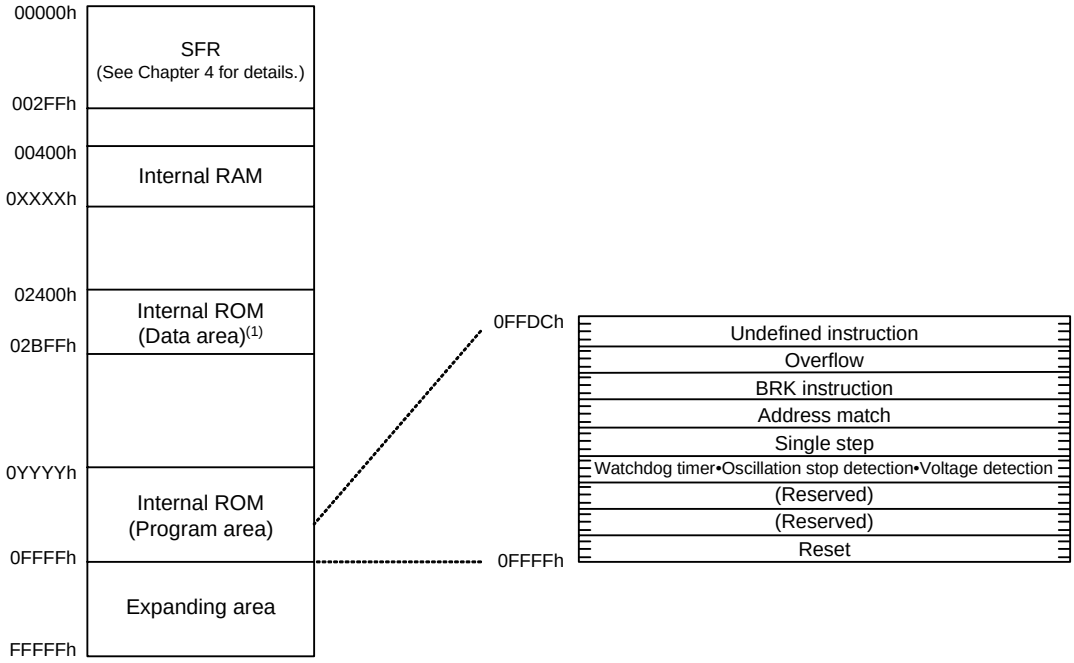
IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write “0”. When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of this MCU. The address space extends the 1M bytes from address 00000h to FFFFFh.
The internal ROM (program area) is allocated in a lower address direction beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated to the addresses from 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated to the addresses from 0FFDCh to 0FFFFh. Therefore, store the start address of each interrupt routine here.
The internal ROM (data area) is allocated to the addresses from 02400h to 02BFFh.
The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated to the addresses from 00400h to 007FFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.
Special function registers (SFR) are allocated to the addresses from 00000h to 002FFh. Peripheral function control registers are located here. Of the SFR, any space which has no functions allocated is reserved for future use and cannot be used by users.



NOTES:
1. The data flash ROM block A (1K bytes) and block B (1K bytes) are shown.

Type name	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F21154SP, R5F21154DSP, R5F21154DD, R5F21154DDD	16K bytes	0C000h	1K bytes	007FFh
R5F21153SP, R5F21153DSP, R5F21153DD, R5F21153DDD	12K bytes	0D000h	768 bytes	006FFh
R5F21152SP, R5F21152DSP, R5F21152DD, R5F21152DDD	8K bytes	0E000h	512 bytes	005FFh

Figure 3.1 Memory Map

4. Special Function Register (SFR)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor mode register 0	PM0	00h
0005h	Processor mode register 1	PM1	00h
0006h	System clock control register 0	CM0	01101000b
0007h	System clock control register 1	CM1	00100000b
0008h			
0009h	Address match interrupt enable register	AIER	XXXXXX00b
000Ah	Protect register	PRCR	00XXX000b
000Bh			
000Ch	Oscillation stop detection register	OCD	00000100b
000Dh	Watchdog timer reset register	WDTR	XXh
000Eh	Watchdog timer start register	WDTS	XXh
000Fh	Watchdog timer control register	WDC	000XXXXXb
0010h	Address match interrupt register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address match interrupt register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count source protect mode register	CSPR	00h
001Dh			
001Eh	INT0 input filter select register	INT0F	XXXXX000b
001Fh			
0020h	High-speed ring A control register 0	HRA0	00h
0021h	High-speed ring A control register 1	HRA1	TBD
0022h			
0023h			
0024h			
0025h			
0026h			
0027h			
0028h			
0029h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h			
0031h	Voltage detection A register 1(2)	VCA1	00001000b
0032h	Voltage detection A register 2(2)	VCA2	00h(3) 01000000b(4)
0033h			
0034h			
0035h			
0036h	Voltage watch 1 control register (2)	VW1C	00001000b(3) 01001001b(4)
0037h	Voltage watch 2 control register (2)	VW2C	00h
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

NOTES:

1. Blank columns are all reserved space. No access is allowed.
2. Software reset or the watchdog timer reset does not affect this register.
3. Owing to Reset input.
4. Owing to Power-on Reset or Hardware Reset 2.

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h			
0049h			
004Ah			
004Bh			
004Ch			
004Dh	Key input interrupt control register	KUPIC	XXXXX000b
004Eh	A-D conversion interrupt control register	ADIC	XXXXX000b
004Fh	SSUA interrupt control register	SSUAIC	XXXXX000b
0050h	Compare 1 interrupt control register	CMP1IC	XXXXX000b
0051h	UART0 transmit interrupt control register	S0TIC	XXXXX000b
0052h	UART0 receive interrupt control register	S0RIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer X interrupt control register	TXIC	XXXXX000b
0057h			
0058h	Timer Z interrupt control register	TZIC	XXXXX000b
0059h	INT1 interrupt control register	INT1IC	XXXXX000b
005Ah	INT3 interrupt control register	INT3IC	XXXXX000b
005Bh	Timer C interrupt control register	TCIC	XXXXX000b
005Ch	Compare 0 interrupt control register	CMP0IC	XXXXX000b
005Dh	INT0 interrupt control register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined
NOTES:
1. Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	After reset
0080h	Timer Z mode register	TZMR	00h
0081h			
0082h			
0083h			
0084h	Timer Z waveform output control register	PUM	00h
0085h	Prescaler Z	PREZ	FFh
0086h	Timer Z secondary	TZSC	FFh
0087h	Timer Z primary	TZPR	FFh
0088h			
0089h			
008Ah	Timer Z output control register	TZOC	00h
008Bh	Timer X mode register	TXMR	00h
008Ch	Prescaler X	PREX	FFh
008Dh	Timer X	TX	FFh
008Eh	Timer count source set register	TCSS	00h
008Fh			
0090h	Timer C	TC	00h
0091h			00h
0092h			
0093h			
0094h			
0095h			
0096h	External input enable register	INTEN	00h
0097h			
0098h	Key input enable register	KIEN	00h
0099h			
009Ah	Timer C control register 0	TCC0	00h
009Bh	Timer C control register 1	TCC1	00h
009Ch	Capture, compare 0 register	TM0	XXh
009Dh			XXh
009Eh	Compare 1 register	TM1	XXh
009Fh			XXh
00A0h	UART0 transmit/receive mode register	U0MR	00h
00A1h	UART0 bit rate register	U0BRG	XXh
00A2h	UART0 transmit buffer register	U0TB	XXh
00A3h			XXh
00A4h	UART0 transmit/receive control register 0	U0C0	00001000b
00A5h	UART0 transmit/receive control register 1	U0C1	00000010b
00A6h	UART0 receive buffer register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h	UART transmit/receive control register 2	UCON	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS control register H	SSCRH	00h
00B9h	SS control register L	SSCRL	7Dh
00BAh	SS mode register	SSMR	18h
00BBh	SS enable register	SSER	00h
00BCh	SS status register	SSSR	00h
00BDh	SS mode register 2	SSMR2	00h
00BEh	SS transmit data register	SSTDR	FFh
00BFh	SS receive data register	SSRDR	FFh

X: Undefined
NOTES:
1. Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	After reset
00C0h	A-D register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A-D control register 2	ADCON2	00h
00D5h			
00D6h	A-D control register 0	ADCON0	00000XXXb
00D7h	A-D control register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h			
00E1h	Port P1 register	P0	XXh
00E2h			
00E3h	Port P1 direction register	PD1	00h
00E4h			
00E5h	Port P3 register	P3	XXh
00E6h			
00E7h	Port P3 direction register	PD3	00h
00E8h	Port P4 register	P4	XXh
00E9h			
00EAh	Port P4 direction register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh	Pull-up control register 0	PUR0	00XX0000b
00FDh	Pull-up control register 1	PUR1	XXXXXX0Xb
00FEh	Port P1 drivability control register	DRR	00h
00FFh	Timer C output control register	TCOUT	00h

01B3h	Flash memory control register 4	FMR4	0100000Xb
01B4h			
01B5h	Flash memory control register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash memory control register 0	FMR0	XX000001b

0FFFFh	Optional function select register	OFS	(2)

X: Undefined

NOTES:

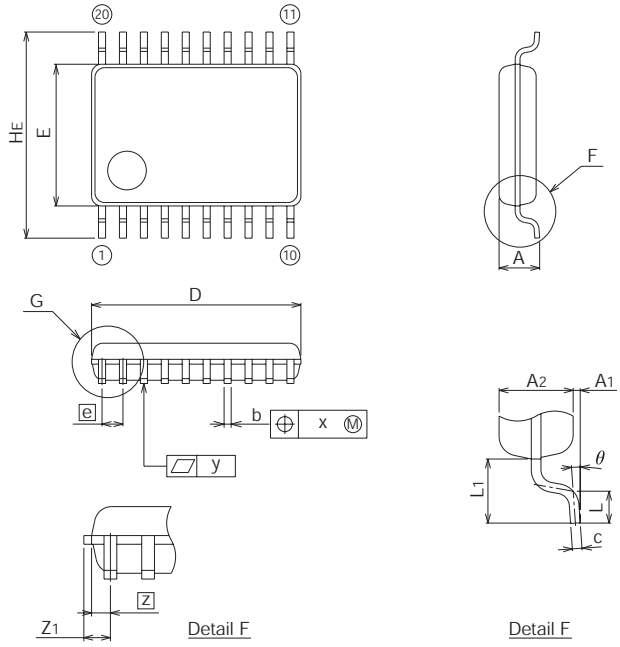
1. Blank columns are all reserved space. No access is allowed.
2. The OFS register cannot be changed by program. Use a flash programmer to write to it.

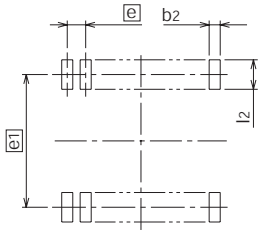
Package Dimensions

20P2F-A Recommended

Plastic 20pin 255mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP20-P-255-0.65	–	–	Cu Alloy





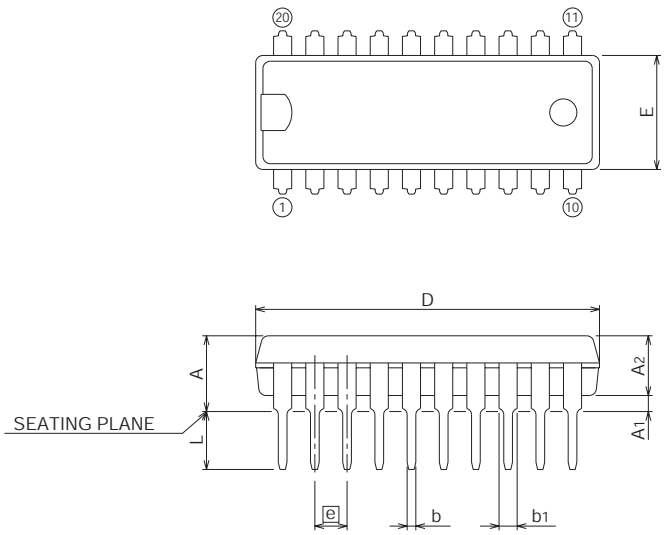
Recommended Mount Pad

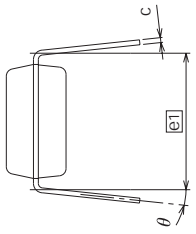
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.45
A1	0	0.1	0.2
A2	–	1.15	–
b	0.17	0.22	0.32
c	0.13	0.15	0.2
D	6.4	6.5	6.6
E	4.3	4.4	4.5
e	–	0.65	–
HE	6.2	6.4	6.6
L	0.3	0.5	0.7
L1	–	1.0	–
Z	–	0.325	–
Z1	–	–	0.475
x	–	–	0.13
y	–	–	0.1
θ	0	–	10
b2	–	0.35	–
e1	–	5.8	–
l2	1.0	–	–

20P4B Recommended

Plastic 20pin 300mil S DIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP20-P-300-1.78	–	1.0	Alloy 42/Cu Alloy





Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	4.5
A1	0.51	–	–
A2	–	3.3	–
b	0.38	0.48	0.58
b1	0.9	1.0	1.3
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	6.15	6.3	6.45
e	–	1.778	–
e1	–	7.62	–
L	3.0	–	–
θ	0	–	15

REVISION HISTORY	R8C/15 Group Short Sheet

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		Page	Summary
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Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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