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74LVTH162373

Low Voltage 16-Bit Transparent Latch with 3-STATE Outputs and 25Ω Series Resistors in the Outputs

General Description

The LVTH162373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the outputs are in a high impedance state.

The LVTH162373 is designed with equivalent 25Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The LVTH162373 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These latches are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH162373 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

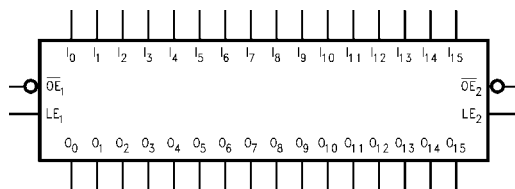
- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs include equivalent series resistance of 25Ω to make external termination resistors unnecessary and reduce overshoot and undershoot
- Functionally compatible with the 74 series 16373
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device model > 1000V

Ordering Code:

Order Number	Package Number	Package Description
74LVTH162373MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TUBES]
74LVTH162373MEX (Note 1)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74LVTH162373MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TUBES]
74LVTH162373MTX (Note 1)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

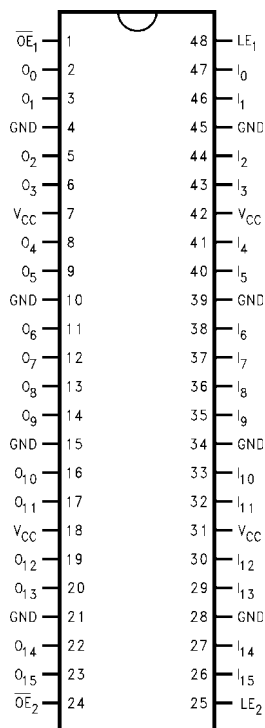
Note 1: Use this Order Number to receive devices in Tape and Reel.

Logic Symbol



74LVTH162373 Low Voltage 16-Bit Transparent Latch with 3-STATE Outputs and 25Ω Series Resistors in the Outputs

Connection Diagram



Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
LE_n	Latch Enable Input
I_0-I_{15}	Inputs
O_0-O_{15}	3-STATE Outputs

Truth Tables

Inputs			Outputs
LE_1	\overline{OE}_1	I_0-I_7	O_0-O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

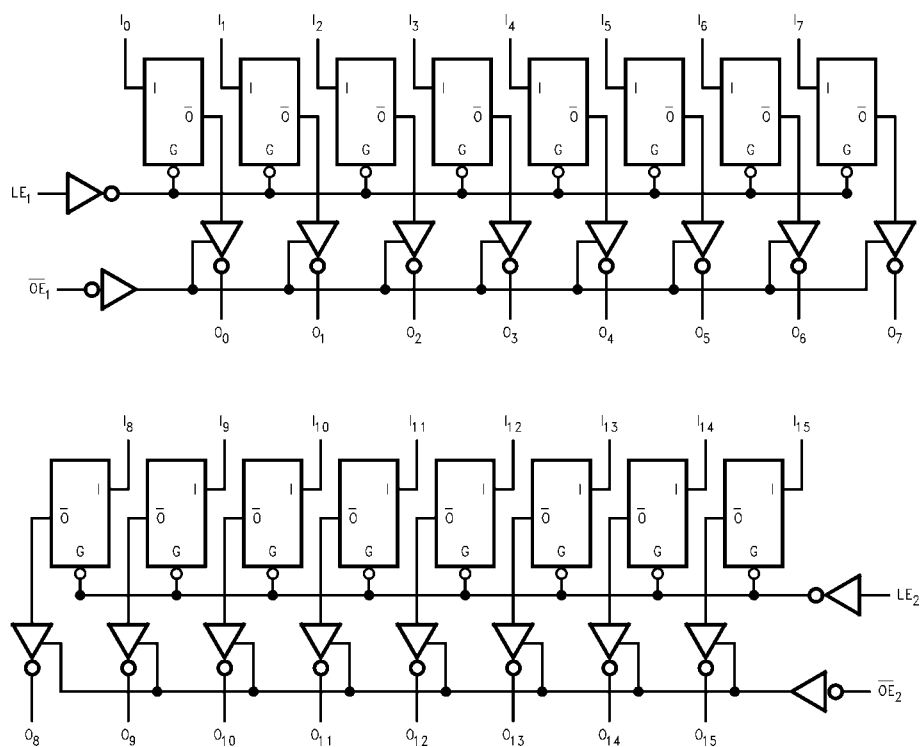
Inputs			Outputs
LE_2	\overline{OE}_2	I_8-I_{15}	O_8-O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = HIGH Impedance
 O_0 = Previous output prior to HIGH-to-LOW transition of LE

Functional Description

The LVTH162373 contains sixteen D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n . The 3-STATE standard outputs are controlled by the Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW, the standard outputs are in the 2-state mode. When \overline{OE}_n is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V _{CC}	Supply Voltage	−0.5 to +4.6		V
V _I	DC Input Voltage	−0.5 to +7.0		V
V _O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to +7.0	Output in HIGH or LOW State (Note 3)	
I _{IK}	DC Input Diode Current	−50	V _I < GND	mA
I _{OK}	DC Output Diode Current	−50	V _O < GND	mA
I _O	DC Output Current	64	V _O > V _{CC} Output at HIGH State	mA
		128	V _O > V _{CC} Output at LOW State	
I _{CC}	DC Supply Current per Supply Pin	±64		mA
I _{GND}	DC Ground Current per Ground Pin	±128		mA
T _{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V _{CC}	Supply Voltage	2.7	3.6	V
V _I	Input Voltage	0	5.5	V
I _{OH}	HIGH Level Output Current		−12	mA
I _{OL}	LOW Level Output Current		12	mA
T _A	Free-Air Operating Temperature	−40	85	°C
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V	0	10	ns/V

Note 2: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 3: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = −40°C to +85°C		Units	Conditions
			Min	Max		
V _{IK}	Input Clamp Diode Voltage	2.7		−1.2	V	I _I = −18 mA
V _{IH}	Input HIGH Voltage	2.7–3.6	2.0		V	V _O ≤ 0.1V or
V _{IL}	Input LOW Voltage	2.7–3.6		0.8	V	V _O ≥ V _{CC} − 0.1V
V _{OH}	Output HIGH Voltage	2.7–3.6	V _{CC} − 0.2		V	I _{OH} = −100 μA
		3.0	2.0			I _{OH} = −12mA
V _{OL}	Output LOW Voltage	2.7		0.2	V	I _{OL} = 100 μA
		3.0		0.8		I _{OL} = 12 mA
I _{I(HOLD)}	Bushold Input Minimum Drive	3.0	75		μA	V _I = 0.8V
			−75			V _I = 2.0V
I _{I(OD)}	Bushold Input Over-Drive Current to Change State	3.0	500		μA	(Note 4)
			−500			(Note 5)
I _I	Input Current	3.6		10	μA	V _I = 5.5V
		Control Pins	3.6	±1		V _I = 0V or V _{CC}
		Data Pins		−5		V _I = 0V
				1		V _I = V _{CC}
I _{OFF}	Power Off Leakage Current	0		±100	μA	0V ≤ V _I or V _O ≤ 5.5V
I _{PU/PD}	Power Up/Down 3-STATE Output Current	0–1.5V		±100	μA	V _O = 0.5V to 3.0V V _I = GND or V _{CC}
I _{OZL}	3-STATE Output Leakage Current	3.6		−5	μA	V _O = 0.5V
I _{OZH}	3-STATE Output Leakage Current	3.6		5	μA	V _O = 3.0V
I _{OZH+}	3-STATE Output Leakage Current	3.6		10	μA	V _{CC} < V _O ≤ 5.5V
I _{CCH}	Power Supply Current	3.6		0.19	mA	Outputs HIGH
I _{CCL}	Power Supply Current	3.6		5	mA	Outputs LOW
I _{CCZ}	Power Supply Current	3.6		0.19	mA	Outputs Disabled

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C		Units	Conditions
			Min	Max		
I _{CCZ} ⁺	Power Supply Current	3.6		0.19	mA	V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled
ΔI _{CC}	Increase in Power Supply Current (Note 6)	3.6		0.2	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND

Note 4: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 6: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 7)

Symbol	Parameter	V _{CC} (V)	T _A = 25°C			Units	Conditions C _L = 50 pF, R _L = 500Ω
			Min	Typ	Max		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3		0.8		V	(Note 8)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3		-0.8		V	(Note 8)

Note 7: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 8: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

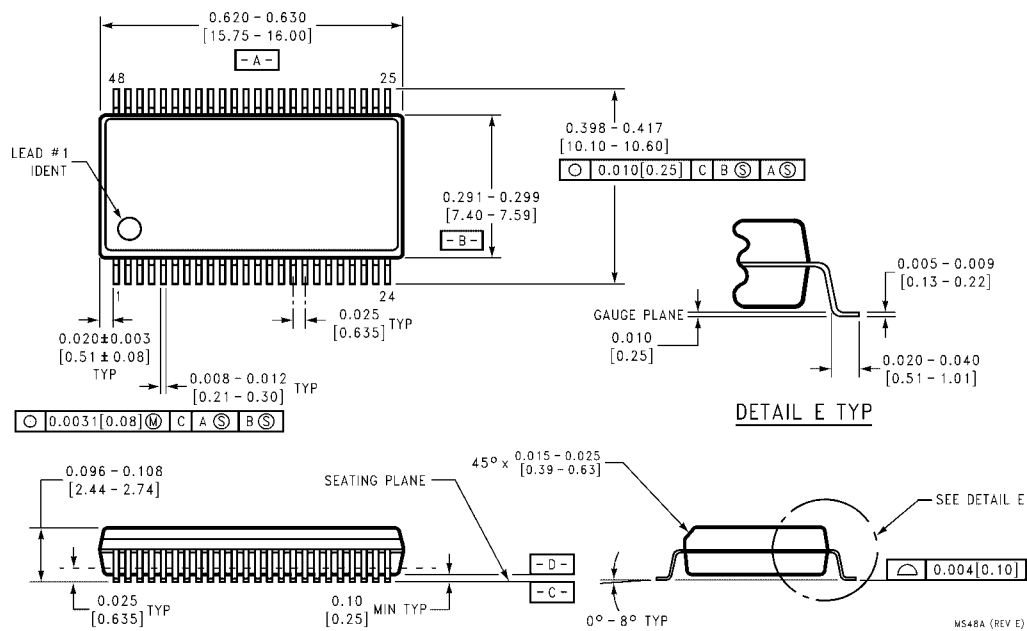
Symbol	Parameter	T _A = -40°C to +85°C, C _L = 50pF, R _L = 500Ω				Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		
		Min	Max	Min	Max	
t _{PHL}	Propagation Delay	1.3	4.8	1.3	5.3	ns
t _{PLH}	D _n to O _n	1.4	4.8	1.4	5.1	
t _{PHL}	Propagation Delay	1.7	5.0	1.7	5.1	ns
t _{PLH}	LE to O _n	1.4	5.1	1.4	5.8	
t _{PZL}	Output Enable Time	1.6	5.0	1.6	6.0	ns
t _{PZH}		1.0	5.4	1.0	6.6	
t _{PLZ}	Output Disable Time	1.6	5.1	1.6	5.0	ns
t _{PHZ}		1.8	5.4	1.8	5.7	
t _S	Setup Time, D _n to LE	1.0		0.8		ns
t _H	Hold Time, D _n to LE	1.0		1.1		ns
t _W	LE Pulse Width	3.0		3.0		ns
t _{OSHL}	Output to Output Skew (Note 9)		1.0		1.0	ns
t _{OSLH}			1.0		1.0	

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 10)

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = OPEN, V _I = 0V or V _{CC}	4	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.0V, V _O = 0V or V _{CC}	8	pF

Note 10: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A**

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