

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT540**

Octal buffer/line driver; 3-state;  
inverting

Product specification  
File under Integrated Circuits, IC06

December 1990

# Octal buffer/line driver; 3-state; inverting

## 74HC/HCT540

### FEATURES

- Inverting outputs
- Output capability: bus driver
- $I_{CC}$  category: MSI

The 74HC/HCT540 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs  $\overline{OE}_1$  and  $\overline{OE}_2$ .

A HIGH on  $\overline{OE}_n$  causes the outputs to assume a high impedance OFF-state.

The "540" is identical to the "541" but has inverting outputs.

### GENERAL DESCRIPTION

The 74HC/HCT540 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

| SYMBOL            | PARAMETER                                   | CONDITIONS                                   | TYPICAL |     | UNIT |
|-------------------|---------------------------------------------|----------------------------------------------|---------|-----|------|
|                   |                                             |                                              | HC      | HCT |      |
| $t_{PHL}/t_{PLH}$ | propagation delay $A_n$ to $\overline{Y}_n$ | $C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$ | 9       | 11  | ns   |
| $C_I$             | input capacitance                           |                                              | 3.5     | 3.5 | pF   |
| $C_{PD}$          | power dissipation capacitance per buffer    | notes 1 and 2                                | 39      | 44  | pF   |

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

### ORDERING INFORMATION

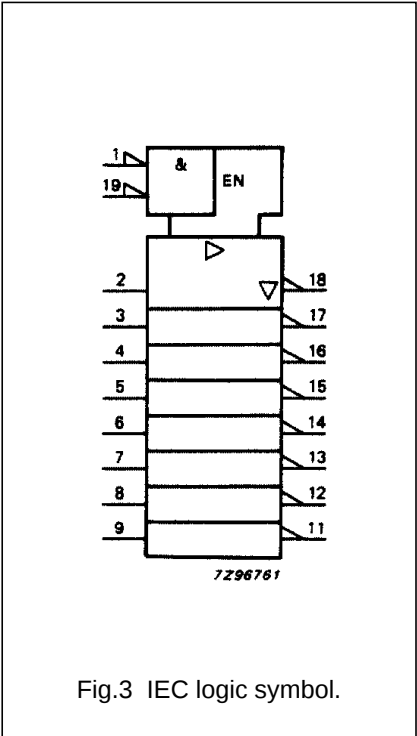
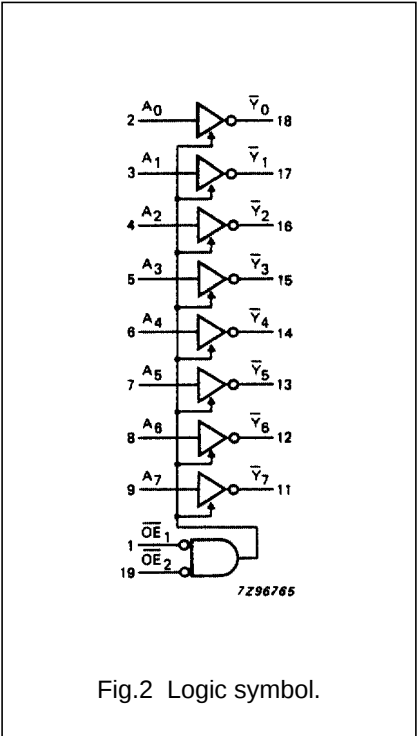
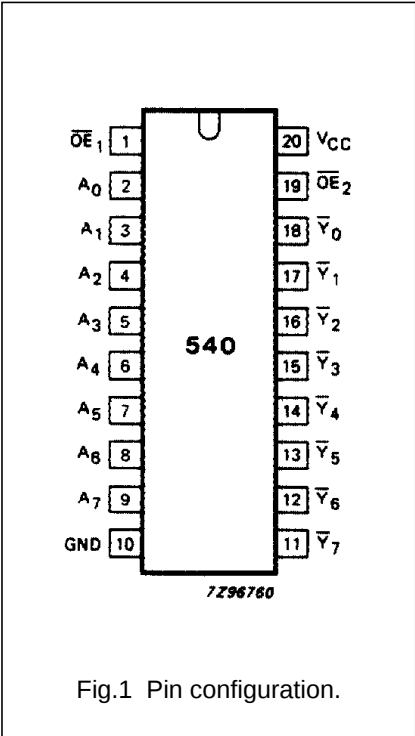
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Octal buffer/line driver; 3-state; inverting

74HC/HCT540

PIN DESCRIPTION

| PIN NO.                        | SYMBOL                               | NAME AND FUNCTION                |
|--------------------------------|--------------------------------------|----------------------------------|
| 1, 19                          | $\overline{OE}_1, \overline{OE}_2$   | output enable input (active LOW) |
| 2, 3, 4, 5, 6, 7, 8, 9         | $A_0$ to $A_7$                       | data inputs                      |
| 10                             | GND                                  | ground (0 V)                     |
| 18, 17, 16, 15, 14, 13, 12, 11 | $\overline{Y}_0$ to $\overline{Y}_7$ | bus outputs                      |
| 20                             | $V_{CC}$                             | positive supply voltage          |



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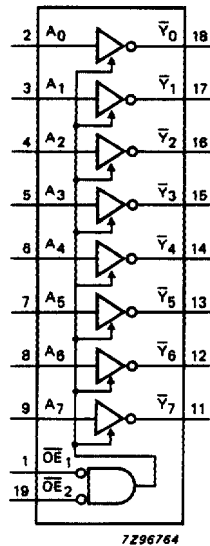


Fig.4 Functional diagram.

FUNCTION TABLE

| INPUTS            |                   |       | OUTPUT           |
|-------------------|-------------------|-------|------------------|
| $\overline{OE}_1$ | $\overline{OE}_2$ | $A_n$ | $\overline{Y}_n$ |
| L                 | L                 | L     | H                |
| L                 | L                 | H     | L                |
| X                 | H                 | X     | Z                |
| H                 | X                 | X     | Z                |

- Notes
- H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

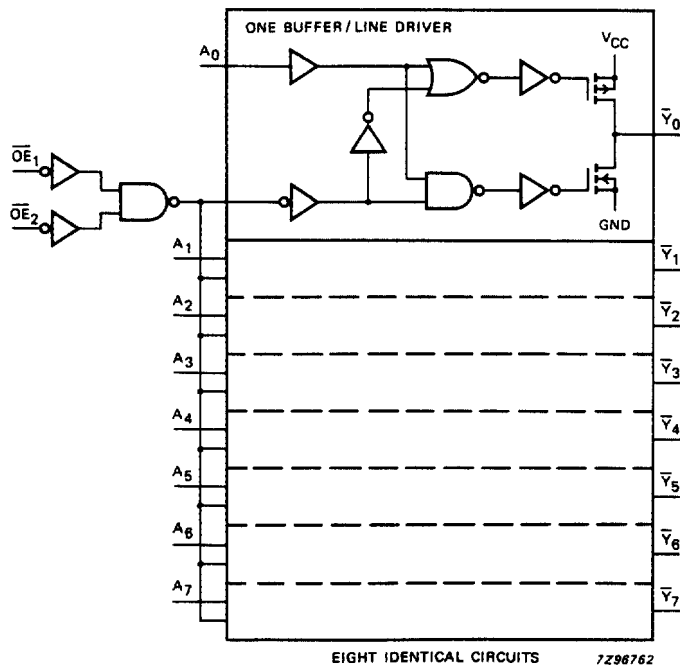


Fig.5 Logic diagram.

## Octal buffer/line driver; 3-state; inverting

## 74HC/HCT540

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                              | T <sub>amb</sub> (°C) |                |                 |            |                 |             |                 | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|--------------------------------------------------------|-----------------------|----------------|-----------------|------------|-----------------|-------------|-----------------|------|------------------------|-----------|
|                                     |                                                        | 74HC                  |                |                 |            |                 |             |                 |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                        | +25                   |                |                 | −40 to +85 |                 | −40 to +125 |                 |      |                        |           |
|                                     |                                                        | min.                  | typ.           | max.            | min.       | max.            | min.        | max.            |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>A <sub>n</sub> to Y <sub>n</sub>  |                       | 30<br>11<br>9  | 100<br>20<br>17 |            | 125<br>25<br>21 |             | 150<br>30<br>26 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output<br>enable time<br>OE to Y <sub>n</sub>  |                       | 52<br>19<br>15 | 160<br>32<br>27 |            | 200<br>40<br>34 |             | 240<br>48<br>41 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output<br>disable time<br>OE to Y <sub>n</sub> |                       | 61<br>22<br>18 | 160<br>32<br>27 |            | 200<br>40<br>34 |             | 240<br>48<br>41 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                 |                       | 14<br>5<br>4   | 60<br>12<br>10  |            | 75<br>15<br>13  |             | 90<br>18<br>15  | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |

## Octal buffer/line driver; 3-state; inverting

## 74HC/HCT540

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT             | UNIT LOAD COEFFICIENT |
|-------------------|-----------------------|
| $\overline{OE}_1$ | 1.50                  |
| $\overline{OE}_2$ | 1.00                  |
| $A_n$             | 1.40                  |

**AC CHARACTERISTICS FOR 74HCT**

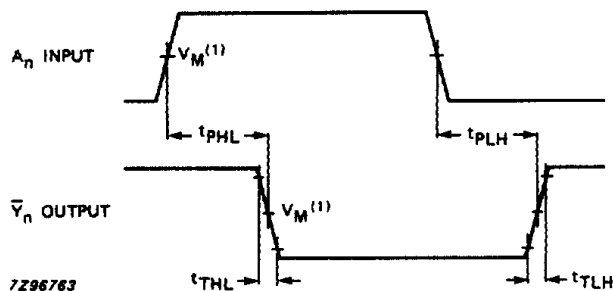
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

| SYMBOL                              | PARAMETER                                                             | T <sub>amb</sub> (°C) |      |      |            |      |             |      | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|-----------------------------------------------------------------------|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------|
|                                     |                                                                       | 74HCT                 |      |      |            |      |             |      |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                                       | +25                   |      |      | −40 to +85 |      | −40 to +125 |      |      |                        |           |
|                                     |                                                                       | min.                  | typ. | max. | min.       | max. | min.        | max. |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>A <sub>n</sub> to $\overline{Y}_n$               |                       | 13   | 24   |            | 30   |             | 36   | ns   | 4.5                    | Fig.6     |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state<br>output enable time<br>$\overline{OE}$ to $\overline{Y}_n$  |                       | 22   | 35   |            | 44   |             | 53   | ns   | 4.5                    | Fig.7     |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output<br>disable time<br>$\overline{OE}$ to $\overline{Y}_n$ |                       | 23   | 35   |            | 44   |             | 53   | ns   | 4.5                    | Fig.7     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                                |                       | 5    | 12   |            | 15   |             | 18   | ns   | 4.5                    | Fig.6     |

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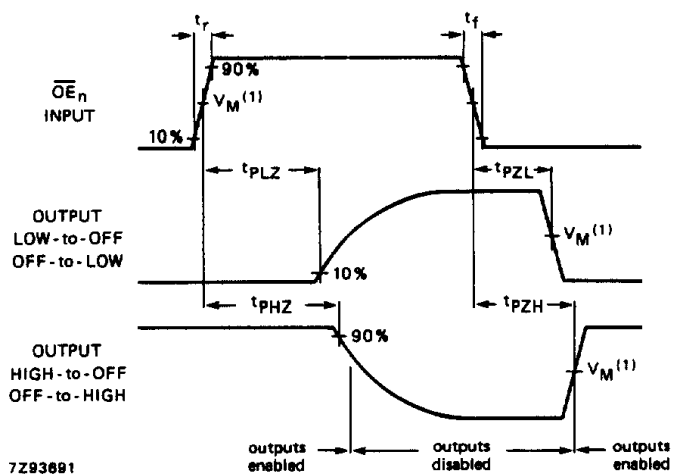
74HC/HCT540

## AC WAVEFORMS



- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.6 Waveforms showing the input ( $A_n$ ) to output ( $\bar{Y}_n$ ) propagation delays and the output transition times.



- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.7 Waveforms showing the 3-state enable and disable times.

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".