

BUK6E2R3-40C

N-channel TrenchMOS intermediate level FET

Rev. 1 — 18 August 2010

Product data sheet

1. Product profile

1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Suitable for intermediate level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V Automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	306	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 11 ; see Figure 12	-	2	2.3	mΩ



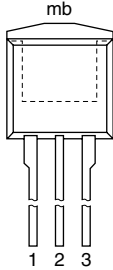
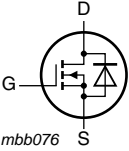
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped	-	-	1.02	J
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; see Figure 13 ; see Figure 14	-	72	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	Drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT226 (I2PAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6E2R3-40C	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	40	V
V_{GS}	gate-source voltage	DC [1]	-16	16	V
		Pulsed [2]	-20	20	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 [3]	-	120	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 [3]	-	120	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}; t_p \leq 10\text{ }\mu\text{s};$ pulsed; see Figure 3	-	1006	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	306	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$ [3]	-	120	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s};$ pulsed; $T_{mb} = 25\text{ °C}$	-	1006	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}; V_{sup} \leq 40\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped	-	1.02	J
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	[4][5][6]	-	-	J

[1] -16V accumulated duration not to exceed 168 hrs

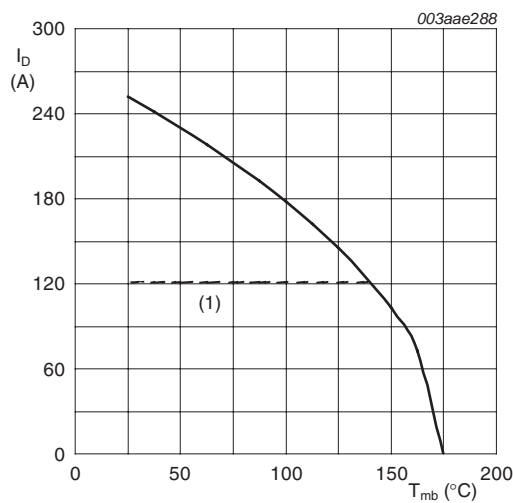
[2] Accumulated pulse duration not to exceed 5mins.

[3] Continuous current is limited by package.

[4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

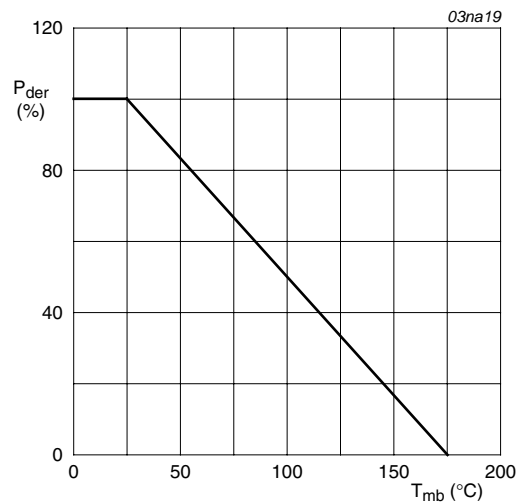
[5] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[6] Refer to application note AN10273 for further information.



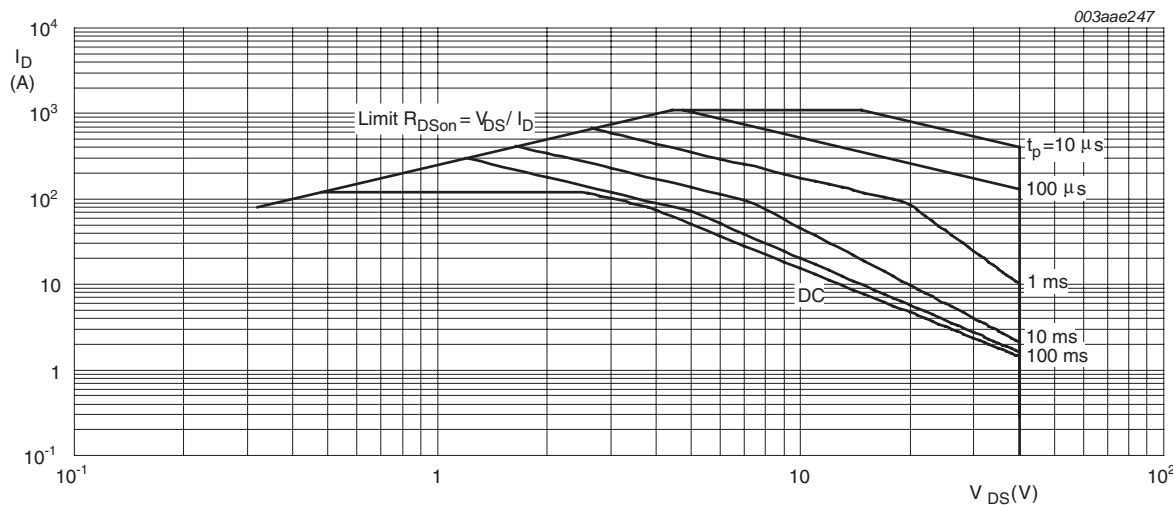
$V_{GS} \geq 10V$
(1) Capped at 120 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



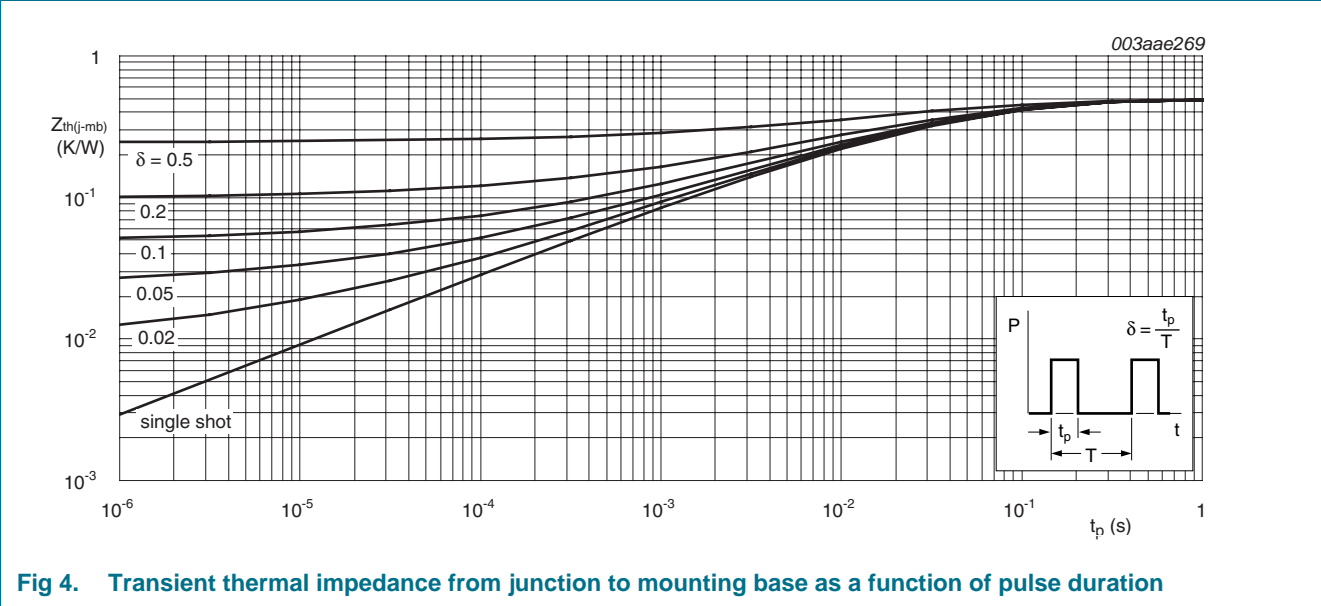
$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.49	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	60	-	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	40	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	36	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 9 ; see Figure 10	1.8	2.3	2.8	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 10	-	-	3.3	V
		I _D = 2.5 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 10	0.8	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C	-	0.02	1	μA
I _{GSS}	gate leakage current	V _{DS} = 0 V; V _{GS} = 20 V; T _j = 25 °C	-	2	100	nA
		V _{DS} = 0 V; V _{GS} = -20 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 11 ; see Figure 12	-	2	2.3	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; see Figure 11 ; see Figure 12	-	2.5	3.1	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; see Figure 11 ; see Figure 12	-	2.8	3.6	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; see Figure 11	-	-	5	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; see Figure 13 ; see Figure 14	-	260	-	nC
		I _D = 25 A; V _{DS} = 32 V; V _{GS} = 5 V; see Figure 13 ; see Figure 14	-	147	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; see Figure 13 ; see Figure 14	-	38	-	nC
Q _{GD}	gate-drain charge		-	72	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; see Figure 16	-	11.3	15.1	nF
C _{oss}	output capacitance		-	1447	1750	pF
C _{rss}	reverse transfer capacitance		-	1014	1390	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 10 V; R _{G(ext)} = 10 Ω	-	60	-	ns
t _r	rise time		-	140	-	ns
t _{d(off)}	turn-off delay time		-	234	-	ns
t _f	fall time		-	416	-	ns
L _D	internal drain inductance	from drain lead 6 mm from package to centre of die; T _j = 25 °C	-	4.5	-	nH
L _S	internal source inductance	from source lead to source bond pad; T _i = 25 °C	-	7.5	-	nH

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 15	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	63	-	ns
Q_r	recovered charge	$V_{DS} = 25\text{ V}$	-	127	-	nC

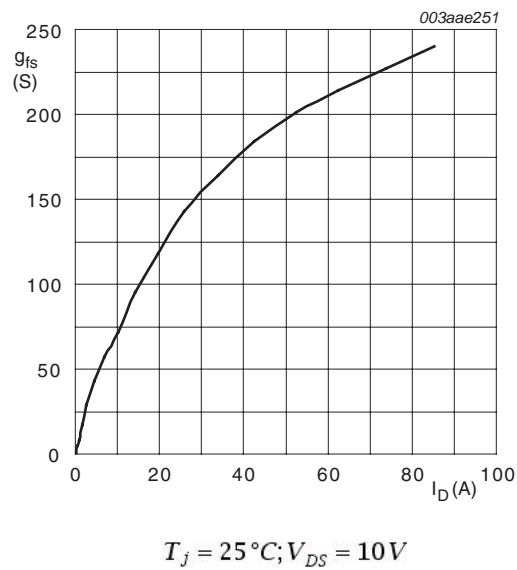


Fig 5. Forward transconductance as a function of drain current; typical values

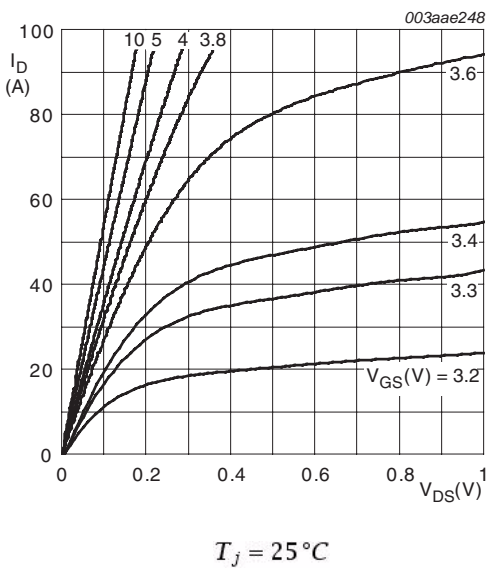


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

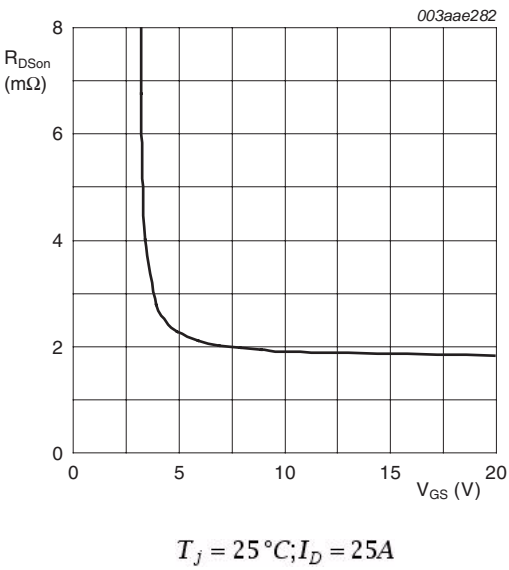


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

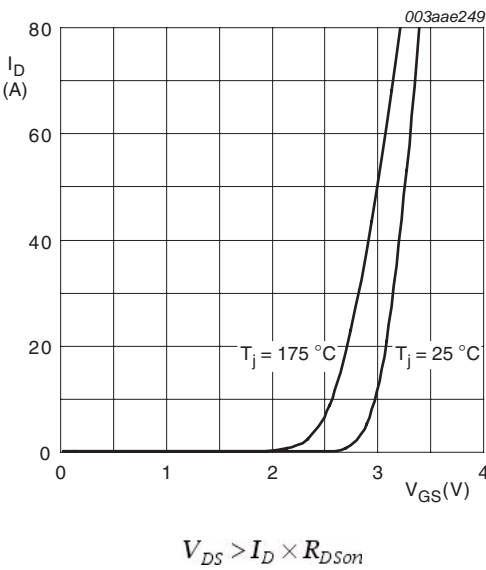
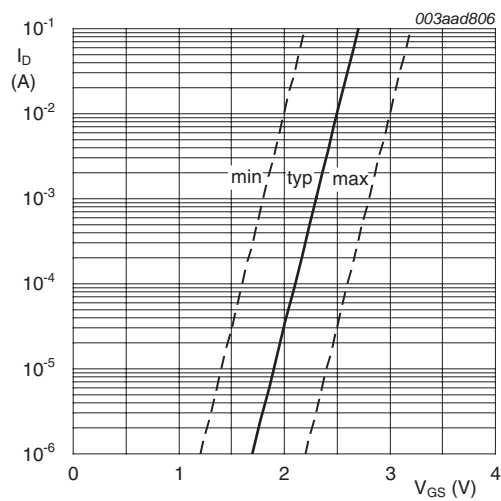
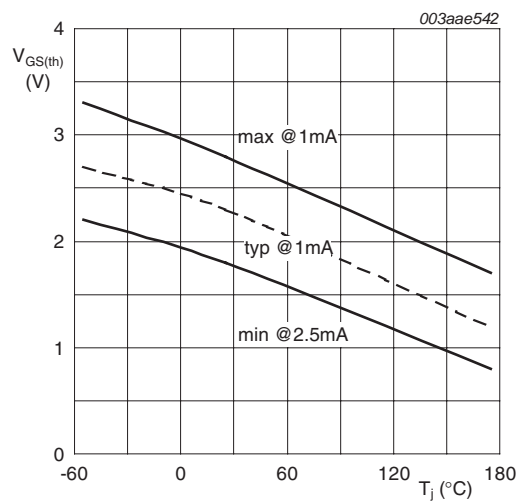


Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values



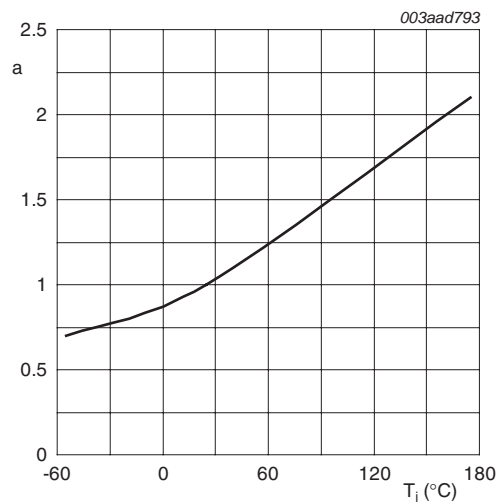
$T_j = 25^{\circ}\text{C}; V_{DS} = 5\text{V}$

Fig 9. Sub-threshold drain current as a function of gate-source voltage



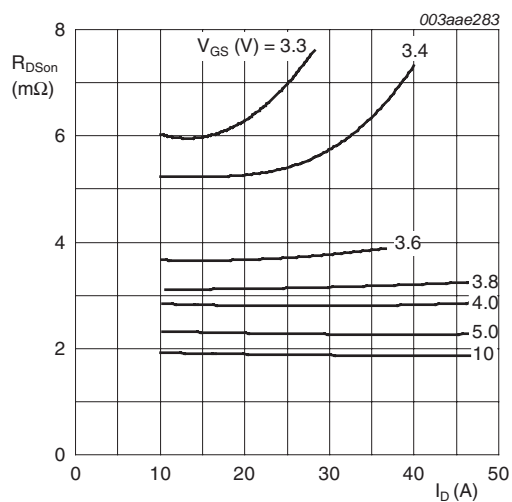
$I_D = 1\text{mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^{\circ}\text{C}$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values

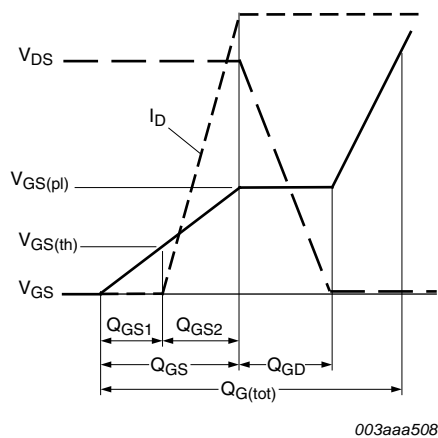
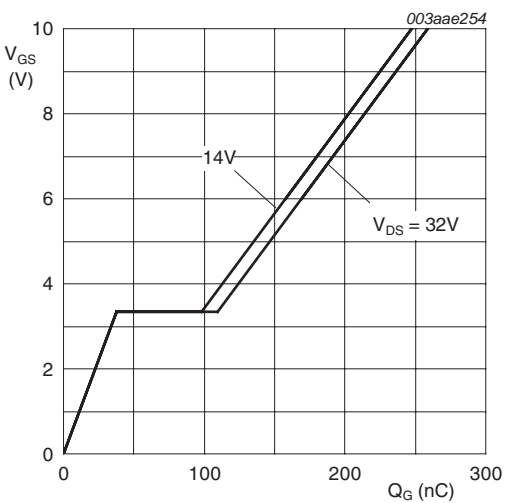
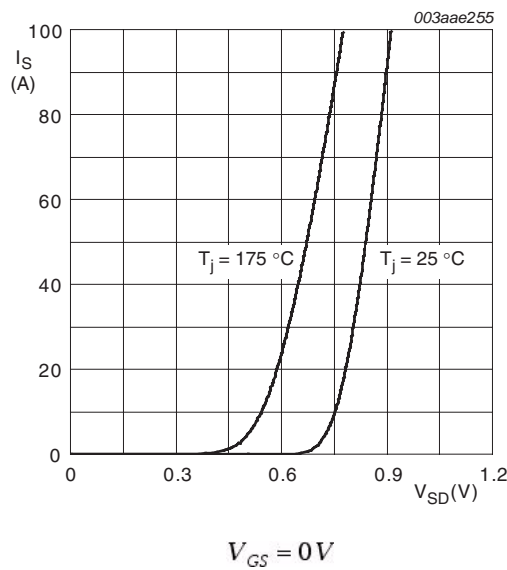


Fig 13. Gate charge waveform definitions



$T_j = 25\text{ }^{\circ}\text{C}; I_D = 25A$

Fig 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V$

Fig 15. Source current as a function of source-drain voltage; typical values

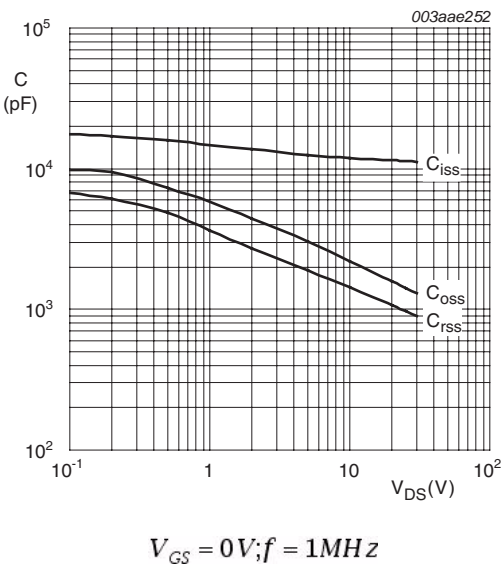


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended package (I2PAK); low-profile 3-lead TO-262

SOT226

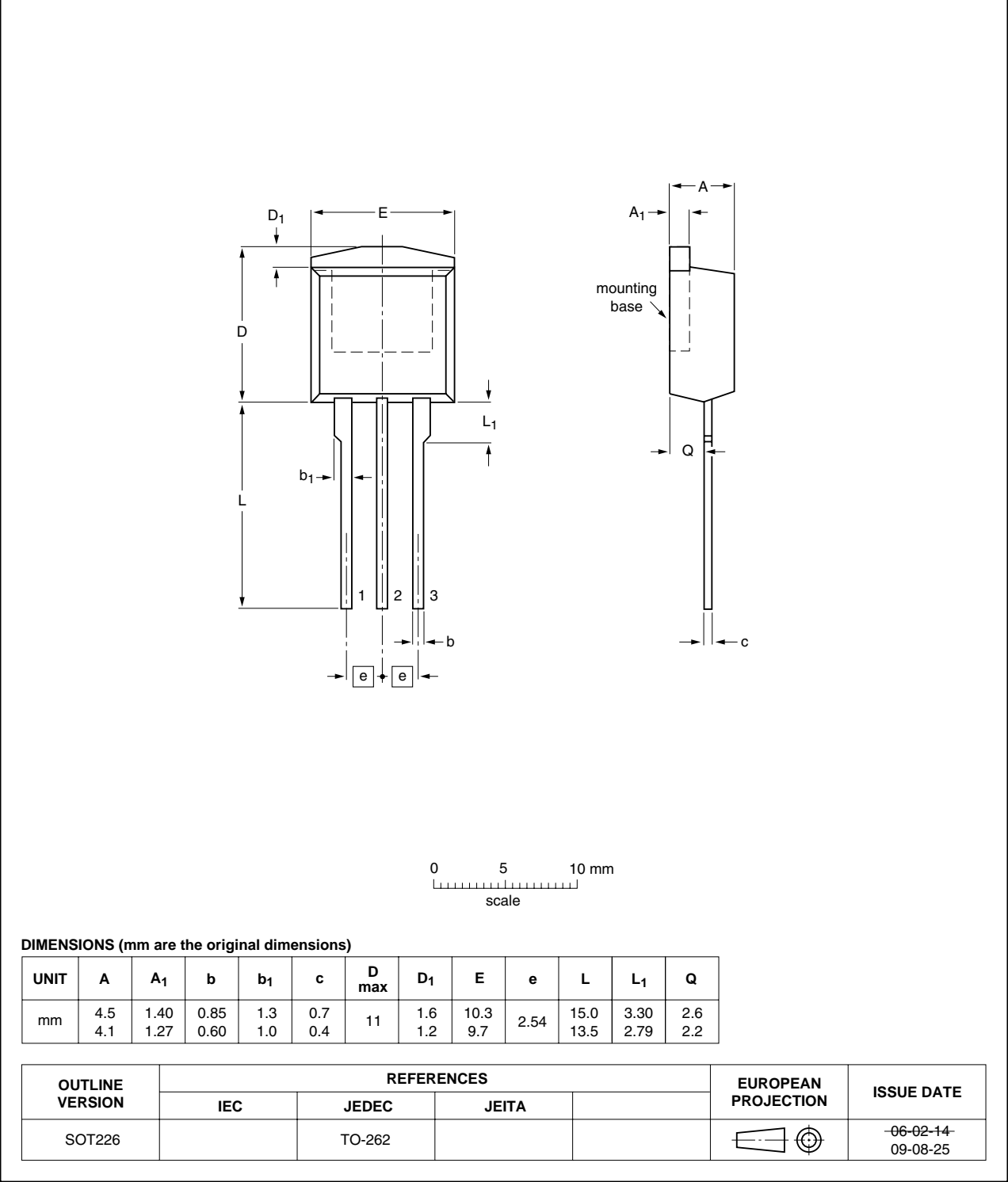


Fig 17. Package outline SOT226 (I2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK6E2R3-40C v.1	20100818	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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