LM5110 Dual 5A Compound Gate Driver with Negative Output Voltage Capability

Check for Samples: LM5110

FEATURES

- **Independently Drives Two N-Channel MOSFETs**
- **Compound CMOS and Bipolar Outputs Reduce Output Current Variation**
- **5A sink/3A Source Current Capability**
- **Two Channels can be Connected in Parallel to Double the Drive Current**
- **Independent Inputs (TTL Compatible)**
- **Fast Propagation Times (25 ns Typical)**
- **Fast Rise and Fall Times (14 ns/12 ns Rise/Fall with 2 nF Load)**
- **Dedicated Input Ground Pin (IN_REF) for Split Supply or Single Supply Operation**
- **Outputs Swing from V_{CC} to V_{EE} which can be Negative Relative to Input Ground**
- **Available in Dual Non-inverting, Dual Inverting and Combination Configurations**
- **Shutdown Input Provides Low Power Mode**
- **Supply Rail Under-voltage Lockout Protection**
- **Pin-out Compatible with Industry Standard Gate Drivers**

TYPICAL APPLICATIONS

- **Synchronous Rectifier Gate Drivers**
- **Switch-mode Power Supply Gate Driver**
- **Solenoid and Motor Drivers**
- **Power Level Shifter**

PACKAGE

- **SOIC-8**
- **WSON-10 (4 mm x 4 mm)**

DESCRIPTION

The LM5110 Dual Gate Driver replaces industry standard gate drivers with improved peak output current and efficiency. Each “compound” output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 5A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Separate input and output ground pins provide Negative Drive Capability allowing the user to drive MOSFET gates with positive and negative VGS voltages. The gate driver control inputs are referenced to a dedicated input ground (IN_REF). The gate driver outputs swing from V_{CC} to the output ground V_{EE} which can be negative with respect to IN_REF. The ability to hold MOSFET gates off with a negative VGS voltage reduces losses when driving low threshold voltage MOSFETs often used as synchronous rectifiers. When driving with conventional positive only gate voltage, the IN_REF and V_{EE} pins are connected together and referenced to a common ground. Under-voltage lockout protection and a shutdown input pin are also provided. The drivers can be operated in parallel with inputs and outputs connected to double the drive current capability. This device is available in the SOIC-8 and the thermally-enhanced WSON-10 packages.

Pin Configurations

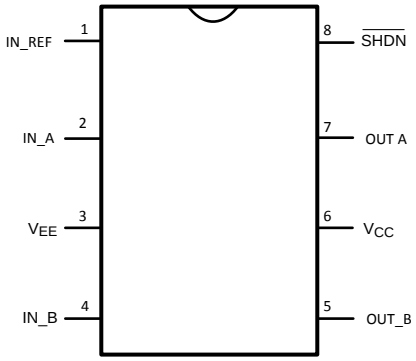


Figure 1. SOIC-8

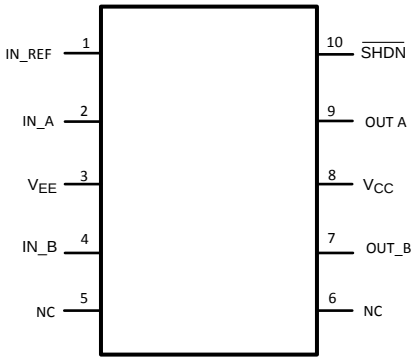


Figure 2. WSON-10
NC - NOT CONNECTED

Block Diagram

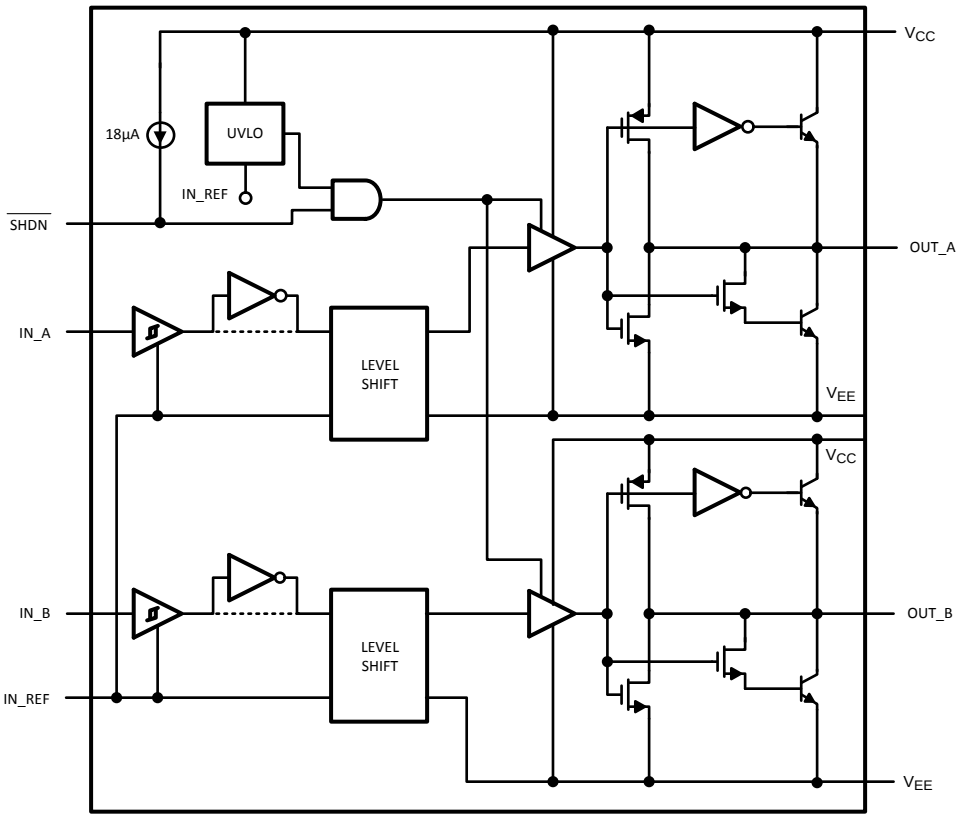


Figure 3. Block Diagram of LM5110

Typical Application

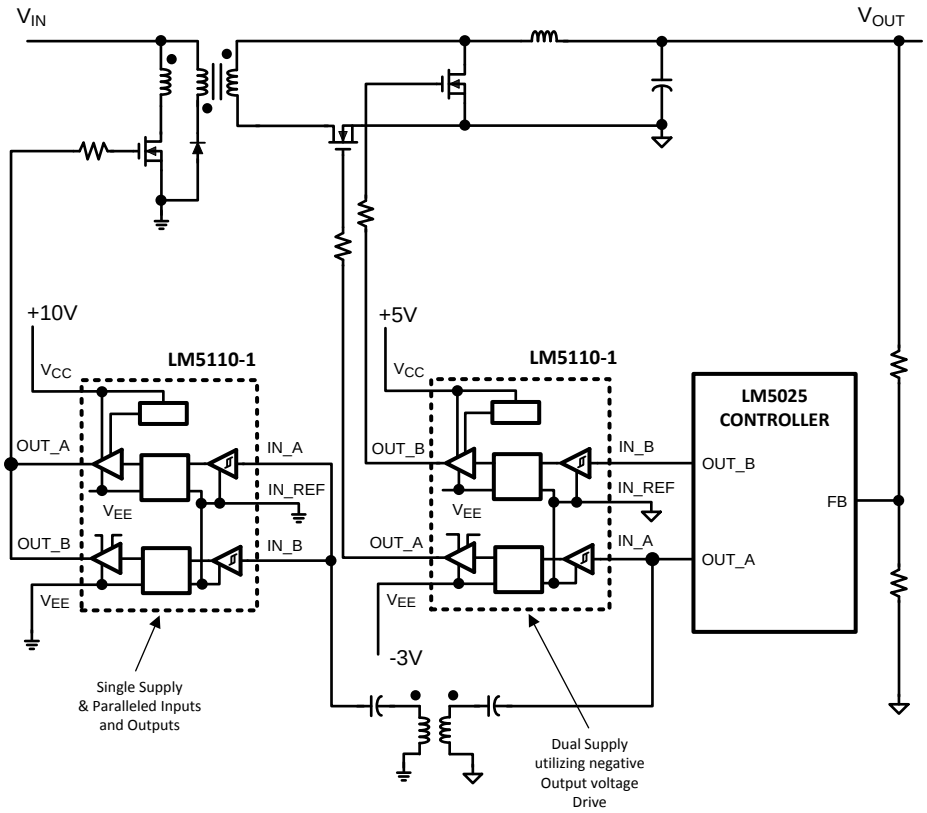


Figure 4. Simplified Power Converter Using Synchronous Rectifiers with Negative Off Gate Voltage

PIN DESCRIPTION

Pin Description		Name	Description	Application Information
SOIC-8	WSON-10			
1	1	IN_REF	Ground reference for control inputs	Connect to V_{EE} for standard positive only output voltage swing. Connect to system logic ground reference for positive and negative output voltage swing.
2	2	IN_A	'A' side control input	TTL compatible thresholds.
3	3	V_{EE}	Power ground of the driver outputs	Connect to either power ground or a negative gate drive supply.
4	4	IN_B	'B' side control input	TTL compatible thresholds.
5	7	OUT_B	Output for the 'B' side driver.	Capable of sourcing 3A and sinking 5A. Voltage swing of this output is from V_{CC} to V_{EE}.
6	8	V_{CC}	Positive supply	Locally decouple to V_{EE} and IN_REF.
7	9	OUT_A.	Output for the 'A' side driver.	Capable of sourcing 3A and sinking 5A. Voltage swing of this output is from V_{CC} to V_{EE} .
8	10	nSHDN	Shutdown input pin	Pull below 1.5V to activate low power shutdown mode.

Configuration Table

Part Number	"A" Output Configuration	"B" Output Configuration	Package
LM5110-1M	Non-Inverting	Non-Inverting	SOIC- 8
LM5110-2M	Inverting	Inverting	SOIC- 8
LM5110-3M	Inverting	Non-Inverting	SOIC- 8
LM5110-1SD	Non-Inverting	Non-Inverting	WSON-10
LM5110-2SD	Inverting	Inverting	WSON-10
LM5110-3SD	Inverting	Non-Inverting	WSON-10

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

V_{CC} to V_{EE}	−0.3V to 15V
V_{CC} to IN_REF	−0.3V to 15V
IN to IN_REF, nSHDN to IN_REF	−0.3V to 15V
IN_REF to V_{EE}	−0.3V to 5V
Storage Temperature Range, T_{STG}	−55°C to +150°C
Maximum Junction Temperature, T_J(max)	+150°C
Operating Junction Temperature	+125°C
ESD Rating	2kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Electrical Characteristics

T_J = −40°C to +125°C, V_{CC} = 12V, V_{EE} = IN_REF = 0V, nSHDN = V_{CC}, No Load on OUT_A or OUT_B, unless otherwise specified.

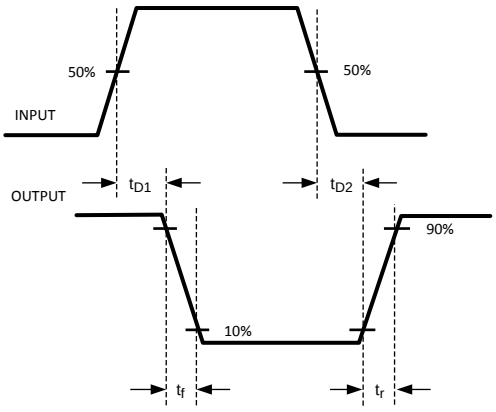
Symbol	Parameter	Conditions	Min	Typ	Max	Units
	V_{CC} Operating Range	V_{CC}−IN_REF and V_{CC}−V_{EE}	3.5		14	V
V_{CCR}	V_{CC} Under Voltage Lockout (rising)	V_{CC}−IN_REF	2.3	2.9	3.5	V
V_{CCH}	V_{CC} Under Voltage Lockout Hysteresis			230		mV
I_{CC}	V_{CC} Supply Current (I_{CC})	IN_A = IN_B = 0V (5110-1)		1	2	mA
		IN_A = IN_B = V_{CC} (5110-2)		1	2	
		IN_A = V_{CC}, IN_B = 0V (5110-3)		1	2	
I_{CCSD}	V_{CC} Shutdown Current (I_{CC})	nSHDN = 0V		18	25	µA
CONTROL INPUTS						
V_{IH}	Logic High			1.75	2.2	V
V_{IL}	Logic Low		0.8	1.35		V
HYS	Input Hysteresis			400		mV
I_{IL}	Input Current Low	IN_A=IN_B=V_{CC} (5110-1-2-3)	−1	0.1	1	µA
I_{IH}	Input Current High	IN_A=IN_B=V_{CC} (5110-1)	10	18	25	
		IN_A=IN_B=V_{CC} (5110-2)	−1	0.1	1	
		IN_A=V_{CC} (5110-3)	-1	0.1	1	
		IN_B=V_{CC} (5110-3)	10	18	25	
SHUTDOWN INPUT						
ISD	Pull-up Current	nSHDN = 0 V		−18	−25	µA

Electrical Characteristics (continued)

T_J = −40°C to +125°C, V_{CC} = 12V, V_{EE} = IN_REF = 0V, nSHDN = V_{CC}, No Load on OUT_A or OUT_B, unless otherwise specified.

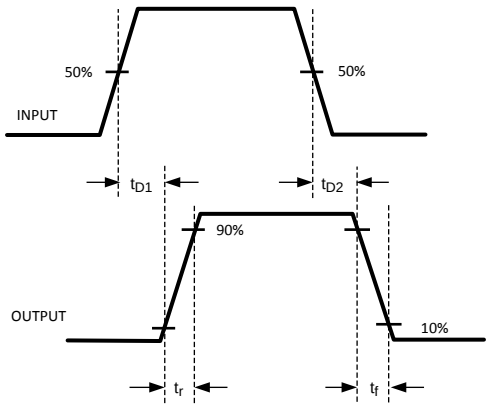
Symbol	Parameter	Conditions	Min	Typ	Max	Units
VSDR	Shutdown Threshold	nSHDN rising	0.8	1.5	2.2	V
VSDH	Shutdown Hysteresis			165		mV
OUTPUT DRIVERS						
R_{OH}	Output Resistance High	I_{OUT} = −10 mA		30	50	Ω
R_{OL}	Output Resistance Low	I_{OUT} = + 10 mA		1.4	2.5	Ω
I_{Source}	Peak Source Current	OUTA/OUTB = V_{CC}/2, 200 ns Pulsed Current		3		A
I_{Sink}	Peak Sink Current	OUTA/OUTB = V_{CC}/2, 200 ns Pulsed Current		5		A
SWITCHING CHARACTERISTICS						
td1	Propagation Delay Time Low to High, IN rising (IN to OUT)	C_{LOAD} = 2 nF, see Figure 6		25	40	ns
td2	Propagation Delay Time High to Low, IN falling (IN to OUT)	C_{LOAD} = 2 nF, see Figure 6		25	40	ns
t_r	Rise Time	C_{LOAD} = 2.0 nF, see Figure 6		14	25	ns
t_f	Fall Time	C_{LOAD} = 2 nF, see Figure 6		12	25	ns
LATCHUP PROTECTION						
	AEC - Q100, Method 004	T_J = 150°C		500		mA

Timing Waveforms



(a)

Figure 5. Inverting Timing Waveforms



(b)

Figure 6. Non-Inverting Timing Waveforms

Typical Performance Characteristics

Supply Current vs Frequency

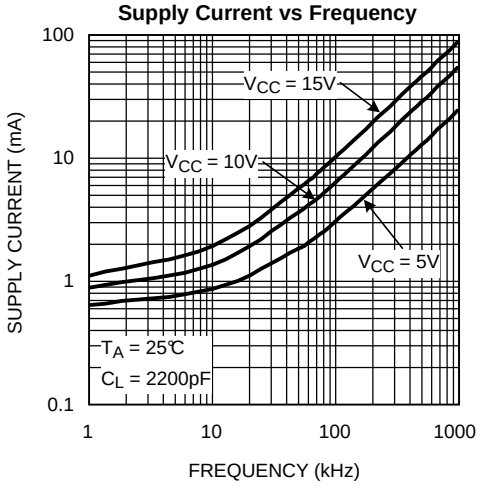


Figure 7.

Supply Current vs Capacitive Load

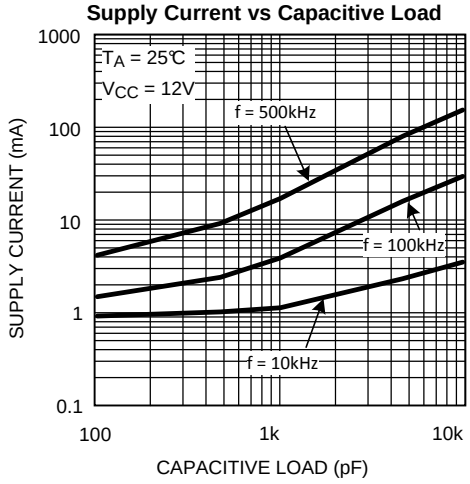


Figure 8.

Rise and Fall Time vs Supply Voltage

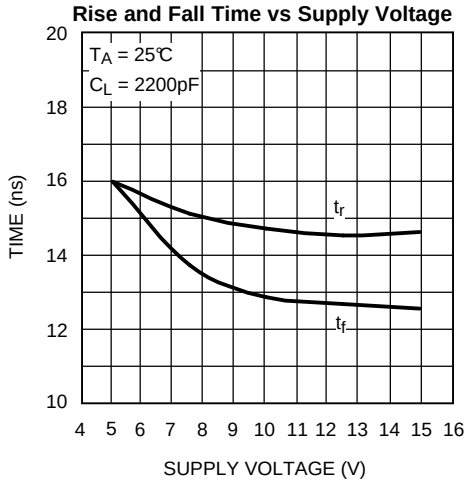


Figure 9.

Rise and Fall Time vs Temperature

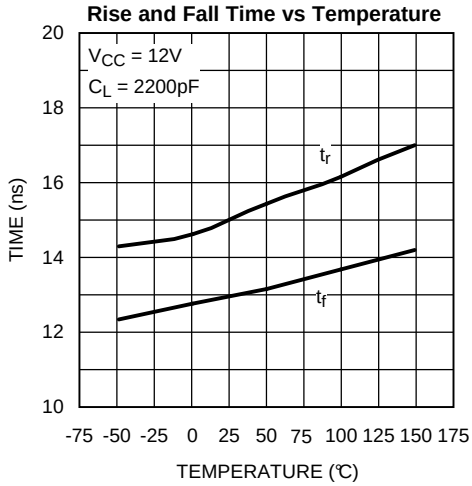


Figure 10.

Rise and Fall Time vs Capacitive Load

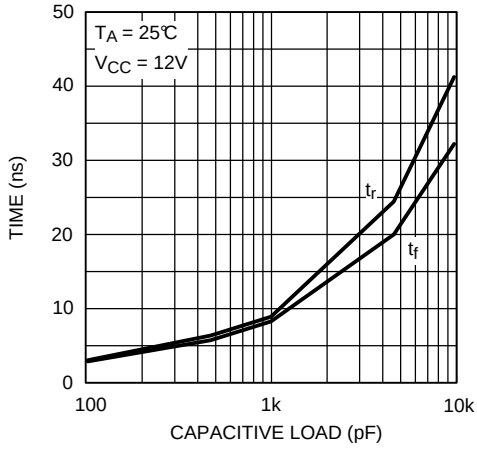


Figure 11.

Delay Time vs Supply Voltage

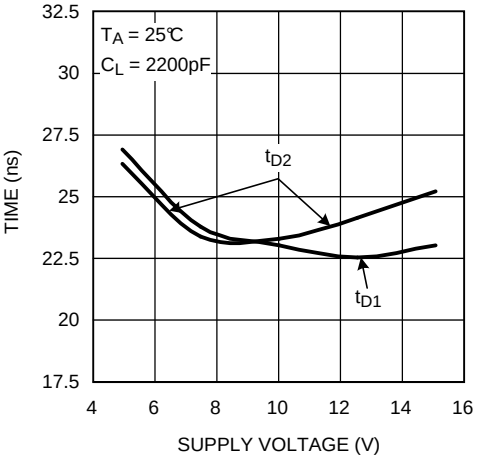


Figure 12.

Typical Performance Characteristics (continued)

Delay Time vs Temperature

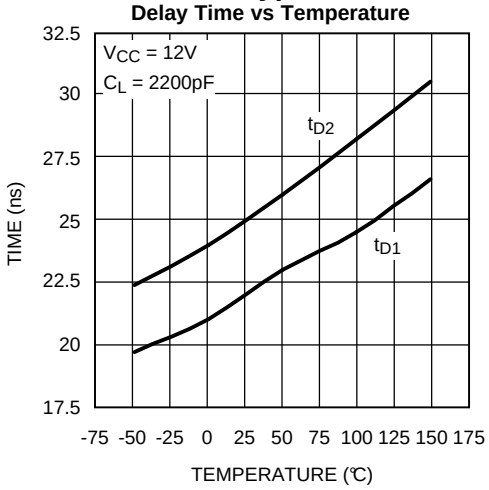


Figure 13.

RDSON vs Supply Voltage

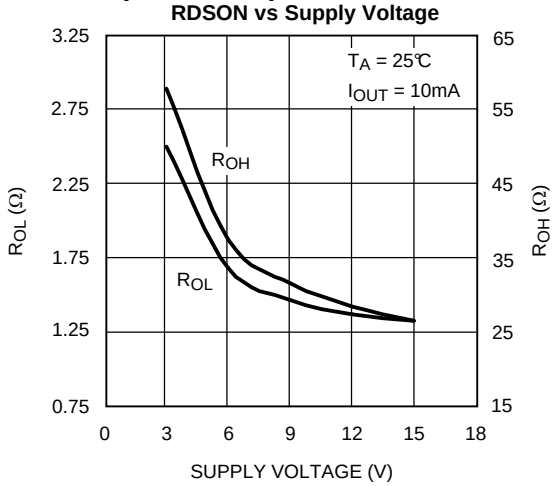


Figure 14.

UVLO Thresholds and Hysteresis vs Temperature

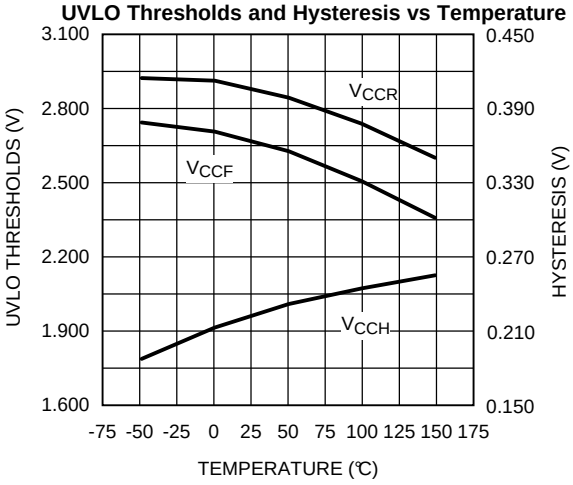


Figure 15.

DETAILED OPERATING DESCRIPTION

LM5110 dual gate driver consists of two independent and identical driver channels with TTL compatible logic inputs and high current totem-pole outputs that source or sink current to drive MOSFET gates. The driver output consist of a compound structure with MOS and bipolar transistor operating in parallel to optimize current capability over a wide output voltage and operating temperature range. The bipolar device provides high peak current at the critical threshold region of the MOSFET VGS while the MOS devices provide rail-to-rail output swing. The totem pole output drives the MOSFET gate between the gate drive supply voltage V_{CC} and the power ground potential at the V_{EE} pin.

The control inputs of the drivers are high impedance CMOS buffers with TTL compatible threshold voltages. The negative supply of the input buffer is connected to the input ground pin IN_REF. An internal level shifting circuit connects the logic input buffers to the totem pole output drivers. The level shift circuit and separate input/output ground pins provide the option of single supply or split supply configurations. When driving MOSFET gates from a single positive supply, the IN_REF and V_{EE} pins are both connected to the power ground. The LM5110 pinout was designed for compatibility with industry standard gate drivers in single supply gate driver applications. Pin 1 (IN_REF) on the LM5110 is a no-connect on standard driver IC's. Connecting pin 1 to pin 3 (V_{EE}) on the printed circuit board accommodates the pin-out of both the LM5110 and competitive drivers.

The isolated input/output grounds provide the capability to drive the MOSFET to a negative VGS voltage for a more robust and reliable off state. In split supply configuration, the IN_REF pin is connected to the ground of the controller which drives the LM5110 inputs. The V_{EE} pin is connected to a negative bias supply that can range from the IN-REF as much as 14V below the V_{CC} gate drive supply. The maximum recommended voltage difference between V_{CC} and IN_REF or between V_{CC} and V_{EE} is 14V. The minimum voltage difference between V_{CC} and IN_REF is 3.5V.

Enhancement mode MOSFETs do not inherently require a negative bias on the gate to turn off the FET. However, certain applications may benefit from the capability of negative VGS voltage during turn-off including:

1. when the gate voltages cannot be held safely below the threshold voltage due to transients or coupling in the printed circuit board.
2. when driving low threshold MOSFETs at high junction temperatures
3. when high switching speeds produce capacitive gate-drain current that lifts the internal gate potential of the MOSFET

The two driver channels of the LM5110 are designed as identical cells. Transistor matching inherent to integrated circuit manufacturing ensures that the ac and dc performance of the channels are nearly identical. Closely matched propagation delays allow the dual driver to be operated as a single driver if inputs and output pins are connected. The drive current capability in parallel operation is 2X the drive of either channel. Small differences in switching speed between the driver channels will produce a transient current (shoot-through) in the output stage when two output pins are connected to drive a single load. The efficiency loss for parallel operation has been characterized at various loads, supply voltages and operating frequencies. The power dissipation in the LM5110 increases by less than 1% relative to the dual driver configuration when operated as a single driver with inputs and outputs connected.

An Under-voltage lockout (UVLO) circuit is included in the LM5110, which senses the voltage difference between V_{CC} and the input ground pin, IN_REF. When the V_{CC} to IN_REF voltage difference falls below 2.7V both driver channels are disabled. The driver will resume normal operation when the V_{CC} to IN_REF differential voltage exceeds approximately 2.9V. UVLO hysteresis prevents chattering during brown-out conditions.

The Shutdown pin (nSHDN) is a TTL compatible logic input provided to enable/disable both driver channels. When nSHDN is in the logic low state, the LM5110 is switched to a low power standby mode with total supply current less than 25 µA. This function can be effectively used for start-up, thermal overload, or short circuit fault protection. It is recommended that this pin be connected to V_{CC} when the shutdown function is not being used. The shutdown pin has an internal 18µA current source pull-up to V_{CC}.

The input pins of non-inverting drivers have an internal 18µA current source pull-down to IN-REF. The input pins of inverting driver channels have neither pull-up nor pull-down current sources.

The LM5110 is available in dual non-inverting (-1), dual inverting (-2) and the combination inverting plus non-inverting (-3) configurations. All three configurations are offered in the SOIC-8 and WSON-10 plastic packages.

Layout Considerations

Attention must be given to board layout when using LM5110. Some important considerations include:

1. A Low ESR/ESL capacitor must be connected close to the IC and between the V_{CC} and V_{EE} pins to support high peak currents being drawn from V_{CC} during turn-on of the MOSFET.
2. Proper grounding is crucial. The drivers need a very low impedance path for current return to ground avoiding inductive loops. The two paths for returning current to ground are a) between LM5110 IN-REF pin and the ground of the circuit that controls the driver inputs, b) between LM5110 V_{EE} pin and the source of the power MOSFET being driven. All these paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance. All these ground paths should be kept distinctly separate to avoid coupling between the high current output paths and the logic signals that drive the LM5110. A good method is to dedicate one copper plane in a multi-layered PCB to provide a common ground surface.
3. With the rise and fall times in the range of 10 ns to 30 ns, care is required to minimize the lengths of current carrying conductors to reduce their inductance and EMI from the high di/dt transients generated by the LM5110.
4. The LM5110 SOIC footprint is compatible with other industry standard drivers. Simply connect IN_REF pin of the LM5110 to V_{EE} (pin 1 to pin 3) to operate the LM5110 in a standard single supply configuration.
5. If either channel is not being used, the respective input pin (IN_A or IN_B) should be connected to either IN_REF or V_{CC} to avoid spurious output signals. If the shutdown feature is not used, the nSHDN pin should be connected to V_{CC} to avoid erratic behavior that would result if system noise were coupled into a floating 'nSHDN' pin.

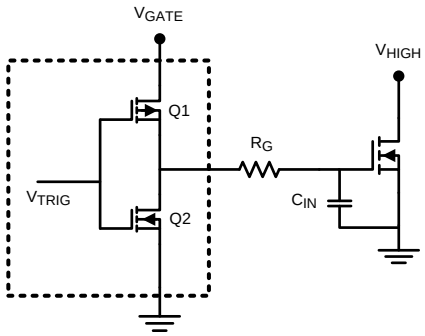
Thermal Performance

INTRODUCTION

The primary goal of thermal management is to maintain the integrated circuit (IC) junction temperature (T_J) below a specified maximum operating temperature to ensure reliability. It is essential to estimate the maximum T_J of IC components in worst case operating conditions. The junction temperature is estimated based on the power dissipated in the IC and the junction to ambient thermal resistance θ_{JA} for the IC package in the application board and environment. The θ_{JA} is not a given constant for the package and depends on the printed circuit board design and the operating environment.

DRIVE POWER REQUIREMENT CALCULATIONS IN LM5110

The LM5110 dual low side MOSFET driver is capable of sourcing/sinking 3A/5A peak currents for short intervals to drive a MOSFET without exceeding package power dissipation limits. High peak currents are required to switch the MOSFET gate very quickly for operation at high frequencies.



The schematic above shows a conceptual diagram of the LM5110 output and MOSFET load. Q1 and Q2 are the switches within the gate driver. R_G is the gate resistance of the external MOSFET, and C_{IN} is the equivalent gate capacitance of the MOSFET. The gate resistance Rg is usually very small and losses in it can be neglected. The equivalent gate capacitance is a difficult parameter to measure since it is the combination of C_{GS} (gate to source capacitance) and C_{GD} (gate to drain capacitance). Both of these MOSFET capacitances are not constants and vary with the gate and drain voltage. The better way of quantifying gate capacitance is the total gate charge Q_G in coloumbs. Q_G combines the charge required by C_{GS} and C_{GD} for a given gate drive voltage V_{GATE}.

Assuming negligible gate resistance, the total power dissipated in the MOSFET driver due to gate charge is approximated by

$P_{DRIVER} = V_{GATE} \times Q_G \times F_{SW}$

where

- F_{SW} = switching frequency of the MOSFET

As an example, consider the MOSFET MTD6N15 whose gate charge specified as 30 nC for V_{GATE} = 12V.

The power dissipation in the driver due to charging and discharging of MOSFET gate capacitances at switching frequency of 300 kHz and V_{GATE} of 12V is equal to

P_{DRIVER} = 12V x 30 nC x 300 kHz = 0.108W.

If both channels of the LM5110 are operating at equal frequency with equivalent loads, the total losses will be twice as this value which is 0.216W.

In addition to the above gate charge power dissipation, - transient power is dissipated in the driver during output transitions. When either output of the LM5110 changes state, current will flow from V_{CC} to V_{EE} for a very brief interval of time through the output totem-pole N and P channel MOSFETs. The final component of power dissipation in the driver is the power associated with the quiescent bias current consumed by the driver input stage and Under-voltage lockout sections.

Characterization of the LM5110 provides accurate estimates of the transient and quiescent power dissipation components. At 300 kHz switching frequency and 30 nC load used in the example, the transient power will be 8 mW. The 1 mA nominal quiescent current and 12V V_{GATE} supply produce a 12 mW typical quiescent power.

Therefore the total power dissipation

P_D = 0.216 + 0.008 + 0.012 = 0.236W.

We know that the junction temperature is given by

$T_J = P_D \times \theta_{JA} + T_A$

Or the rise in temperature is given by

$T_{RISE} = T_J - T_A = P_D \times \theta_{JA}$

For SOIC-8 package θ_{JA} is estimated as 170°C/W for the conditions of natural convection.

Therefore T_{RISE} is equal to

T_{RISE} = 0.236 x 170 = 40.1°C

For WSON-10 package, the integrated circuit die is attached to leadframe die pad which is soldered directly to the printed circuit board. This substantially decreases the junction to ambient thermal resistance (θ_{JA}). θ_{JA} as low as 40°C/W is achievable with the WSON10 package. The resulting T_{RISE} for the dual driver example above is thereby reduced to just 9.5 degrees.

CONTINUOUS CURRENT RATING OF LM5110

The LM5110 can deliver pulsed source/sink currents of 3A and 5A to capacitive loads. In applications requiring continuous load current (resistive or inductive loads), package power dissipation, limits the LM5110 current capability far below the 5A sink/3A source capability. Rated continuous current can be estimated both when sourcing current to or sinking current from the load. For example when sinking, the maximum sink current can be calculated as

$$I_{SINK}(MAX) := \sqrt{\frac{T_J(MAX) - T_A}{\theta_{JA} \cdot R_{DS}(ON)}}$$

where

- R_{DS}(on) is the on resistance of lower MOSFET in the output stage of LM5110

Consider T_J(max) of 125°C and θ_{JA} of 170°C/W for an SO-8 package under the condition of natural convection and no air flow. If the ambient temperature (T_A) is 60°C, and the R_{DS}(on) of the LM5110 output at T_J(max) is 2.5Ω, this equation yields I_{SINK}(max) of 391mA which is much smaller than 5A peak pulsed currents.

Similarly, the maximum continuous source current can be calculated as

$$I_{SOURCE}(MAX) := \frac{T_J(MAX) - T_A}{\theta_{JA} \cdot V_{DIODE}}$$

where

- V_{DIODE} is the voltage drop across hybrid output stage which varies over temperature and can be assumed to be about 1.1V at T_J(max) of 125°C

Assuming the same parameters as above, this equation yields I_{SOURCE}(max) of 347mA.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5110-1M	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	5110 -1M	Samples
LM5110-1M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5110 -1M	Samples
LM5110-1MX	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	5110 -1M	Samples
LM5110-1MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5110 -1M	Samples
LM5110-1SD	ACTIVE	WSON	DPR	10	1000	TBD	Call TI	Call TI	-40 to 125	5110-1	Samples
LM5110-1SD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5110-1	Samples
LM5110-1SDX	ACTIVE	WSON	DPR	10		TBD	Call TI	Call TI	-40 to 125	5110-1	Samples
LM5110-1SDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5110-1	Samples
LM5110-2M	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	5110 -2M	Samples
LM5110-2M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5110 -2M	Samples
LM5110-2MX	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	5110 -2M	Samples
LM5110-2MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5110 -2M	Samples
LM5110-2SD	ACTIVE	WSON	DPR	10		TBD	Call TI	Call TI	-40 to 125	5110-2	Samples
LM5110-2SD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5110-2	Samples
LM5110-2SDX	ACTIVE	WSON	DPR	10		TBD	Call TI	Call TI	-40 to 125	5110-2	Samples
LM5110-2SDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5110-2	Samples
LM5110-3M	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	5110 -3M	Samples
LM5110-3M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5110 -3M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5110-3MX	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	5110 -3M	Samples
LM5110-3MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5110 -3M	Samples
LM5110-3SD	ACTIVE	WSON	DPR	10	1000	TBD	Call TI	Call TI	-40 to 125	5110-3	Samples
LM5110-3SD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5110-3	Samples
LM5110-3SDX	ACTIVE	WSON	DPR	10		TBD	Call TI	Call TI	-40 to 125	5110-3	Samples
LM5110-3SDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5110-3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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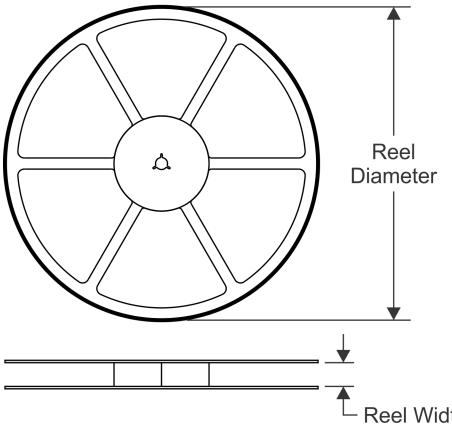
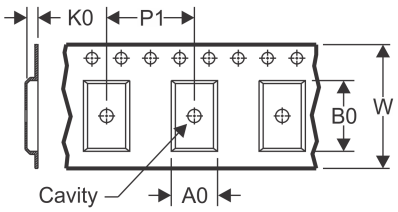
TAPE AND REEL INFORMATION

REEL DIMENSIONS

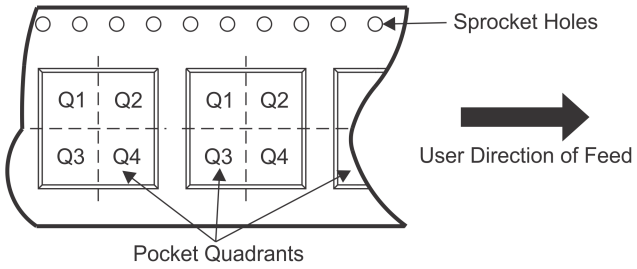


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

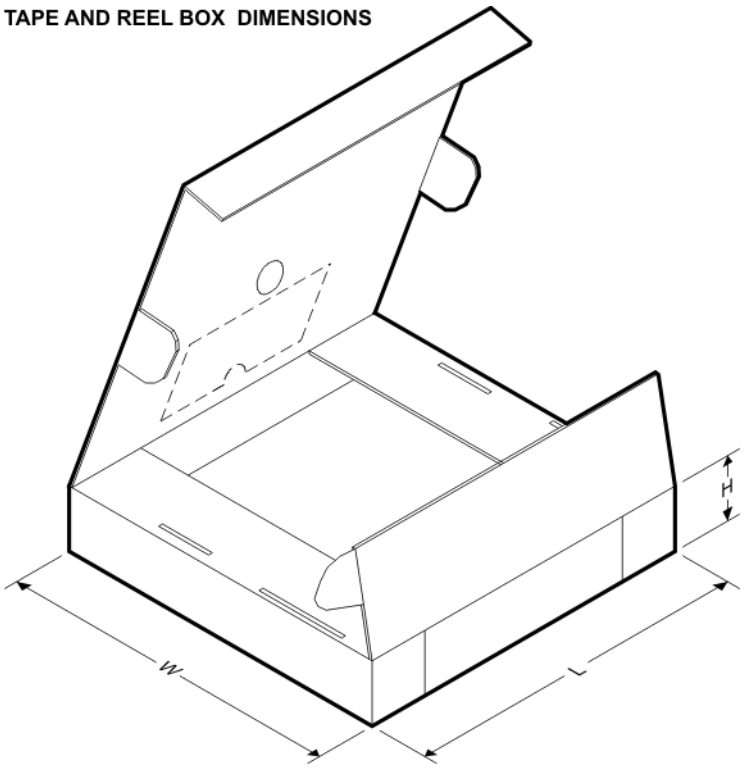
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5110-1MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5110-1SD	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5110-1SD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5110-1SDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5110-2MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5110-2SD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5110-2SDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5110-3MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5110-3SD	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5110-3SD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5110-3SDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

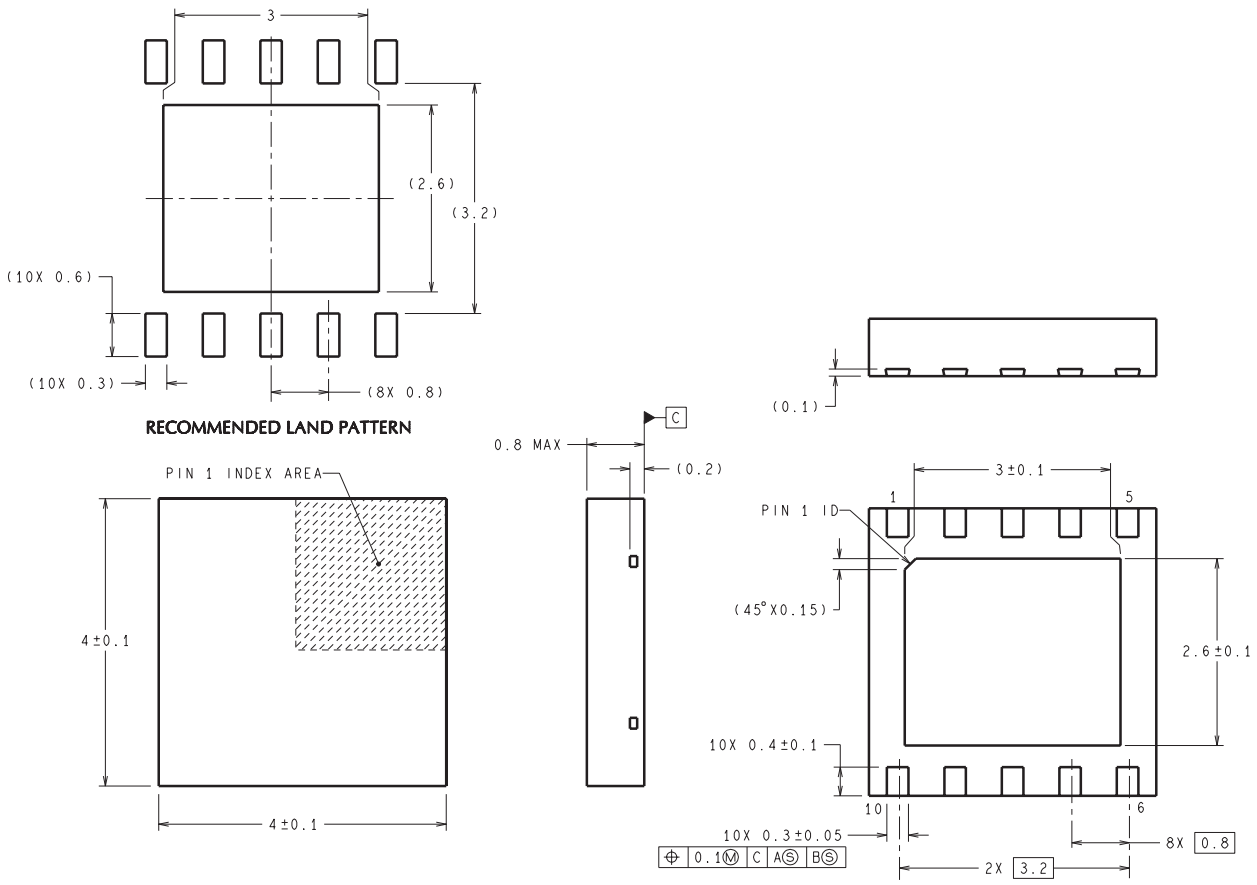
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5110-1MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5110-1SD	WSON	DPR	10	1000	210.0	185.0	35.0
LM5110-1SD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5110-1SDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0
LM5110-2MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5110-2SD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5110-2SDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0
LM5110-3MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5110-3SD	WSON	DPR	10	1000	210.0	185.0	35.0
LM5110-3SD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5110-3SDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0

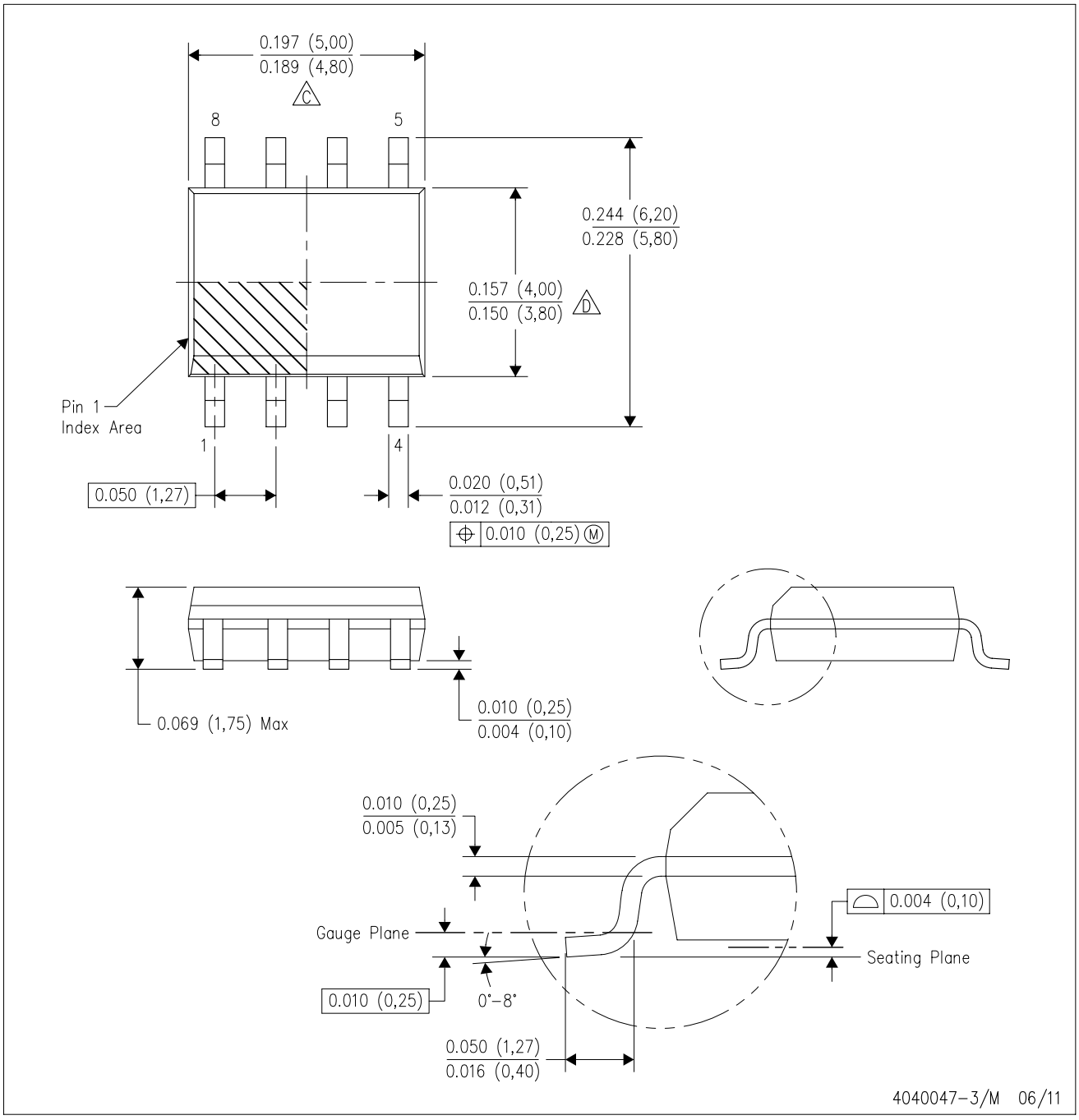
DPR0010A



DIMENSIONS ARE IN MILLIMETERS

SDC10A (Rev A)

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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