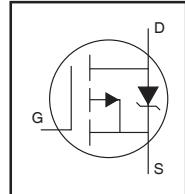
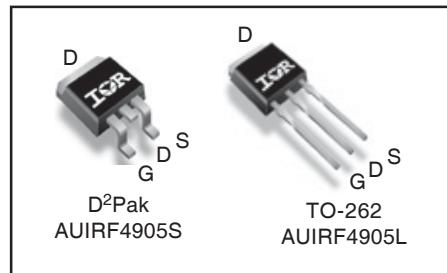


AUIRF4905S/L

HEXFET® Power MOSFET

	$V_{(BR)DSS}$	-55V
$R_{DS(on)}$ max.	20mΩ	
I_D (Silicon Limited)	-70A	
I_D (Package Limited)	-42A	



G	D	S
Gate	Drain	Source

Description

Specifically designed for Automotive applications, this cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	-70	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	-44	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	-42	
I_{DM}	Pulsed Drain Current ①	-280	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	170	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	140	mJ
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value ⑥	790	
I_{AR}	Avalanche Current ①	See Fig. 12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ①		mJ
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting Torque, 6-32 or M3 screw ⑦	10 lbf·in (1.1N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R_{QC}	Junction-to-Case ⑧	—	0.75	°C/W
R_{QA}	Junction-to-Ambient (PCB mount) ⑦⑧	—	40	

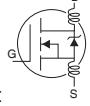
HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>
www.irf.com

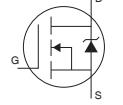
Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	-55	—	—	V	$V_{\text{GS}} = 0\text{V}$, $I_D = -250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	-0.054	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	—	20	$\text{m}\Omega$	$V_{\text{GS}} = -10\text{V}$, $I_D = -42\text{A}$ ④
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = -250\mu\text{A}$
g_{fs}	Forward Transconductance	19	—	—	S	$V_{\text{DS}} = -25\text{V}$, $I_D = -42\text{A}$ ⑤
I_{bss}	Drain-to-Source Leakage Current	—	—	-25	μA	$V_{\text{DS}} = -55\text{V}$, $V_{\text{GS}} = 0\text{V}$
		—	—	-250		$V_{\text{DS}} = -44\text{V}$, $V_{\text{GS}} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{\text{GS}} = -20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{\text{GS}} = 20\text{V}$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	—	120	180	nC	$I_D = -42\text{A}$
Q_{gs}	Gate-to-Source Charge	—	32	—		$V_{\text{DS}} = -44\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	53	—		$V_{\text{GS}} = -10\text{V}$ ③
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	20	—	ns	$V_{\text{DD}} = -28\text{V}$
t_r	Rise Time	—	99	—		$I_D = -42\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	51	—		$R_G = 2.6\ \Omega$
t_f	Fall Time	—	64	—		$V_{\text{GS}} = -10\text{V}$ ③
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3500	—	pF	$V_{\text{GS}} = 0\text{V}$
C_{oss}	Output Capacitance	—	1250	—		$V_{\text{DS}} = -25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	450	—		$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	4620	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = -1.0\text{V}$, $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	940	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = -44\text{V}$, $f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance	—	1530	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 0\text{V}$ to -44V ④

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-42	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-280		
V_{SD}	Diode Forward Voltage	—	—	-1.3	V	$T_J = 25^\circ\text{C}$, $I_S = -42\text{A}$, $V_{\text{GS}} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	61	92	ns	$T_J = 25^\circ\text{C}$, $I_F = -42\text{A}$, $V_{\text{DD}} = -28\text{V}$
Q_{rr}	Reverse Recovery Charge	—	150	220	nC	$\text{di}/\text{dt} = 100\text{A}/\mu\text{s}$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.16\text{mH}$ ⑥ $R_G = 25\Omega$, $I_{\text{AS}} = -42\text{A}$, $V_{\text{GS}} = -10\text{V}$. Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
- ④ $C_{\text{oss eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R_θ is measured at T_J approximately 90°C

Qualification Information[†]

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level	TO-262	N/A	
	D ² Pak	MSL1	
ESD	Machine Model	Class M4 (+/- 425V) ^{††} AEC-Q101-002	
	Human Body Model	Class H2 (+/- 4000V) ^{††} AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V) ^{††} AEC-Q101-005	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

^{††} Highest passing voltage.

AUIRF4905S/L

International
Rectifier

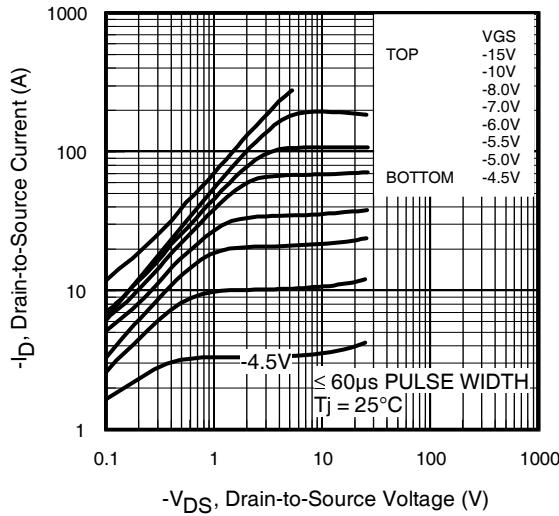


Fig 1. Typical Output Characteristics

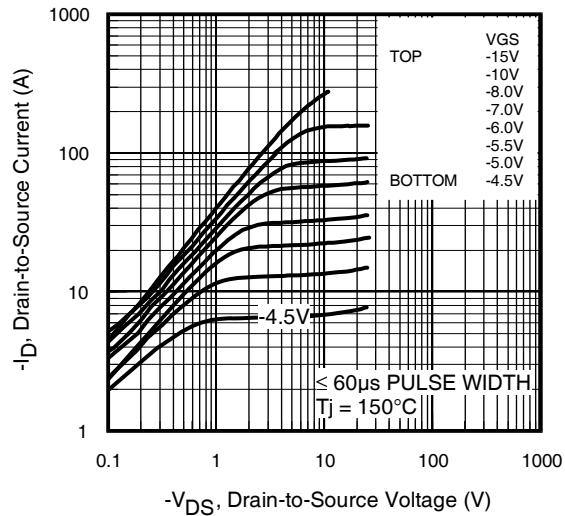


Fig 2. Typical Output Characteristics

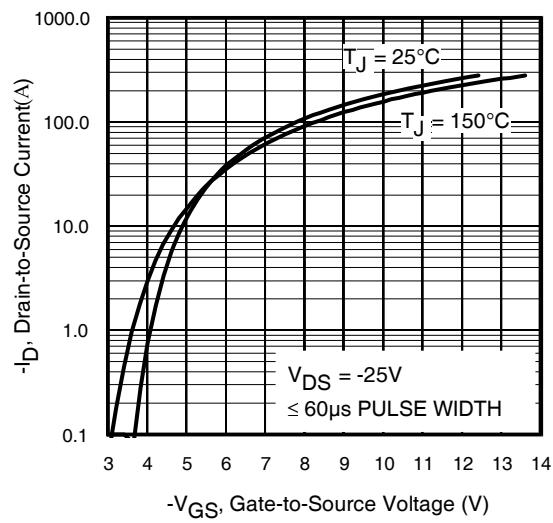


Fig 3. Typical Transfer Characteristics

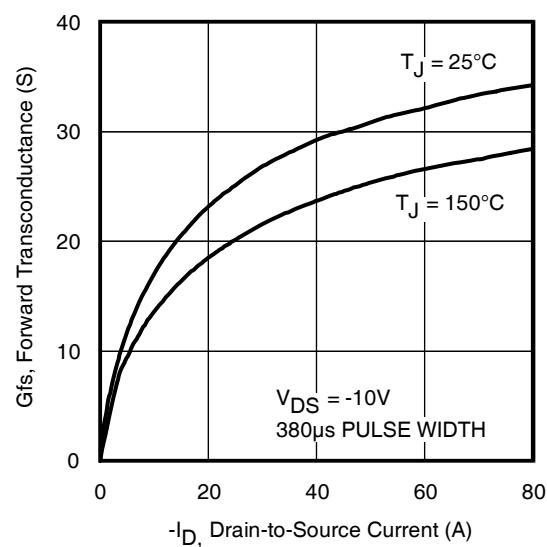


Fig 4. Typical Forward Transconductance Vs. Drain Current

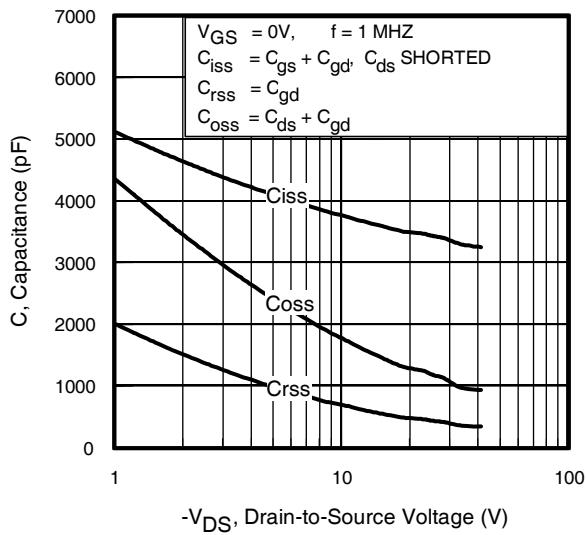


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

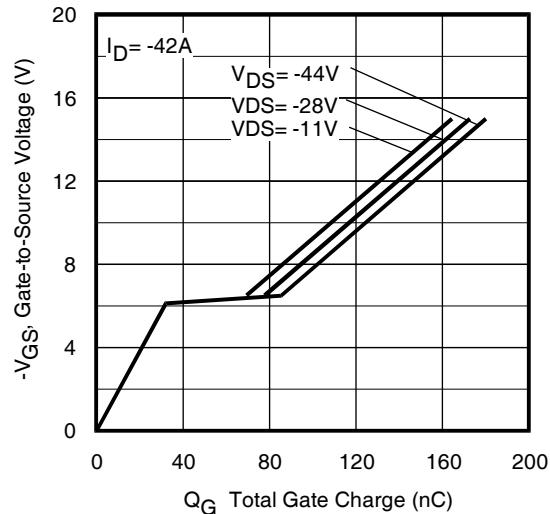


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

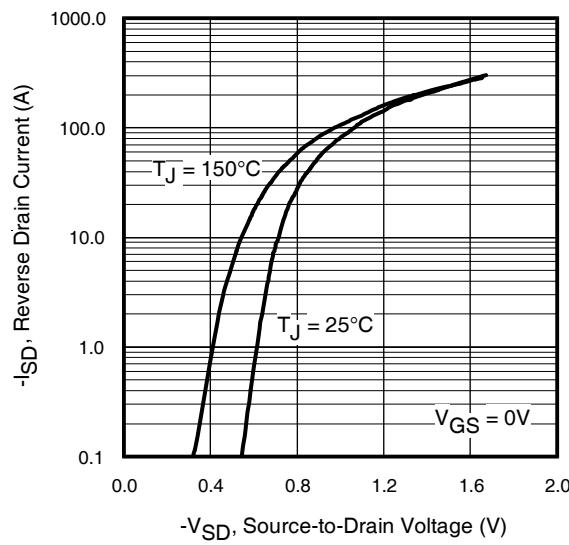


Fig 7. Typical Source-Drain Diode
Forward Voltage

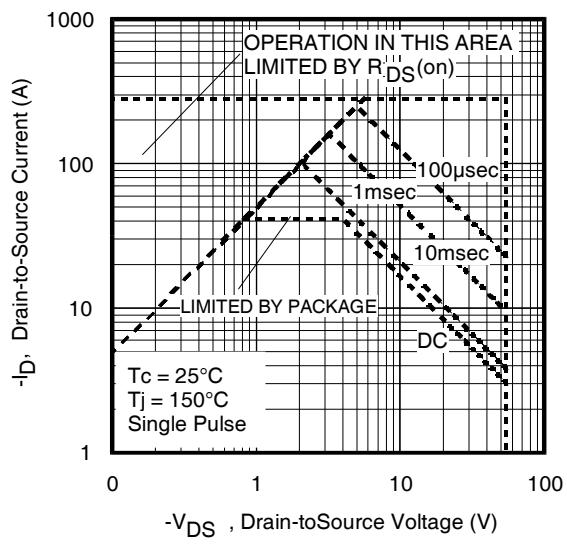


Fig 8. Maximum Safe Operating Area

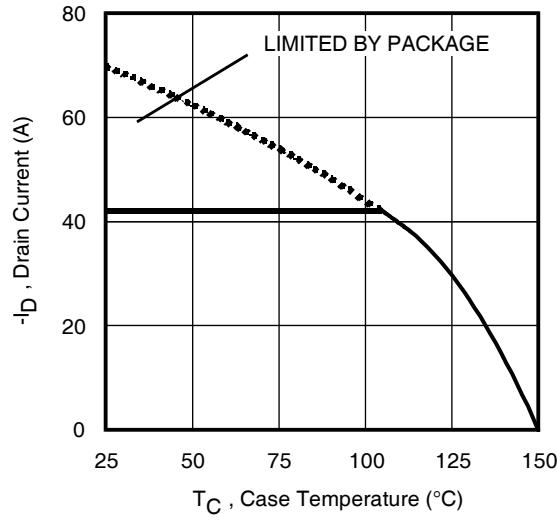


Fig 9. Maximum Drain Current Vs.
Case Temperature

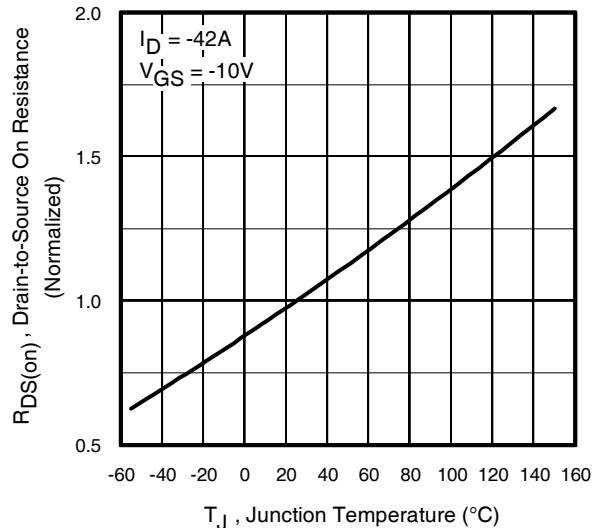


Fig 10. Normalized On-Resistance
Vs. Temperature

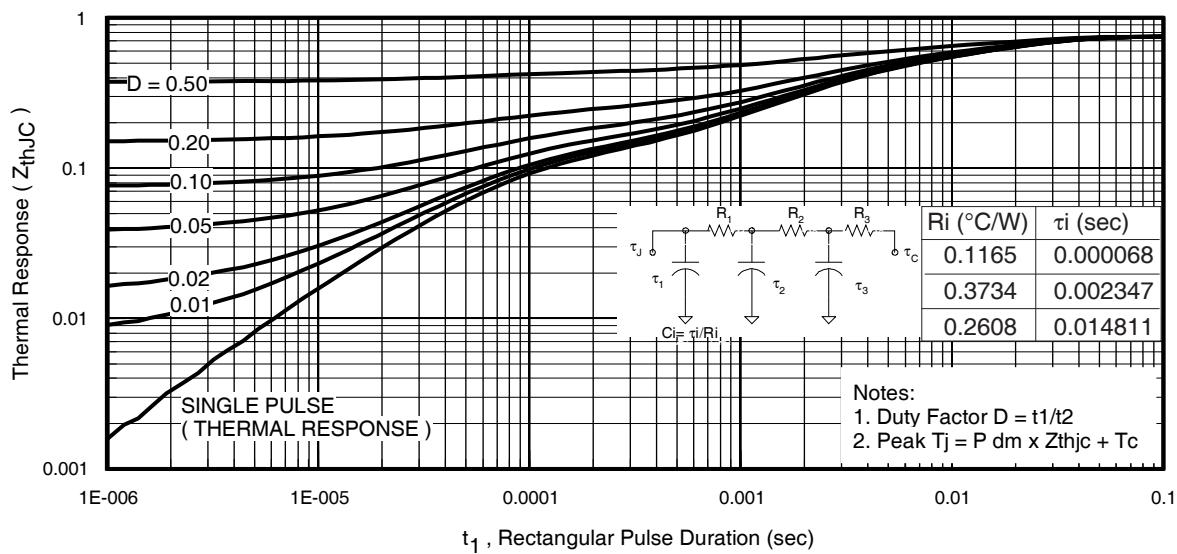


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

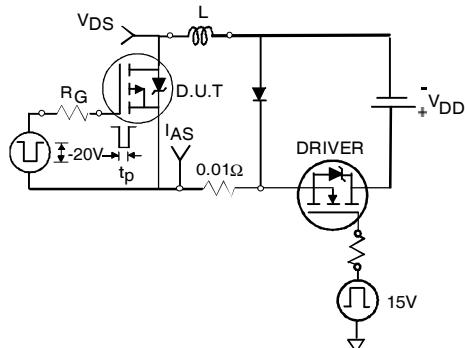


Fig 12a. Unclamped Inductive Test Circuit

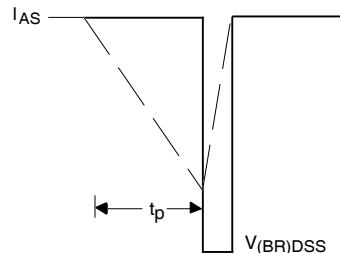


Fig 12b. Unclamped Inductive Waveforms

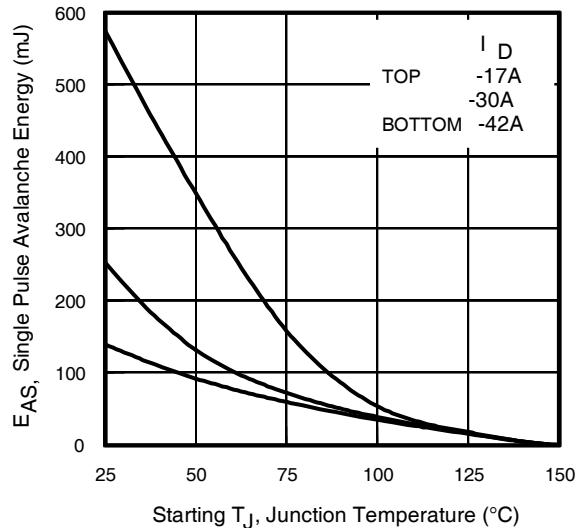


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

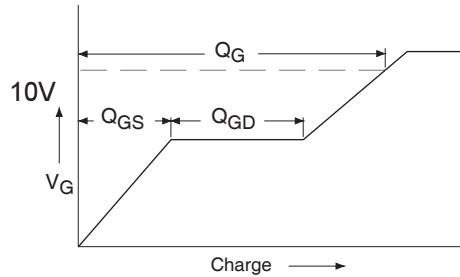


Fig 13a. Basic Gate Charge Waveform

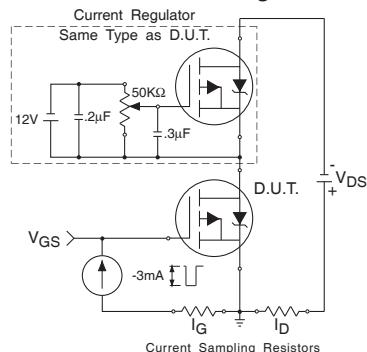


Fig 13b. Gate Charge Test Circuit

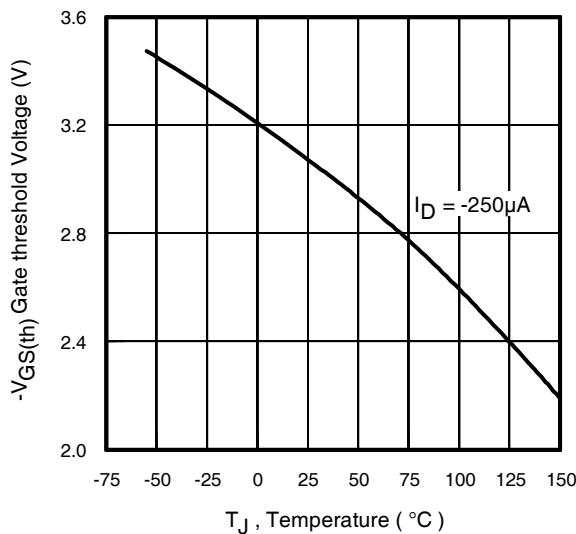


Fig 14. Threshold Voltage Vs. Temperature

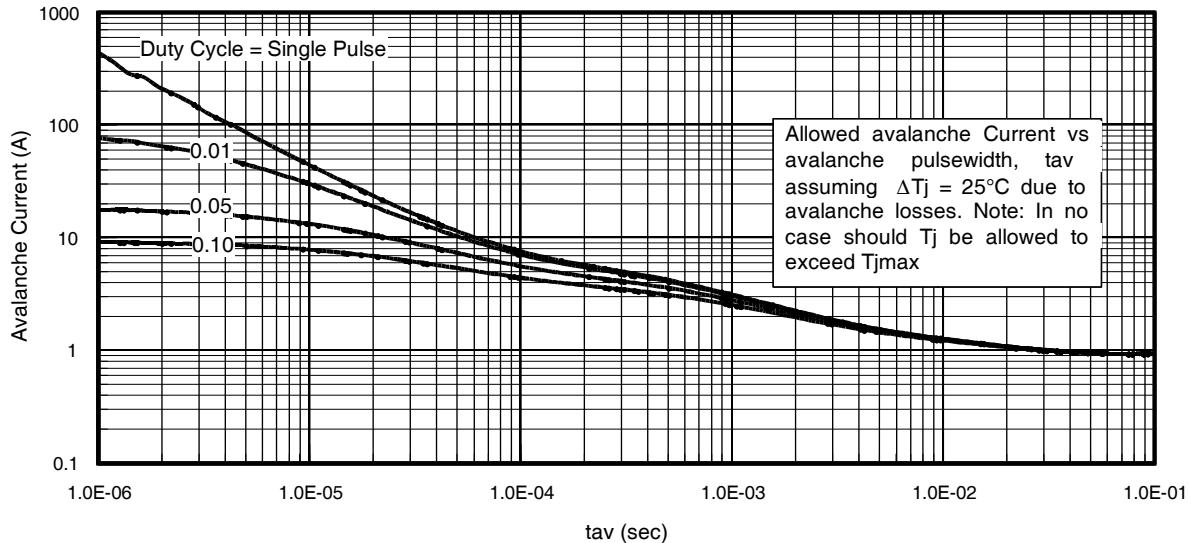


Fig 15. Typical Avalanche Current Vs.Pulsewidth

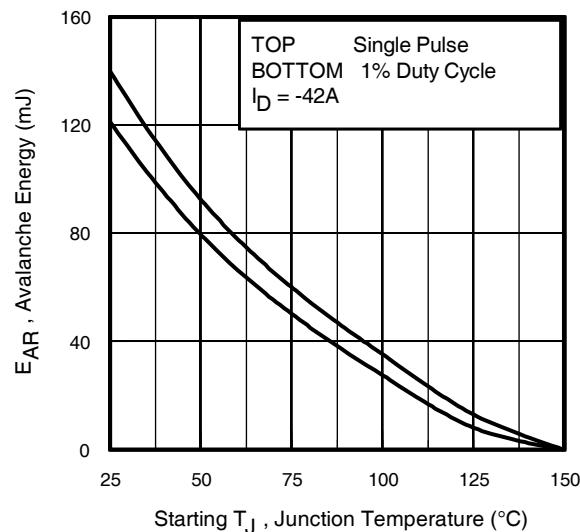


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
- t_{av} = Average time in avalanche.
- D = Duty cycle in avalanche = $t_{av} \cdot f$
- $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

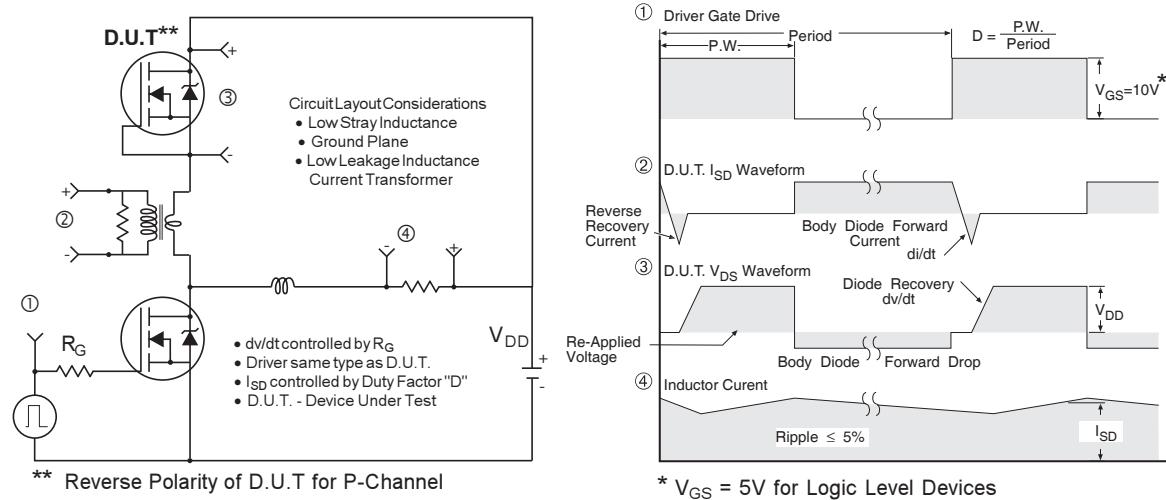


Fig 17. Peak Diode Recovery dv/dt Test Circuit for P-Channel HEXFET® Power MOSFETs

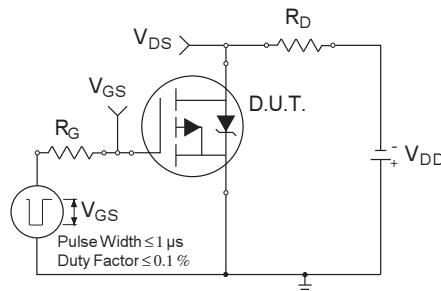


Fig 18a. Switching Time Test Circuit

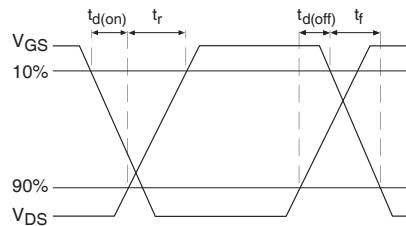


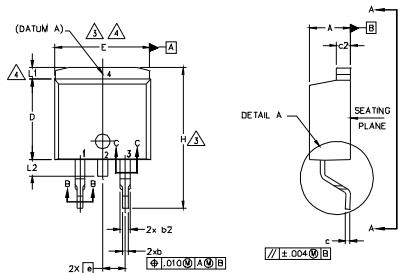
Fig 18b. Switching Time Waveforms

AUIRF4905S/L

International
IR Rectifier

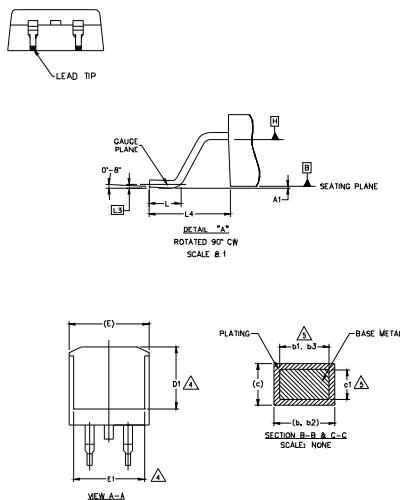
D²Pak Package Outline

(Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.



S Y M B O L	DIMENSIONS				N O T E S	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190		
A1	0.00	0.254	.000	.010		
b	0.51	0.99	.020	.039	5	
b1	0.51	0.89	.020	.035		
b2	1.14	1.78	.045	.070		
b3	1.14	1.73	.045	.068	5	
c	0.38	0.74	.015	.029		
c1	0.38	0.58	.015	.023	5	
c2	1.14	1.65	.045	.065		
D	8.38	9.65	.330	.380		
D1	6.86	—	.270		4	
E	9.65	10.67	.380	.420	3.4	
E1	6.22	—	.245		4	
e	2.54	BSC	.100	BSC		
H	14.61	15.88	.575	.625		
L	1.78	2.79	.070	.110		
L1	—	1.65	—	.066	4	
L2	1.27	1.78	—	.070		
L3	0.25	BSC	.010	BSC		
L4	4.78	5.28	.188	.208		

LEAD ASSIGNMENTS

HEXFET

- 1. - GATE
- 2. 4. - DRAIN
- 3. - SOURCE

IGBTs - CoPACK

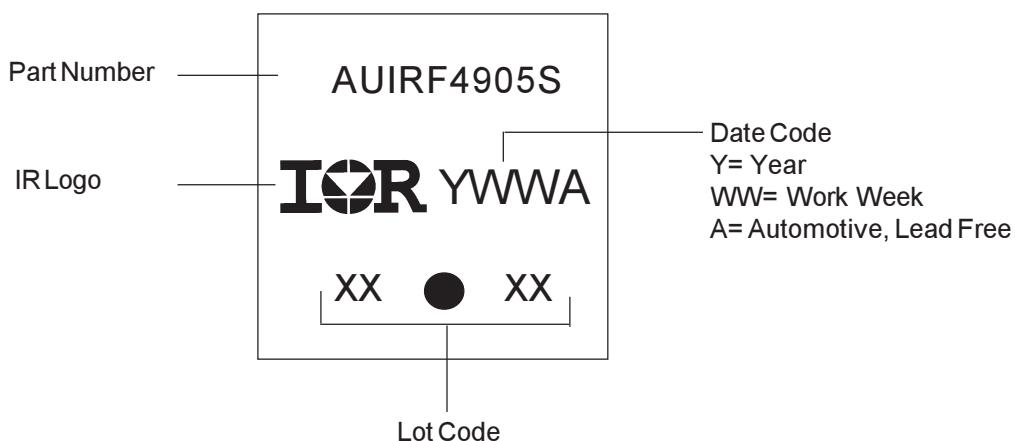
- 1. - GATE
- 2. 4. - COLLECTOR
- 3. - Emitter

DIODES

1. - ANODE *
2. 4. - CATHODE
3. - ANODE

* PART DEPENDENT

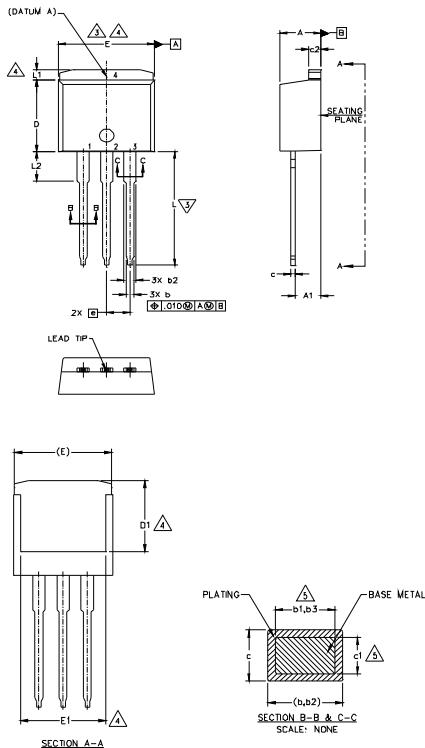
D²Pak Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TO-262 Package Outline

Dimensions are shown in millimeters (inches)

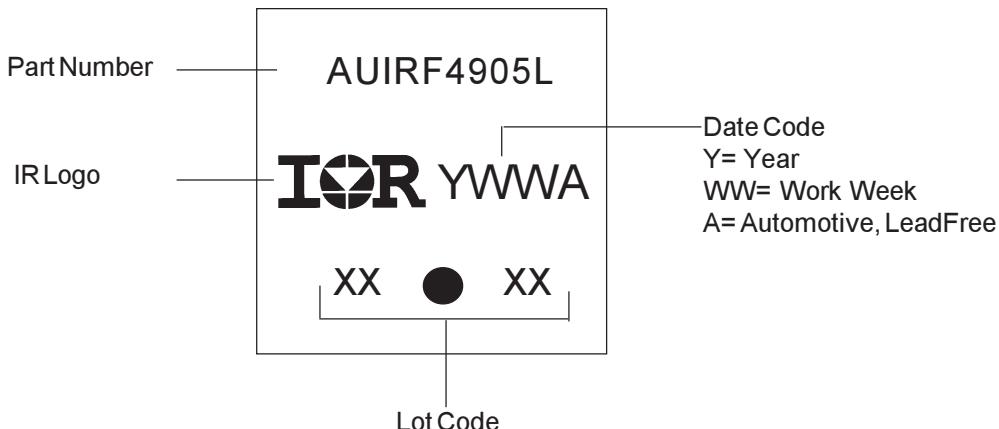


SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190		
A1	2.03	3.02	.080	.119		
b	0.51	0.99	.020	.039		
b1	0.51	0.89	.020	.035	5	
b2	1.14	1.78	.045	.070		
b3	1.14	1.73	.045	.068	5	
c	0.38	0.74	.015	.029		
c1	0.38	0.58	.015	.023	5	
c2	1.14	1.65	.045	.065		
D	8.38	9.65	.330	.380	3	
D1	6.86	—	.270	—	4	
E	9.65	10.67	.380	.420	3,4	
E1	6.22	—	.245	—	4	
e	2.54	BSC	.100	BSC		
L	13.46	14.10	.530	.555		
L1	—	1.65	—	.065		
L2	3.56	3.71	.140	.146	4	

NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
 △ DIMENSION D & E DO NOT INCLUDE WELD FLASH. WELD FLASH SHALL NOT EXCEED 0.127 (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 △ INTERNAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
 △ DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 6. CONTROLLING DIMENSIONS INCH.
 7. - PLATING CONTOUR TO JEDEC TO-262 EXCEPT A1(1mm), B2(0mm) AND D1(0mm)
 WHERE DIMENSIONS DENOTE THE ACTUAL PACKAGE OUTLINE

LEAD ASSIGNMENTS
 IC01, DPA01
 1. - GATE
 2. - DRAIN
 3. - SOURCE
 4. - COLLECTOR
 HOOKUP
 1. - GATE 2. - ANODE (NO DE) / OPEN (ONE DE)
 3. - DRAIN 4. - CATHODE
 5. - SOURCE
 6. - ANODE
 7. - DRAIN

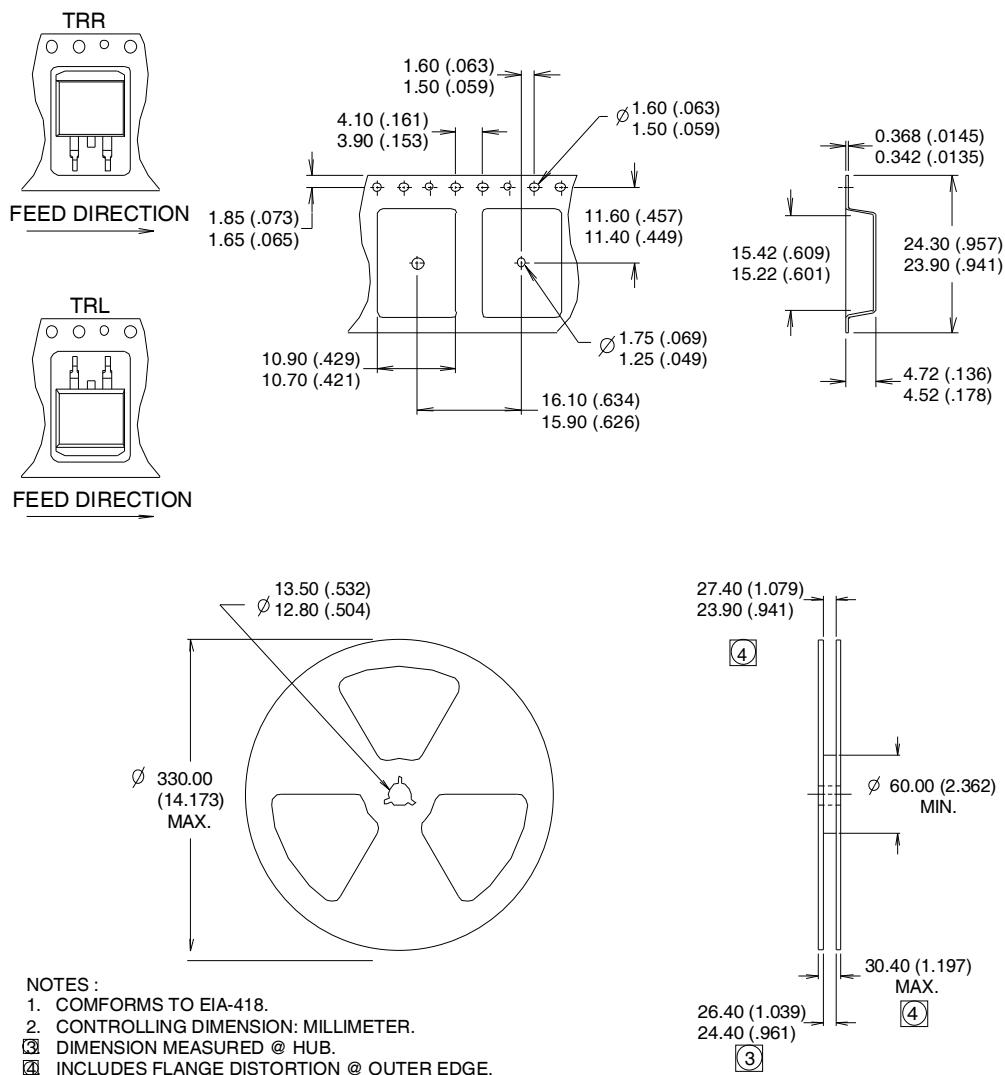
TO-262 Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRF4905L	TO-262	Tube	50	AUIRF4905L
AUIRF4905S	D2Pak	Tube	50	AUIRF4905S
		Tape and Reel Left	800	AUIRF4905STRL
		Tape and Reel Right	800	AUIRF4905STRR

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