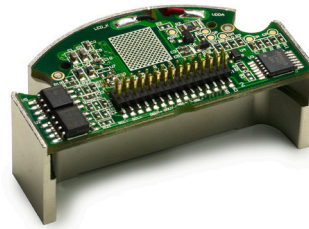


AEAT-9000-1GSH0 (Full Option)

Ultra-precision 17-Bit Absolute Single Turn Encoder



Data Sheet



Description

Avago Technologies' AEAT-9000 series are high resolution single turn optical absolute encoders. They are designed to allow users to achieve superior positioning performance in terms of speed and accuracy performance. The modular package enables the encoder to be directly integrated to the motor unlike conventional encoders. As a result, users can expect cost savings and better performance of the overall system.

The AEAT-9000 addresses key qualities that are motor-related such as position accuracy, speed stability, and bandwidth which determine command-signal response, disturbance rejection capability, power loss, size, and quietness. They are capable of the industry's best accuracy for an absolute encoder.

The AEAT-9000 is a modular absolute encoder that consists of a read head module and a high-precision code disc [(HEDG-9000-H13 & HEDG-9000-H14) which is ordered separately]. The modular design allows for better flexibility to system designers to easily design-in the encoder feedback system.

NOTE: Avago Technologies encoders are not recommended for use in safety critical applications, e.g., ABS braking systems, power steering, life support systems and critical care medical equipment. Avago's products and software are not specifically designed, manufactured or authorized for sale as parts, components or assemblies for the planning, construction, maintenance or direct operation of a nuclear facility or for use in medical devices or applications. Customer is solely responsible, and waives all rights to make claims against Avago or its suppliers, for all loss, damage, expense or liability in connection with such use. Please contact sales representative if more clarification is needed.

Features

- 17-bit absolute single turn output (131072 absolute positions over 360°)
- 2 channel true differential Sine/Cosine outputs with 2048 cycles per revolution
- 2048 CPR A/B channel incremental digital output
- Interface output is SSI (2wire SSI / 3wire SSI) with RS485 line transceiver or single ended option
- On-chip interpolation and code correction compensate for mounting tolerance
- Selectable direction for Up/Down position counter
- Electrical alignment output for tilt and locate
- Built-in monitor track for monitoring of LED light level
- Error output for LED degradation
- -40 to 115° C operating temperature

Applications

Typical applications include

- Rotary applications up to 17 bits/360° absolute position
- Integration into servo motors
- Industrial and maritime valve control
- High precision test and measurement machines
- Industrial and factory automation equipments
- Textile, woodworking & packaging machineries
- Nacelle & blades control in wind turbine

ESD WARNING: HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T _S	-40	85	°C
Operating Temperature	T _A	-40	115	°C
Supply Voltage	V _{DD}	-0.3	6	V
Voltages at all input and output pins	V _{in} & V _{out}	-0.3	V _{DD} +0.3	V

Note: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables "Recommended Operating Conditions and Characteristics" provide conditions for actual device operation.

Recommended Operating Conditions

Description	Symbol	Min.	Typical	Max.	Units	Notes
Temperature	T _A	-40	25	115	°C	
Supply Voltage	V _{DD}	4.5	5	5.5	V	Ripple < 100 mVpp
Input-H-Level Threshold	V _{ih}	2.0		V _{DD}	V	Input-H-Level threshold
Input-L-Level Threshold	V _{il}	0		0.8	V	Input-L-Level threshold

Electrical Characteristics Table (VDD = 4.5 to 5.5 V, TA = -40 to +115° C)

Electrical characteristics over recommended operating conditions. Typical values at 25° C

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Currents						
Total Current	I _{Total}	LED current @10 mA typ		94		mA
Digital Inputs						
Pull Up Current	I _{pu}	Room Temperature	-106	-60	-35	μA
Pull down Current	I _{pd}	Room Temperature	-108	-56	-31	μA
Digital Outputs						
Output-H-Level	V _{oh}	I _{oh} = 2 mA	V _{DD} - 0.5V		V _{DD}	V
Output-L-Level	V _{ol}	I _{ol} = -2mA	0		0.5	V
SSI Serial Interface						
SCL Clock Frequency (3wire SSI)	f _{clock}				10	MHz
SCL clock Frequency (2wire SSI)	f _{clock}				1.5	MHz
Duty Cycle f _{clock}	T _{clock, LH}	f _{clock} = 10 MHz	0.4		0.6	
Gray Code Monotony Error ⁽¹⁾		f _{clock} = 5 MHz, RPM = 100		1		Error step
SPI Serial Interface						
SPI_Clock	t _{clock}			100		kHZ

Electrical Characteristics Table (VDD = 4.5 to 5.5 V, TA = -40 to +115° C) (Continued)

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Units
Analog-Signal (single ended sine+/- Cosine+/-)						
Signal Frequency	f_{sin}, f_{cos}	With LED reg turns On		500		kHz
Output Voltage Amplitude ⁽²⁾				0.56		V
Output DC voltage ⁽²⁾			2.20	2.50	2.80	V
Incremental A/B (2048cpr)						
Cycle error		5.0 V @ Nominal	-8		+8	Deg
Phase error btw A/B		5.0 V @ Nominal	-15	5	+15	Deg
Duty error		5.0 V @ Nominal	-23	4	+28	Deg

Notes:

1. Code monotony error is dependent on customer installation and the bearing and shaft eccentricity being used.
2. Analog signal output is single ended +/- with 0.5 Vpp, after combine the single ended signal will get 1 Vpp differential output.

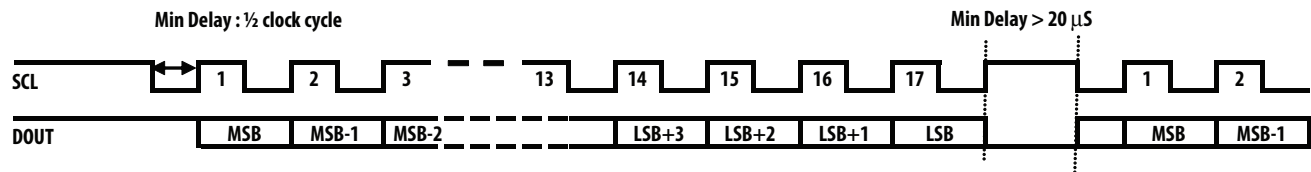


Figure 1a. 2-wire SSI Timing diagram (for single ended drive)

2 wire mode:

NSL pins will not be used. Connect the NSL+ to Ground before Power On and NSL- to high at +5V before Power On.

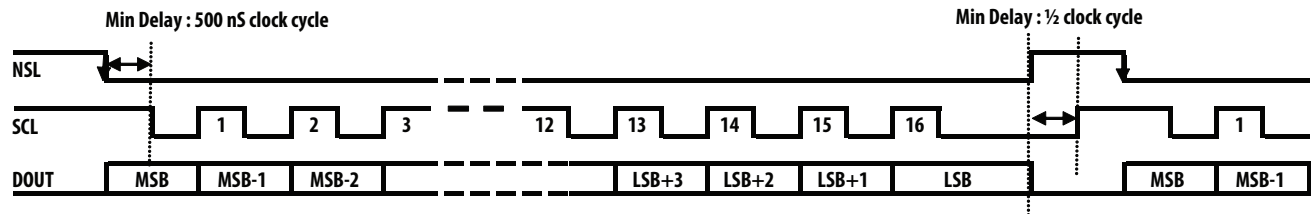


Figure 1b. 3-wire SSI Timing diagram (for single ended drive)

3 wire mode:

When NSL = 1 (act as chip enable) for the 3 wire mode, it means it is in load mode and is used to obtain the position of the code disc. When NSL = 0, it is in the shift mode of the internal registers and with the SCL clock pin, the register will be clocked with related frequency required.

Set NSL sequence correctly: NSL set "high" before Power On and when read data output then only pull NSL to ground. NSL to be triggered low before the SCL clock can reach the encoder to read out the positional data output.

Additional note – To avoid any potential power on sequence timing issue follow these instructions:

With the NSL tied high, trigger the nRST (pin 26) low (toggle the nReset pin) for about 1 us before switching back to high. "NSL must be held high until the release of the nReset". In a typical application, hold the NSL high about 1 us before the clock begins (or long enough to meet the minimum 500ns requirement).

Theory of Operation

1. The AEAT-9000 encoder consists of 13 differential absolute track signals. 12 tracks generated from code wheel and track number 13 is generating from the analogue sine of the incremental track.
2. 8 photo sensors are used for analog Sine+, Sine-, Cosine+, Cosine- signal generation with 90° phase shift. The analog signals are calibrated to correct the offset and gain via SPI interface. The offset and gain values will be preloaded into internal memory. After signal conditioning, the encoder performs on chip interpolation to generate an additional 4bit absolute output (D-1~D-4) and synchronizes with the 13 absolute track to make up a 17 bits absolute encoder. The analog signals are true differential signals with a frequency response of 500 kHz, enabling output position data to be read at high speed.
3. An additional sensor is used for radial alignment. Sensor Locate will output at LocTest pin and is enabled using SPI interface during alignment mode.
4. Besides that, the inner and outer tracks are used for tilt angle measurement, by generation of pulses via TiltOut pin. The TiltOut pulse width will be used to determine the tilt angle.
5. A Zero_RST pin is used to allow the encoder to set zero position at any position. The encoder stores this preset value into the internal memory and indicates the new position information with reference to the preset value every time data is read out. The Zero reset function is enabled when Zero_RST pin is pulled to ground.

Alignment Mode

Align the code discs to the read head by positioning the mid-point location of the code disc hub about 17.5 mm away from center point of the mounting hole as shown below. SPI will command to switch to alignment mode.

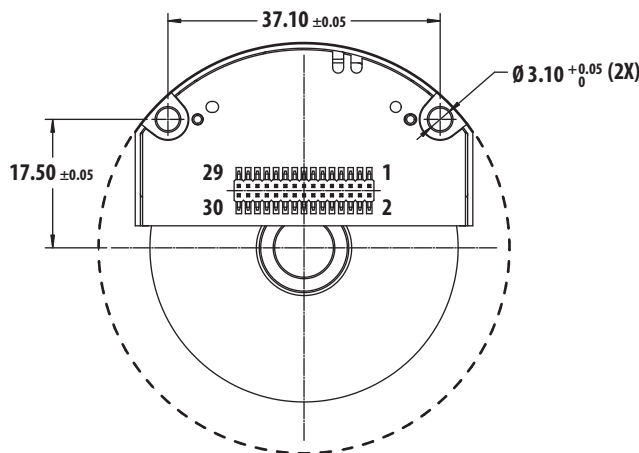


Figure 2. Alignment between read head and the codewheel.

1. Write address 0x11 with 1010 1011 to unlock the register.
2. Write address 0x10 with 0001 0001 to turn on alignment mode.

address	Command+add	Data
0x11	01+01 0001	1010 1011
0x10	01+01 0000	0001 0001

The D1 signal will be output to LocTest pin and at nominal location, the signal pattern is as shown in below figure 3 and 4. The amplitude of the signal will depend on the total stack-up TIR of the code wheel.

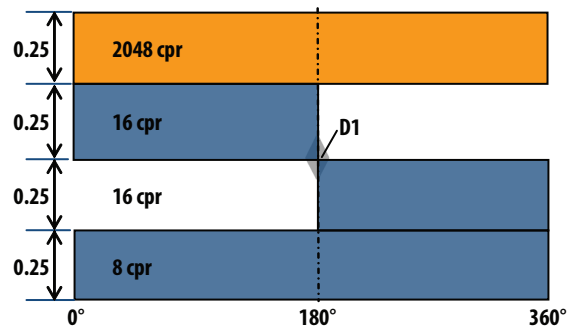


Figure 3. Code disk track 7 alignment to D1 photo detector

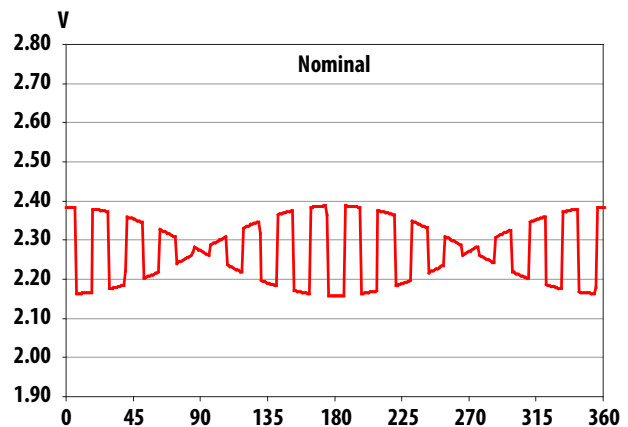


Figure 4. Output of D1 with code wheel eccentricity of 10 μm

D1 is used to align the code disk to the encoder chip in radial axes. For the sensor tilt alignment, the TiltOut signal is monitored. An output pulse is generated via TiltOut pin as shown below in Figure 5. At nominal position the t/T will be at the ratio of 0.0078 at any motor spinning speed.

After alignment is done, an SPI command is sent to set the same address (0x10) with 0000 0001 or a power cycle is performed to set back the register to the default value of 0000 0001.

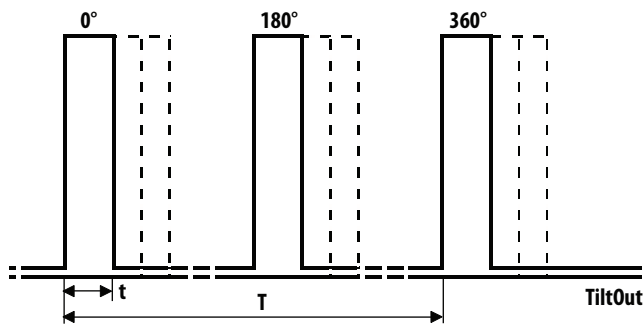


Figure 5. TiltOut signal in alignment mode.

LED regulation

The LED regulation control unit keeps the LED power perceived by the PDA constant regardless of temperature or aging effects. It also acts to stabilize the amplitudes of the Sine/Cosine signals.

If the power control exceeds the operating range the LERR pin will be pulled to logic High.

The LED power control is generated from the analog tracks, i.e. the Sine/Cosine photo sensors. At high RPM speeds, the LED power control will compensate for signal amplitudes attenuation, and it can drive up to 50 mA maximum current.

Sine/Cosine Signal Calibration

Due to amplifier mismatch and mechanical misalignment the signals do have gain and offset errors. Once the alignment is done, the encoder will need to be switched to calibration mode, which to correct the single-ended sine and cosine to 2.5 V offset and 1 Vpp amplitude. The signal calibration is done with LED regulation turned off.

The sine/cosine signal will driven out through an op-amp where the Vpp will be 0.5Vpp amplitude for a single ended sin/cosine with 2.5 V offset.

Calibration is done at Avago in factory prior to ship out, so user can skip this process.

Interpolator for Sine & Cosine Channels

The interpolator on the Sine/Cosine analog signal generates the digital signal of D-1 to D-4 by a flash A/D conversion; the interpolation value will be synchronized with the 13 digital tracks to generate the 17-bit absolute position value.

DOUT, SCL, NSL (3wire/2 wire SSI)

The absolute position is serially streamed out using SSI protocol. The most significant bit, MSB (D17) will always be sent first from the DOUT pin. The positional data can be inverted (i.e. count down instead of up) with MSBINV pulled to high. By default it will be low once powered on.

The NSL pin acts as the chip enable pin. NSL has to be triggered first to low before SCL clock can reach the encoder to read out the positional data. The maximum SCL clock frequency is up to 10 MHz.

Valid data of DOUT should be read when the SCL clock is low. Please refer to timing diagram on Figure 1.

In some application of point to point interface, 2 wire SSI is use which will eliminate the use of NSL pin. In this case NSL will need to pull to low all times. For 2 wire SSI, the SCL timing will be limited to about 1.5 MHz. The NSL+ pin have to connect to ground and NSL- connect to high voltage at 5V.

LERR pin is a general error pin as a feedback to user on some errors such as temperature sensor exceeding operating limit, LED ray is low, and this is an indication when light intensity is at a critical stage affecting the performance of the encoder. It is caused either by contamination of the code disc or LED degradation.

Incremental A/B output

Besides the absolute position read out, AEAT-9000 also comes with 2 channel incremental output with 2048CPR. These A/B channel is generated from differential Sin/Cosine. The frequency response of the A/B will be based on the differential Sin/Cosine response with a max of 500 kHz without much degradation on the Vpp amplitude.

SPI Interface (SPI_S0, SPI_SI, SPI_CLK)

SPI is the interface that is used to configure the internal register settings to turn on alignment mode and calibration mode.

During alignment mode, Loctest signal and Tiltout will provide an output to perform alignment.

During calibration mode, the SPI interface is used to perform Sine/Cosine gain and offset calibration. It is also used to program the EEPROM once the calibration has been done.

To access the SPI register, write the data 1110 1011 to address 0x1b to enable changes on the register setting. This is needed every time the device is power on.

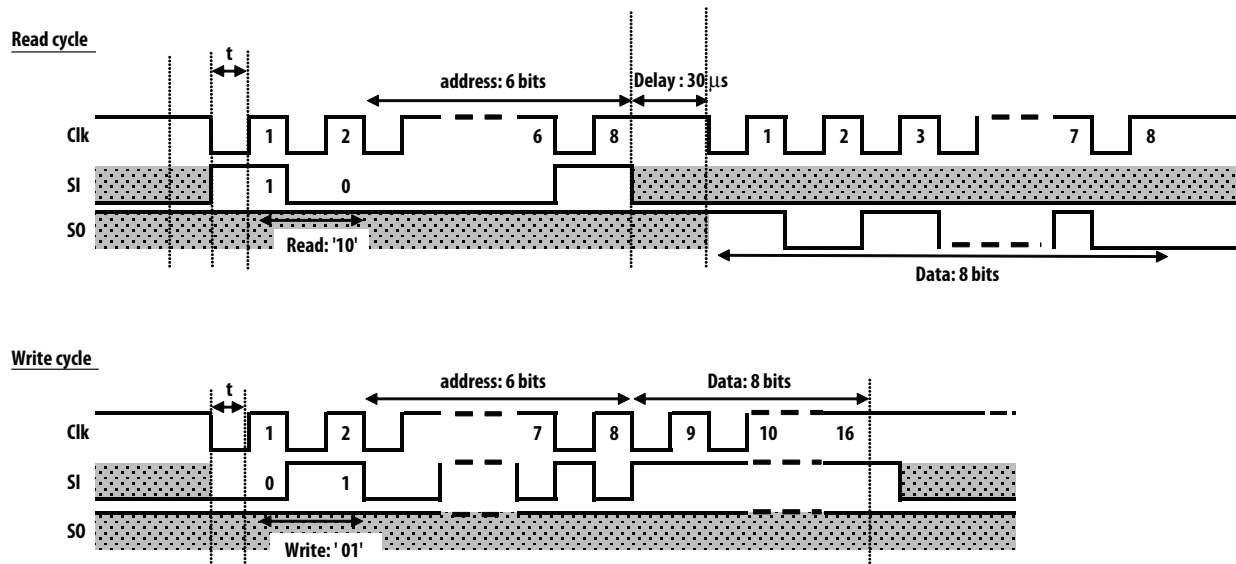
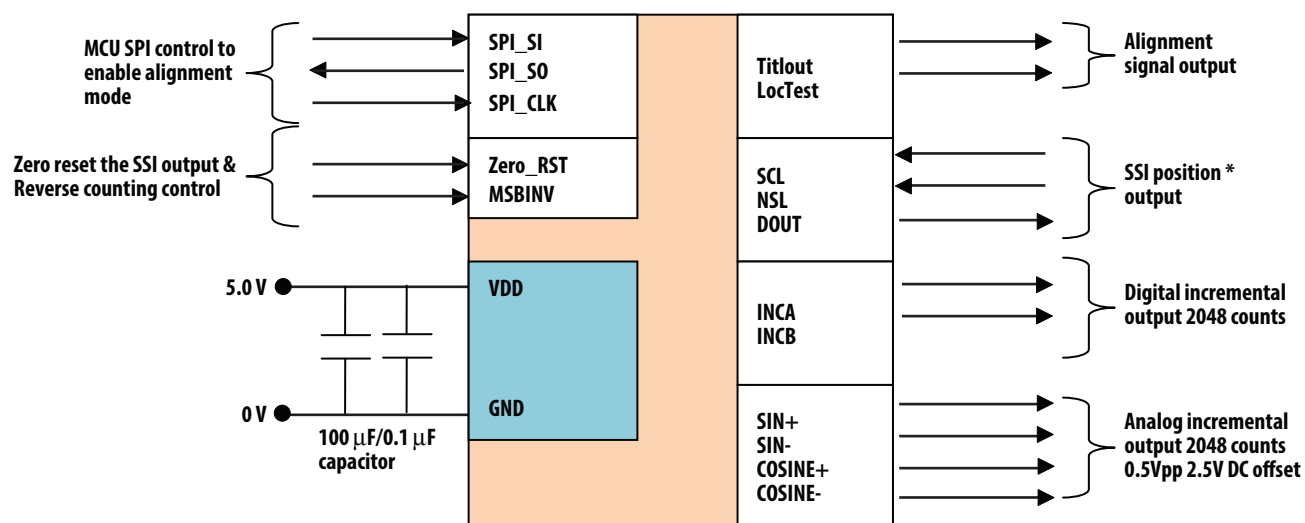


Figure 6. SPI timing diagram for read and write



* SCL, NSL and DOUT pins : reference to differential pins.
Refer to page 7 pin out descriptions.

Figure 7. AEAT9000 interface Block diagram

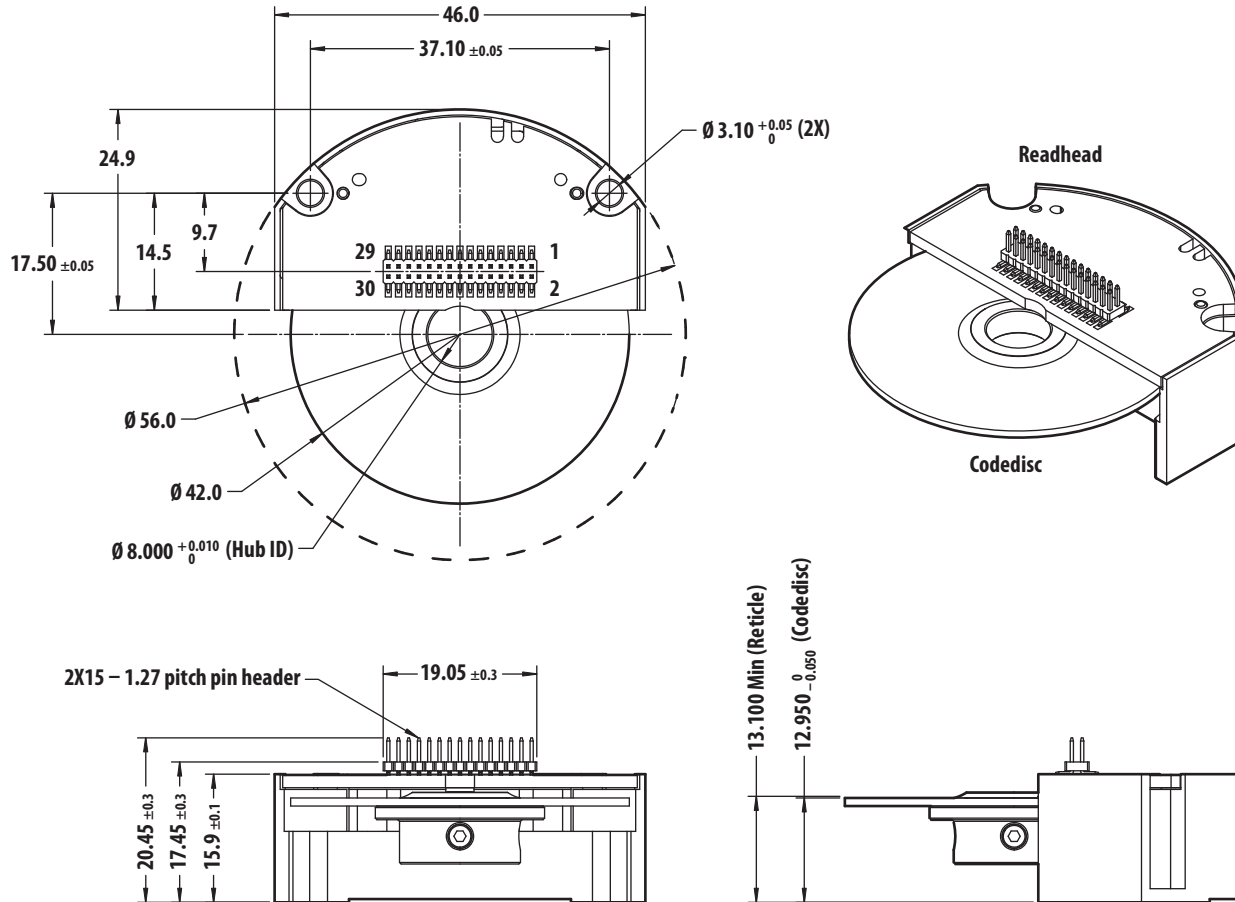
Pin out Descriptions (Serial SSI 2/3wire option)

No.	Pin Name	Description	Function	Notes
1	COSINE+	Analog Output	Diff Cosine+ analog output	CMOS, analog out
2	COSINE-	Analog Output	Diff Cosine- analog output	CMOS, analog out
3	SINE+	Analog Output	Diff SINE+ analog output	CMOS, analog out
4	SINE-	Analog Output	Diff SINE- analog output	CMOS, analog out
5	TiltOut	Digital Output	Tilt alignment output	CMOS
6	GND	Ground for supply voltage	Connect ground	
7	LocTest	Analog Output	Alignment locate signal	CMOS, analog out
8	GND	Ground for Supply Voltage	Connect ground	
9	NC		Not use	
10	MSBINV	Digital Input	Inverted counting	CMOS, internal pd
11	SPI_CLK	Digital Input	SPI clock input	CMOS, internal pu
12	Zero_RST	Digital Input	Pull down to zero the absolute position	CMOS, internal pu
13	SPI_SI	Digital Input	SPI data input	CMOS, internal pd
14	NSL+	Digital Input	NSL + Differential (for 3wire SSI only) ^[1]	
15	SPI_SO	Digital Output	SPI data output	CMOS
16	NSL-	Digital Input	NSL- Differential (for 3wire SSI only) ^[1]	
17	GND	Ground for Supply Voltage	Connect ground	
18	GND	Ground for Supply Voltage	Connect ground	
19	INCB	Digital Output	B Digital output	CMOS
20	DOUT-	Digital Output	DOUT- Differential DOUT (for 3wire/2wire SSI)	
21	INCA	Digital Output	A Digital output	CMOS
22	DOUT+	Digital Output	DOUT+ Differential DOUT (for 3wire/2wire SSI)	
23	DIN-	Digital Input	DIN- Differential (for cascading use only)	
24	LERR	Digital Output	ERROR pin, error(=1)/no error(=0)	CMOS
25	DIN+	Digital Input	DIN+ Differential (for cascading use only)	
26	nRST	Digital Output	Chip Reset	CMOS, internal pu
27	VDD	Supply Voltage	+5 V Supply	
28	SCL+	Digital Input	SCL+ Differential clock (for 3wire/2wire SSI)	
29	VDD	Supply Voltage	+5 V Supply	
30	SCL-	Digital Input	SCL- Differential clock (for 3wire/2wire SSI)	

Note:

1. For 2 wire SSI application, connect the NSL+ pin to ground before power on and NSL- to high at 5V before power on.

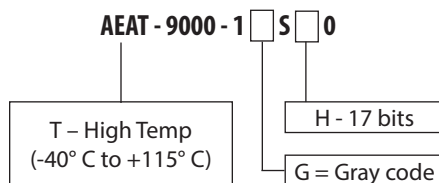
Mechanical Dimensions



Notes:

1. All dimensions are in millimeter.
2. Tolerance: X.X ± 0.10 mm.
3. Code disk and readhead mounting tolerances for radial, tangential and gap are as below
 - Radial : $\pm 50 \mu\text{m}$ (inclusive shaft eccentricity)
 - Tangential : $\pm 100 \mu\text{m}$ (inclusive shaft eccentricity)
 - Gap : 150 to 300 μm
4. Recommended mounting screw:-
 - Socket Head cap screw, M2.5 (ISO 4762)
 - Flat Washer, M2.5 (ISO 7092)

Ordering Information



HEDS-8949 - Alignment kit for AEAT-9000-1GSH0

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

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