

Synchronous Rectified MOSFET Driver with Pre-Biased Load Startup Capability

The ISL6608 is a high frequency, MOSFET driver optimized to drive two N-Channel power MOSFETs in a synchronous-rectified buck converter topology. This driver combined with an Intersil HIP63xx or ISL65xx Multi-Phase Buck PWM controller forms a complete single-stage core-voltage regulator solution with high efficiency performance at high switching frequency for advanced microprocessors.

The IC is biased by a single low voltage supply (5V) and minimizes gate drive losses due to MOSFET gate charge at high switching frequency applications. Each driver is capable of driving a 3000pF load with a low propagation delay and less than 10ns transition time. This product implements bootstrapping on the upper gate with an internal bootstrap Schottky diode, reducing implementation cost, complexity, and allowing the use of higher performance, cost effective N-Channel MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

The ISL6608 features 4A sink current for the lower gate driver, which is capable of holding the lower MOSFET gate during the Phase node rising edge to prevent shoot-through power loss caused by the high dv/dt of the Phase node.

The ISL6608 also features a Three-State PWM input which, working together with Intersil multi-phase PWM controllers, will prevent a negative transient on the output voltage when the output is shut down. This feature eliminates the Schottky diode that is usually seen in a microprocessor power system for protecting the microprocessor from reversed output voltage events.

A diode emulation feature is integrated in the ISL6608 to enhance converter efficiency at light load conditions. Diode emulation also prevents a negative transient when starting up with a pre-biased voltage on the output. When diode emulation is enabled, the driver allows discontinuous conduction mode by detecting when the inductor current reaches zero and subsequently turns off the low side MOSFET, which prevents the output from sinking current and producing a negative transient on a pre-biased output (see Figures 6 and 7 on page 7).

Features

- Dual MOSFET Drives for Synchronous Rectified Bridge
- Adaptive Shoot-Through Protection
- 0.5Ω On-Resistance and 4A Sink Current Capability
- Supports High Switching Frequency up to 2MHz
 - Fast Output Rise/Fall Time and Low Propagation Delay
- Three-State PWM Input for Power Stage Shutdown
- Internal Bootstrap Schottky Diode
- Low Bias Supply Current (5V, 80μA)
- Diode Emulation for Enhanced Light Load Efficiency and Pre-Biased Startup Applications
- VCC POR (Power-On-Reset) Feature Integrated
- Low Three-State Shutdown Holdoff Time (Typically 160ns)
- Pin-to-Pin Compatible with ISL6605
- QFN Package:
 - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
 - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-free Available as an Option

Applications

- Core Voltage Supplies for FPGAs and PowerPC Microprocessors
- Point-Of-Load Modules with Pre-Biased Start-Up Requirements
- High Frequency and High Current DC-DC Converters

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices"

Ordering Information

PART NUMBER	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6608CB	0 to 70	8 Ld SOIC	M8.15
ISL6608CB-T	8 Ld SOIC Tape and Reel		
ISL6608CR	0 to 70	8 Ld 3x3 QFN	L8.3x3
ISL6608CR-T	8 Ld 3x3 QFN Tape and Reel		
ISL6608CBZ (Note)	0 to 70	8 Ld SOIC (Lead-Free)	M8.15
ISL6608CBZ-T	8 Ld SOIC Tape and Reel (Lead-Free)		
ISL6608CRZ (Note)	0 to 70	8 Ld 3x3 QFN (Lead-Free)	L8.3x3
ISL6608CRZ-T	8 Ld 3x3 QFN Tape and Reel (Lead-Free)		
ISL6608IB	-40 to 85	8 Ld SOIC	M8.15
ISL6608IB-T	8 Ld SOIC Tape and Reel		
ISL6608IR	-40 to 85	8 Ld 3x3 QFN	L8.3x3

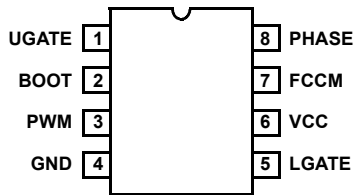
Ordering Information (Continued)

PART NUMBER	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6608IR-T	8 Ld 3x3 QFN Tape and Reel		
ISL6608IBZ (Note)	-40 to 85	8 Ld SOIC (Lead-Free)	M8.15
ISL6608IBZ-T (Note)	8 Ld SOIC Tape and Reel (Lead-Free)		
ISL6608IRZ (Note)	-40 to 85	8 Ld 3x3 QFN (Lead-Free)	L8.3x3
ISL6608IRZ-T (Note)	8 Ld 3x3 QFN Tape and Reel (Lead-Free)		

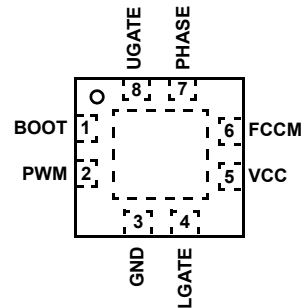
NOTE: Intersil Lead-Free products employ special lead-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and lead-free soldering operations. Intersil Lead-Free products are MSL classified at lead-free peak reflow temperatures that meet or exceed the lead-free requirements of IPC/JEDEC J Std-020B.

Pinouts

ISL6608CB (SOIC)
TOP VIEW



ISL6608CR (3X3 QFN)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage (VCC)	-0.3V to 7V
BOOT Voltage (V _{BOOT})	-0.3V to 22V
Phase Voltage (V _{PHASE}) (Note 1)	V _{BOOT} - 7V to V _{BOOT} + 0.3V
Input Voltage (V _{DE} , V _{PWM})	-0.3V to VCC + 0.3V
UGATE	V _{PHASE} - 0.3V to V _{BOOT} + 0.3V
LGATE	-0.3V to VCC + 0.3V
Ambient Temperature Range	-40°C to 125°C

Thermal Information

Thermal Resistance (Typical, Notes 2, 3, 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 2)	110	n/a
QFN Package (Notes 3, 4)	82	16
Maximum Junction Temperature (Plastic Package)	150°C	
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s)	300°C	
(SOIC - Lead Tips Only)		

Recommended Operating Conditions

Ambient Temperature Range	-40°C to 85°C
Maximum Operating Junction Temperature	125°C
Supply Voltage, VCC	5V $\pm$ 10%

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The Phase Voltage is capable of withstanding -7V when the BOOT pin is at GND.
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.
5. Guaranteed by design, not tested.

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Bias Supply Current	I _{VCC}	PWM Pin Floating, V _{VCC} = 5V	-	80	-	μA
POWER-ON RESET (POR)						
VCC Rising			-	3.40	4.00	V
VCC Falling		T _A = 0°C to 70°C	2.40	2.90	-	V
		T _A = -40°C to 85°C	2.175	2.90	-	V
Hysteresis			-	500	-	mV
BOOTSTRAP DIODE						
Forward Voltage	V _F	V _{VCC} = 5V, I _F = 2mA	0.40	0.52	0.62	V
PWM INPUT						
Input Current	I _{PWM}	V _{PWM} = 5V	-	250	-	μA
		V _{PWM} = 0V	-	-250	-	μA
PWM Three-State Rising Threshold		V _{VCC} = 5V	0.80	1.00	1.20	V
PWM Three-State Falling Threshold		V _{VCC} = 5V, T _A = 0°C to 70°C	3.40	3.65	3.90	V
		V _{VCC} = 5V, T _A = -40°C to 85°C	3.05	3.65	4.10	V
		V _{VCC} = 5.5V	-	-	4.55	V
Three-State Shutdown Holdoff Time	t _{TSSHD}	V _{VCC} = 5V, T _A = 0°C to 70°C	100	160	250	ns
		V _{VCC} = 5V, T _A = -40°C to 85°C	80	160	250	ns
FORCED CONTINUOUS CONDUCTION MODE (FCCM) INPUT						
FCCM LOW Threshold			0.50	-	-	V
FCCM HIGH Threshold		T _A = 0°C to 70°C	-	-	2.00	V
		T _A = -40°C to 85°C	-	-	2.05	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING TIME						
UGATE Rise Time	t_{RU}	$V_{VCC} = 5V, 3nF$ Load	-	8.0	-	ns
LGATE Rise Time	t_{RL}	$V_{VCC} = 5V, 3nF$ Load	-	8.0	-	ns
UGATE Fall Time	t_{FU}	$V_{VCC} = 5V, 3nF$ Load	-	8.0	-	ns
LGATE Fall Time	t_{FL}	$V_{VCC} = 5V, 3nF$ Load	-	4.0	-	ns
UGATE Turn-Off Propagation Delay	t_{PDLU}	$V_{VCC} = 5V$, Outputs Unloaded	-	35	-	ns
LGATE Turn-Off Propagation Delay	t_{PDLL}	$V_{VCC} = 5V$, Outputs Unloaded	-	35	-	ns
UGATE Turn-On Propagation Delay	t_{PDHU}	$V_{VCC} = 5V$, Outputs Unloaded	-	20	-	ns
LGATE Turn-On Propagation Delay	t_{PDHL}	$V_{VCC} = 5V$, Outputs Unloaded	-	20	-	ns
UG/LG Three-state Propagation Delay	t_{PTS}	$V_{VCC} = 5V$, Outputs Unloaded	-	35	-	ns
Minimum LG On TIME in DCM (Note 5)	t_{LGMIN}		-	400	-	ns
OUTPUT						
Upper Drive Source Resistance	R_U	250mA Source Current	-	1	2.5	Ω
Upper Driver Source Current (Note 5)	I_U	$V_{UGATE-PHASE} = 2.5V$	-	2.00	-	A
Upper Drive Sink Resistance	R_U	250mA Sink Current	-	1	2.5	Ω
Upper Driver Sink Current (Note 5)	I_U	$V_{UGATE-PHASE} = 2.5V$	-	2.00	-	A
Lower Drive Source Resistance	R_L	250mA Source Current	-	1	2.5	Ω
Lower Driver Source Current (Note 5)	I_L	$V_{LGATE} = 2.5V$	-	2.00	-	A
Lower Drive Sink Resistance	R_L	250mA Sink Current	-	0.5	1.0	Ω
Lower Driver Sink Current (Note 5)	I_L	$V_{LGATE} = 2.5V$	-	4.00	-	A

Functional Pin Description**UGATE (Pin 1 for SOIC-8, Pin 8 for QFN)**

The UGATE pin is the upper gate drive output. Connect to the gate of high-side power N-Channel MOSFET.

BOOT (Pin 2 for SOIC-8, Pin 1 for QFN)

BOOT is the floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Bootstrap Diode and Capacitor section under DESCRIPTION for guidance in choosing the appropriate capacitor value.

PWM (Pin 3 for SOIC-8, Pin 2 for QFN)

The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the three-state PWM Input section under DESCRIPTION for further details. Connect this pin to the PWM output of the controller.

GND (Pin 4 for SOIC-8, Pin 3 for QFN)

GND is the ground pin for the IC.

LGATE (Pin 5 for SOIC-8, Pin 4 for QFN)

LGATE is the lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.

VCC (Pin 6 for SOIC-8, Pin 5 for QFN)

Connect the VCC pin to a +5V bias supply. Place a high quality bypass capacitor from this pin to GND.

FCCM (Pin 7 for SOIC-8, Pin 6 for QFN)

The FCCM pin enables or disables Diode Emulation. When FCCM is LOW, diode emulation is allowed. Otherwise, continuous conduction mode is forced (FCCM= Forced Continuous Conduction Mode). See the Diode Emulation section under DESCRIPTION for more detail.

PHASE (Pin 8 for SOIC-8, Pin 7 for QFN)

Connect the PHASE pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate driver.

Thermal Pad (in QFN only)

The PCB "thermal land" design for this exposed die pad should include thermal vias that drop down and connect to one or more buried copper plane(s). This combination of vias for vertical heat escape and buried planes for heat spreading allows the QFN to achieve its full thermal potential. This pad should be grounded. Refer to TB389 for design guidelines.

Description

Theory of Operation

Designed for speed, the ISL6608 dual MOSFET driver controls both high-side and low-side N-Channel FETs from one externally provided PWM signal.

A rising edge on PWM initiates the turn-off of the lower MOSFET (see Figure 1, Timing Diagram). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall times [t_{FL}] are provided in the Electrical Specifications section. Adaptive shoot-through circuitry monitors the LGATE voltage. When LGATE has fallen below 1V, UGATE is allowed to turn ON. This prevents both the lower and upper MOSFETs from conducting simultaneously, or shoot-through.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short

propagation delay [t_{PDLU}] is encountered before the upper gate begins to fall [t_{FU}]. The upper MOSFET gate-to-source voltage is monitored, and the lower gate is allowed to rise after the upper MOSFET gate-to-source voltage drops below 1V. The lower gate then rises [t_{RL}], turning on the lower MOSFET.

This driver is optimized for converters with large step down compared to the upper MOSFET because the lower MOSFET conducts for a much longer time in a switching period. The lower gate driver is therefore sized much larger to meet this application requirement.

The 0.5Ω on-resistance and 4A sink current capability enable the lower gate driver to absorb the current injected to the lower gate through the drain-to-gate capacitor of the lower MOSFET and prevent a shoot through caused by the high dv/dt of the phase node.

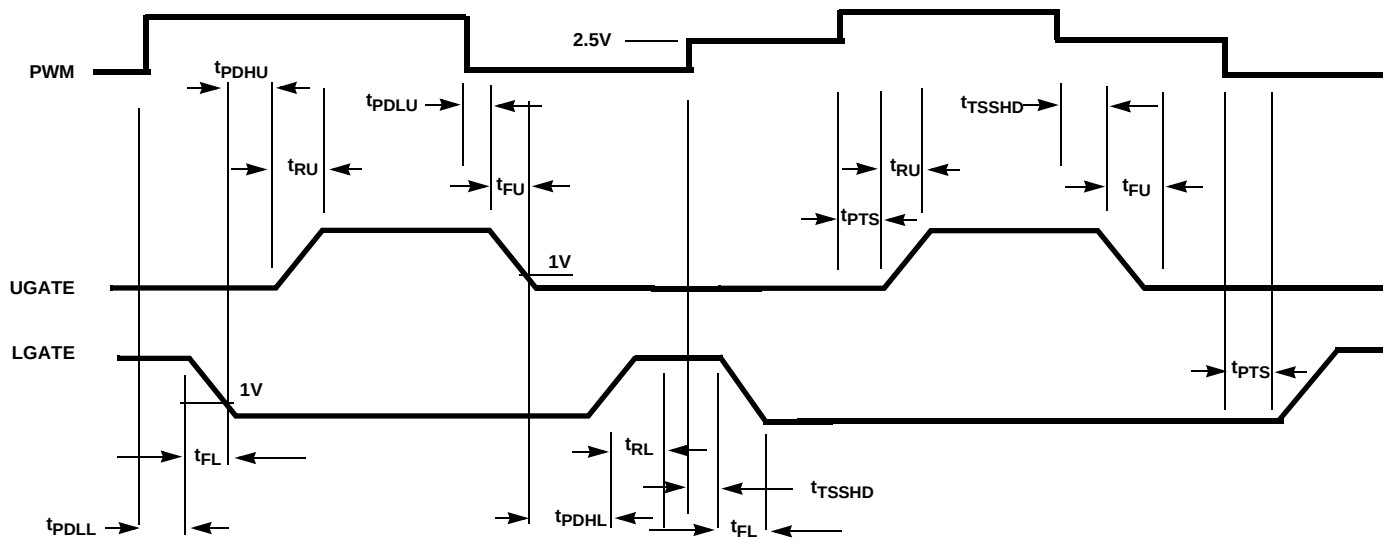


FIGURE 1. TIMING DIAGRAM

Typical Performance Waveforms

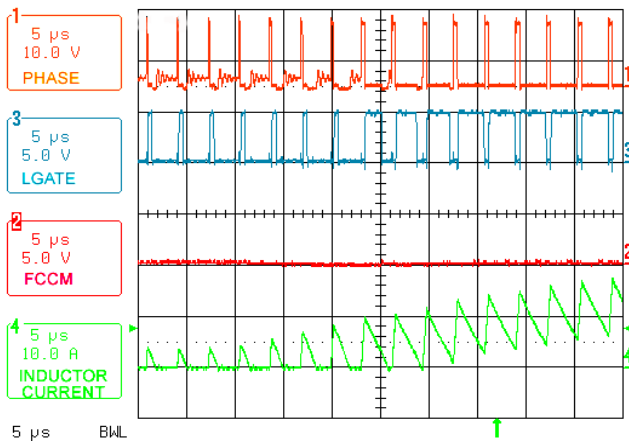


FIGURE 2. LOAD TRANSIENT (0 to 30A, 3-PHASE)

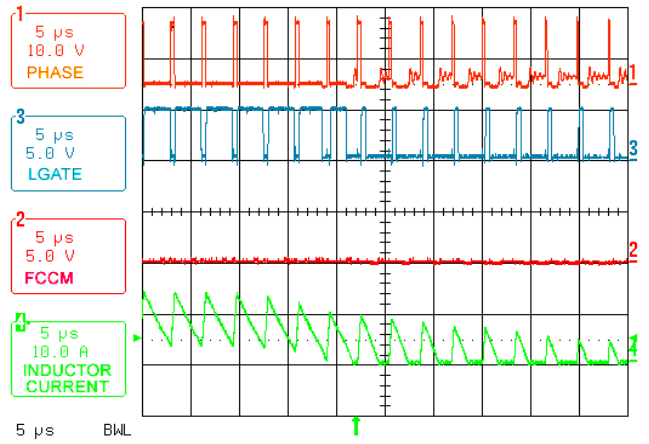


FIGURE 3. LOAD TRANSIENT (30 to 0A, 3-PHASE)

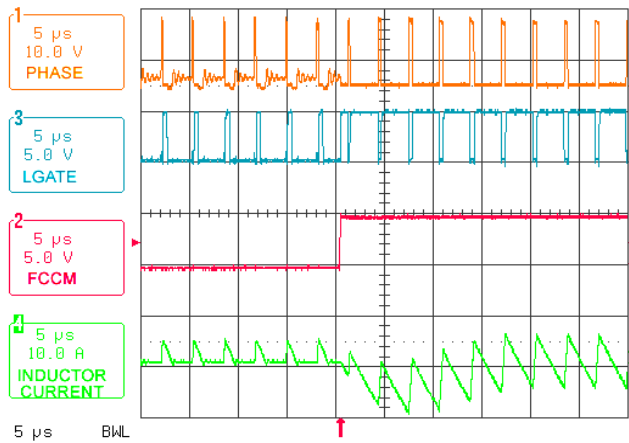


FIGURE 4. DCM TO CCM TRANSITION AT NO LOAD

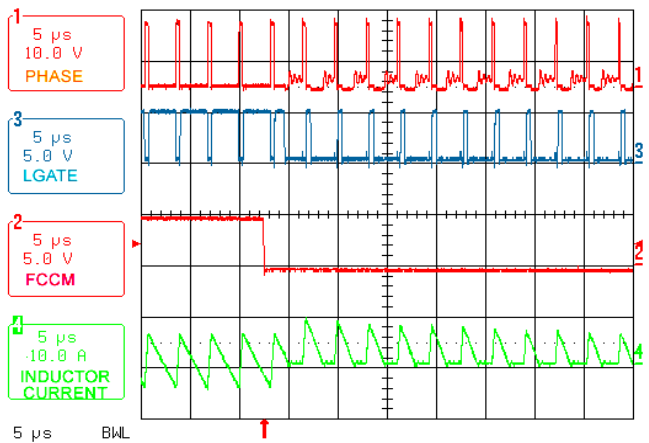


FIGURE 5. CCM TO DCM TRANSITION AT NO LOAD

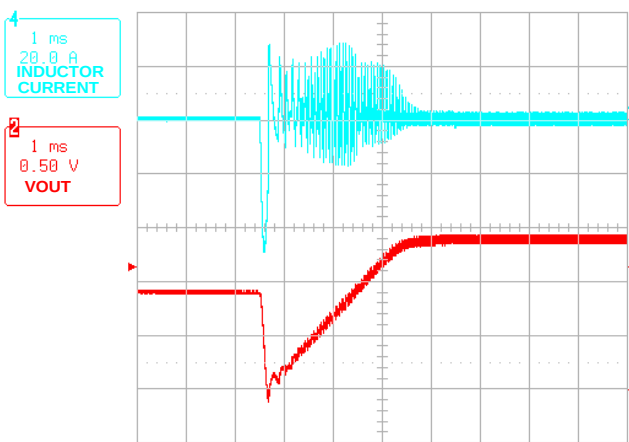


FIGURE 6. PRE-BIASED STARTUP IN CCM MODE (FCCM = HI)

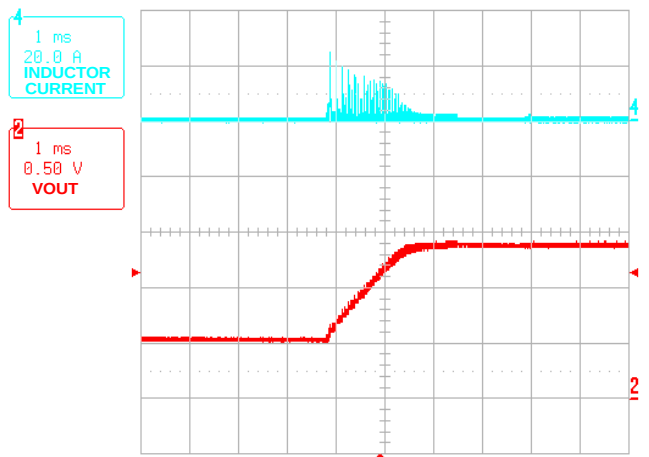


FIGURE 7. PRE-BIASED STARTUP IN DCM MODE (FCCM = LO)

Diode Emulation

Diode emulation allows for higher converter efficiency under light-load situations. With diode emulation active (FCCM = LO), the ISL6608 will detect the zero current crossing of the output inductor and turn off LGATE. This ensures that discontinuous conduction mode (DCM) is achieved. This prevents the low side MOSFET from sinking current, and no negative spike at the output is generated during pre-biased startup (See Figure 7 on page 7). The LGATE has a minimum ON time of 400ns in DCM mode. Diode emulation is asynchronous to the PWM signal. Therefore, the ISL6608 responds to the FCCM input immediately after it changes state. Refer to Figures 2 to 7 on page 7 for details.

Intersil does not recommend Diode Emulation used with the $r_{DS(ON)}$ of the freewheeling MOSFET current sensing topology. The turn-OFF of the low side MOSFET forces the forward current going through the body diode of the MOSFET. If the current sampling circuit of the controller is activated during the body diode conduction, a diode voltage drop, instead of a much smaller MOSFET's $r_{DS(ON)}$ voltage drop, is sampled. This will falsely trigger the over current protection function of the controller.

The ISL6608 works with DCR, upper MOSFET, or power resistor current sensing topologies to start up from pre-biased load with no problem.

Three-State PWM Input

A unique feature of the ISL6608 and other Intersil drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time (typically 160ns), the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the ELECTRICAL SPECIFICATIONS determine when the lower and upper gates are enabled.

Adaptive Shoot-Through Protection

Both drivers incorporate adaptive shoot-through protection to prevent upper and lower MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to turn on.

During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a 1V threshold, at which time the UGATE is released to rise. Adaptive shoot-through circuitry monitors the upper MOSFET gate-to-source voltage during UGATE turn-off. Once the upper MOSFET gate-to-source voltage has dropped below a threshold of 1V, the LGATE is allowed to rise.

Internal Bootstrap Diode

This driver features an internal bootstrap Schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap capacitor must have a maximum voltage rating above $V_{CC} + 5V$ and its capacitance value can be chosen from the following equation:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}}$$

$$Q_{GATE} = \frac{Q_{G1} \cdot V_{CC}}{V_{GS1}} \cdot N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT} term is defined as the allowable droop in the rail of the upper drive. The previous relationship is illustrated in Figure 8.

As an example, suppose an upper MOSFET has a gate charge, Q_{GATE} , of 65nC at 5V and also assume the droop in the drive voltage over a PWM cycle is 200mV. One will find that a bootstrap capacitance of at least 0.125 μ F is required. The next larger standard value capacitance is 0.15 μ F. A good quality ceramic capacitor is recommended.

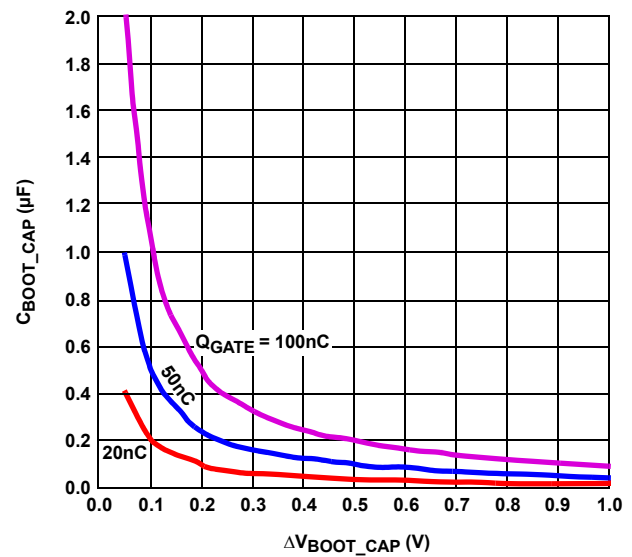


FIGURE 8. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Power Dissipation

Package power dissipation is mainly a function of the switching frequency and total gate charge of the selected MOSFETs. Calculating the power dissipation in the driver for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the SO-8 package is approximately 800mW. When designing the driver into an application, it is recommended that the following calculation be performed to ensure safe operation at the desired frequency for the selected MOSFETs. The power dissipated by the driver is approximated as below and plotted as in Figure 9.

$$P = f_{sw}(1.5V_UQ_U + V_LQ_L) + I_{DDQ}V_{CC}$$

where f_{sw} is the switching frequency of the PWM signal. V_U and V_L represent the upper and lower gate rail voltage. Q_U and Q_L are the upper and lower gate charge determined by MOSFET selection and any external capacitance added to the gate pins. The $I_{DDQ}V_{CC}$ product is the quiescent power of the driver and is typically negligible.

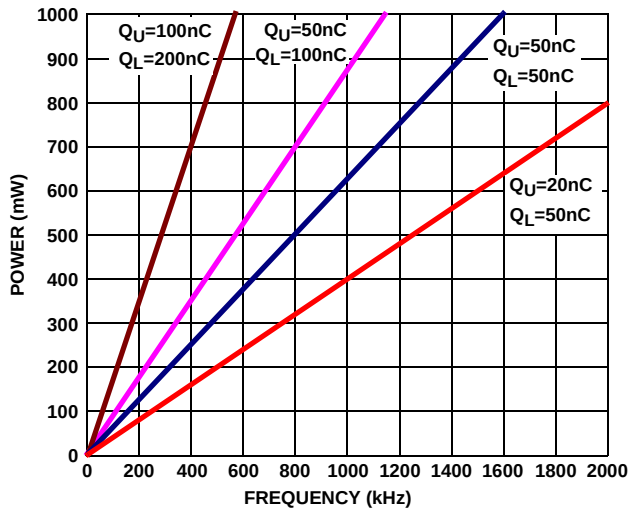


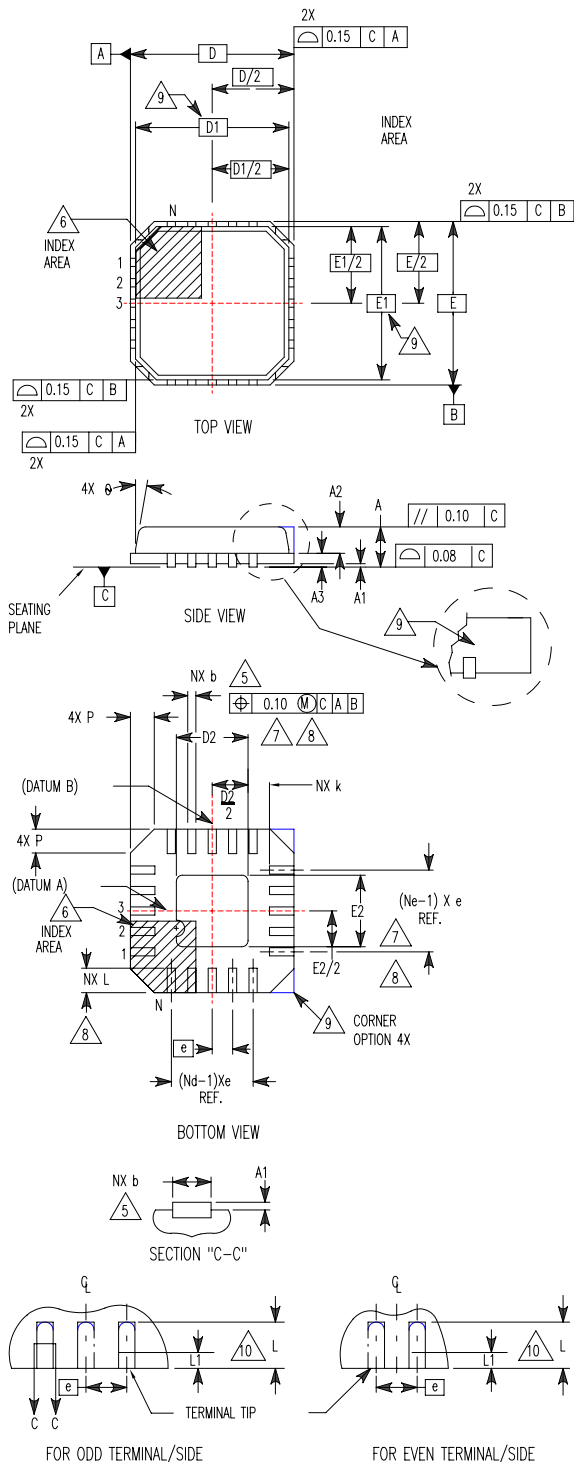
FIGURE 9. POWER DISSIPATION vs FREQUENCY

Layout Consideration

For heat spreading, place copper underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried copper plane(s) with thermal vias. This combination of vias for vertical heat escape, extended copper plane, and buried planes for heat spreading allows the IC to achieve its full thermal potential.

Place each channel power component as close to each other as possible to reduce PCB copper losses and PCB parasitics: shortest distance between DRAINS of upper FETs and SOURCES of lower FETs; shortest distance between DRAINS of lower FETs and the power ground. Thus, smaller amplitudes of positive and negative ringing are on the switching edges of the PHASE node. However, some space in between power components is required for good airflow. The gate traces from the drivers to the FETs should be kept short and wide to reduce the inductance of the traces and promote clean drive signals.

Quad Flat No-Lead Plastic Package (QFN) **Micro Lead Frame Plastic Package (MLFP)**



L8.3x3

8 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
(COMPLIANT TO JEDEC MO-220VEEC ISSUE C)

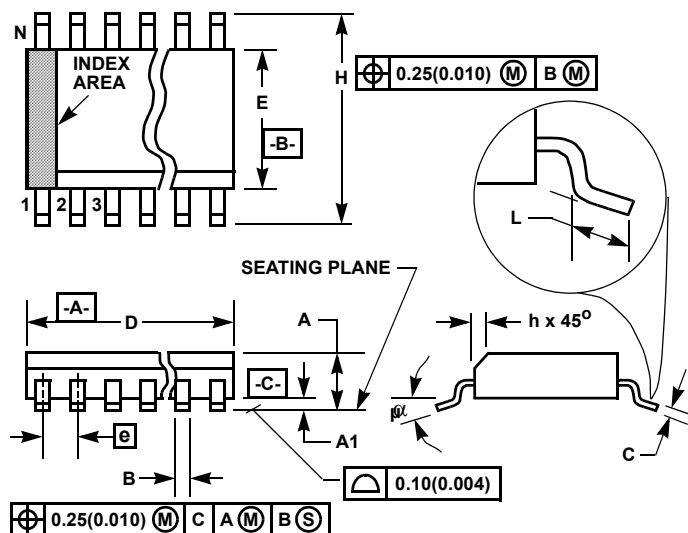
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3	0.20 REF			9
b	0.23	0.28	0.38	5, 8
D	3.00 BSC			-
D1	2.75 BSC			9
D2	0.25	1.10	1.25	7, 8
E	3.00 BSC			-
E1	2.75 BSC			9
E2	0.25	1.10	1.25	7, 8
e	0.65 BSC			-
k	0.25		-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N	8			2
Nd	2			3
Ne	2			3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C) 8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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