Ordering number : EN5198

Discontinued

SANYO Semiconductors
DATA SHEET

Monolithic Digital IC

LB1814M — 3.5-inch Magneto-Optical Disk Spindle Motor Driver

Overview

LB1814M is a driver IC that was developed to drive 3.5-inch magneto-optical disk spindle motors. It integrates all the necessary functions, including the speed control circuit, drive circuit and other functions on a single chip. Using a current linear drive technique for minimal motor drive noise and PLL speed control circuit with excellent jitter characteristics, this IC offers selectivity in the methods for FG input and reference clock input, enabling it to support a wide range of applications. With a view to interfacing with equipment controllers (e.g., of microcontrollers), it comes with a variety of outputs that can be used to monitor the motor operation.

Functions and Features

- 5 V and 12 V power supplies use supported
- 3-phase full-wave current linear drive
- Crystal oscillator circuit
- PLL speed control circuit
- Hall FG/pattern FG switching circuit
- Internal clock/external clock switching circuit, clock frequency division switching circuit
- Brake circuit (reverse torque brake)
- Phase lock detection output, stop detection output, rotation monitor output
- Current limiter circuit (OCL), low power supply voltage protection circuit (LVSD), thermal protection circuit (TSD)
- Power-saving function
- Built-in FG amplifier, integrating amplifier
- Built-in spark killer diode

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		14.5	V
Maximum output current	I_O max	T<0.1s	1.0	A
HG pin applied voltage	V_{HG} max		14.5	V
LD pin applied voltage	V_{LD} max		14.5	V
SD pin applied voltage	V_{SD} max		14.5	V
Allowable power dissipation	Pd max	Independent IC	0.95	W
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		4.2 to 13.5	V
HG pin applied voltage	V_{HG}		0 to 13.5	V
LD pin applied voltage	V_{LD}		0 to 13.5	V
SD pin applied voltage	V_{SD}		0 to 13.5	V
HG pin output current	I_{HG}		0 to 3	mA
LD pin output current	I_{LD}		0 to 3	mA
SD pin output current	I_{SD}		0 to 3	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	$I_{CC}1$	Start mode (FC pin = GND)		21	30	mA
	$I_{CC}2$	Power save mode		180	250	μA
Output saturation voltage						
SOURCE(1)	$V_{SAT}1$-1	I_O=0.5A, R_f=0Ω		0.90	1.25	V
SOURCE(2)	$V_{SAT}1$-2	I_O=0.7A, R_f=0Ω		0.95	1.35	V
SINK(1)	$V_{SAT}2$-1	I_O=0.5A, R_f=0Ω		0.20	0.45	V
SINK(2)	$V_{SAT}2$-2	I_O=0.7A, R_f=0Ω		0.30	0.55	V
SOURCE+SINK	V_{SAT}	I_O=0.5A, R_f=0Ω		1.1	1.3	V
Output leakage current	I_{OLEAK}	V_{CC}=13.5V			100	μA
Hall input block						
Input bias current	$I_{B(HA)}$				10	μA
Differential input range	V_{HIN}	Sine wave input	40			mVp-p
Common-mode input range	V_{ICM}		2.0		V_{CC}	V
Input offset voltage	V_{IOH}	Design target value	-10		+10	mV
Hall amplifier gain	G_{HO}	Logic input, design target value		7		
Hysteresis width	V_{HHIS}	Logic input, design target value		100		mV
Low power supply voltage protection circuit block						
Operating voltage	V_{SDL}		3.6	3.8	4.0	V
Resetting voltage	V_{SDH}		3.8	4.0	4.2	V
Hysteresis width	ΔV_{SD}		0.1	0.2	0.3	V
Thermal protection circuit block						
Thermal shutdown operating temperature	TSD	Design target value (junction temperature)	150	180		°C
Hysteresis width	ΔTSD	Design target value (junction temperature)		40		°C
Current limit operation						
Limiter 1	$V_{RF}1$		0.21	0.23	0.25	V
Limiter 2	$V_{RF}2$	In reverse rotation torque mode	0.16	0.18	0.20	V

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
FG amplifier block						
Input offset voltage	V_{IO}(FG)		-10		+10	mV
Input bias current	I_B(FG)		-1		+1	µA
DC bias level	V_B(FG)		1.8	1.9	2.0	V
Output high level voltage	V_{OH}(FG)	I_{FGI}= -100µA, No external load	2.3	2.7	3.1	V
Output low level voltage	V_{OL}(FG)	I_{FGI}=100µA, No external load	0.8	1.2	1.6	V
FG Schmitt block						
Input hysteresis (high to low)	V_{SHL}			0		mV
Input hysteresis (low to high)	V_{SLH}			140		mV
Hysteresis width	V_{FGL}		90		200	mV
Input operating level	V_{FGSIL}		400			mVp-p
Error amplifier block						
Input offset voltage	V_{IO}(ER)	Design target value	-10		+10	mV
Input bias current	I_B(ER)		-1		+1	µA
DC bias level	V_B(ER)		-5%	1/2V_{REG}	+5%	V
Output high level voltage	V_{OH}(ER)1	No external load	V_{REG}-1.0			V
	V_{OH}(ER)2	I_{LOAD}=2mA	V_{REG}-1.5			V
Output low level voltage	V_{OL}(ER)	No external load			1.0	V
Phase comparator output						
Output high level voltage	V_{PDH}	No external load	V_{REG}-0.2			V
Output low level voltage	V_{PDL}	No external load		0.1	0.2	V
Output source current	I_{PD}^+	V_{PD}=V_{REG} / 2			-0.4	mA
Output sink current	I_{PD}^-	V_{PD}=V_{REG} / 2	2.5			mA
Lock detector output						
Output saturation voltage	V_{LDSAT}	I_{LD}=1.5mA		0.1	0.4	V
Output leakage current	I_{LDLEAK}	V_{LD}=13.5V			10	µA
Rotation monitor output						
Output saturation voltage	V_{HGSAT}	I_{HG}=1.5mA		0.1	0.4	V
Output leakage current	I_{HGLEAK}	V_{HG}=13.5V			10	µA
Stop sensor output						
Output saturation voltage	V_{SDSAT}	I_{SD}=1.5mA		0.1	0.4	V
Output leakage current	I_{SDLEAK}	V_{SD}=13.5V			10	µA
Drive block						
Dead zone width	V_{DZ}		50	195	300	mV
Output idling voltage	V_{ID}				6	mV
Forward gain	G_{DF}^+		0.4	0.5	0.6	
Reverse gain	G_{DF}^-		-0.6	-0.5	-0.4	
Forward limiter voltage	V_L^+	R_f=10Ω, V_{EI}=0V	0.21	0.23	0.25	V
Reverse limiter voltage	V_L^-	R_f=10Ω, V_{EI}=V_{REG}	0.16	0.18	0.20	V
Reference signal block						
Crystal oscillator frequency	f_{OSC}	In crystal oscillator mode	1		10	MHz
Hall bias pin						
Sink current	I_{HB}		10			mA
Analog filter block						
Delay time 1	T_{FD}1	Rising	5.0	9.0	13.5	µs
Delay time 2	T_{FD}2	Falling	4.5	8.5	13.0	µs
S/B pin						
High level input voltage	V_{SBH}		V_{CC}-1.5		V_{CC}	V
Low level input voltage	V_{SBL}		0		V_{CC}-3.5	V
Input open voltage	V_{SBO}		V_{CC}-0.2	V_{CC}		V
Low level input current	I_{SBL}	V_{SB}=0V	-200	-140	-80	µA

Continued on next page.

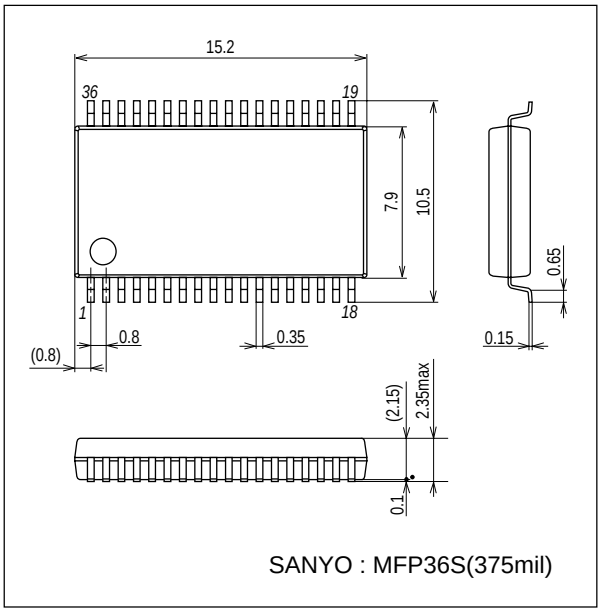
Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
N pin						
High level input voltage	V_{NH}		4.0		V_{CC}	V
Medium level input voltage	V_{NM}		2.0		3.0	V
Low level input voltage	V_{NL}		0		1.0	V
Input open voltage	V_{NO}		2.1	2.5	2.9	V
High level input current	I_{NH}	$V_N=V_{CC}$	70	115	200	μA
Low level input current	I_{NL}	V_N=0V	-70	-50	-30	μA
3.8V constant voltage output block						
Output voltage	V_{REG}		3.6	3.8	4.0	V
Output current	I_{REG}				5	mA
Voltage variation	$\Delta V_{REG}1$	V_{CC}=4.2V to 13.5V		2	200	mV
Load variation	$\Delta V_{REG}2$	I_{REG}=0 to 3mA		15	200	mV
Temperature coefficient	$\Delta V_{REG}3$	Design target value		0		mV/°C
BC oscillator circuit						
Oscillation frequency	f(BC)	C=1000pF	1.4	2.0	2.6	kHz
Output high level voltage	V_{OH}(BC)		2.2	2.5	2.8	V
Output low level voltage	V_{OL}(BC)		0.5	0.7	0.9	V
Amplitude	V(BC)		1.5	1.8	2.1	V
Charge current	$I_{CHG}1$		-10.0	-6.5	-4.5	μA
Discharge current	$I_{CHG}2$		5.5	8.0	11.5	μA

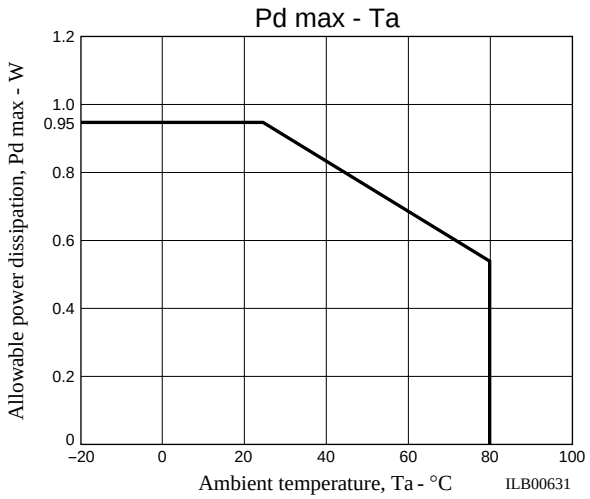
Package Dimensions

unit : mm (typ)

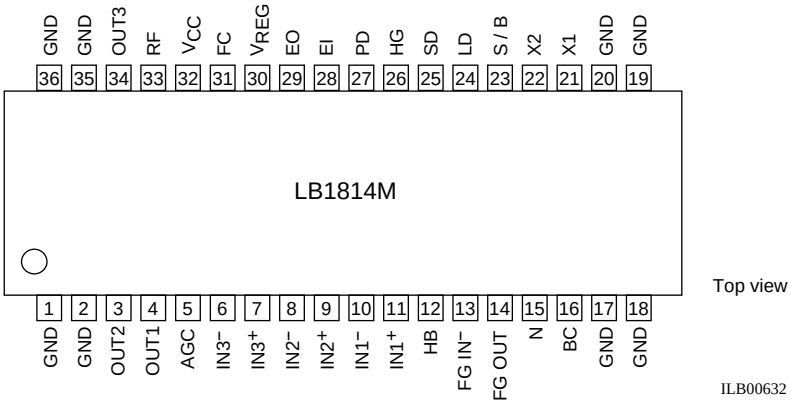
3204B



SANYO : MFP36S(375mil)



Pin Assignment



Clock Divisor Switching

FG mode	Pin N	Divisor
Hall FG mode	L	24576 (6×8×512)
	H	20480 (5×8×512)
Pattern FG mode	L	3072 (6×1×512)
	H	2560 (5×1×512)
×	M	EXT. CLK

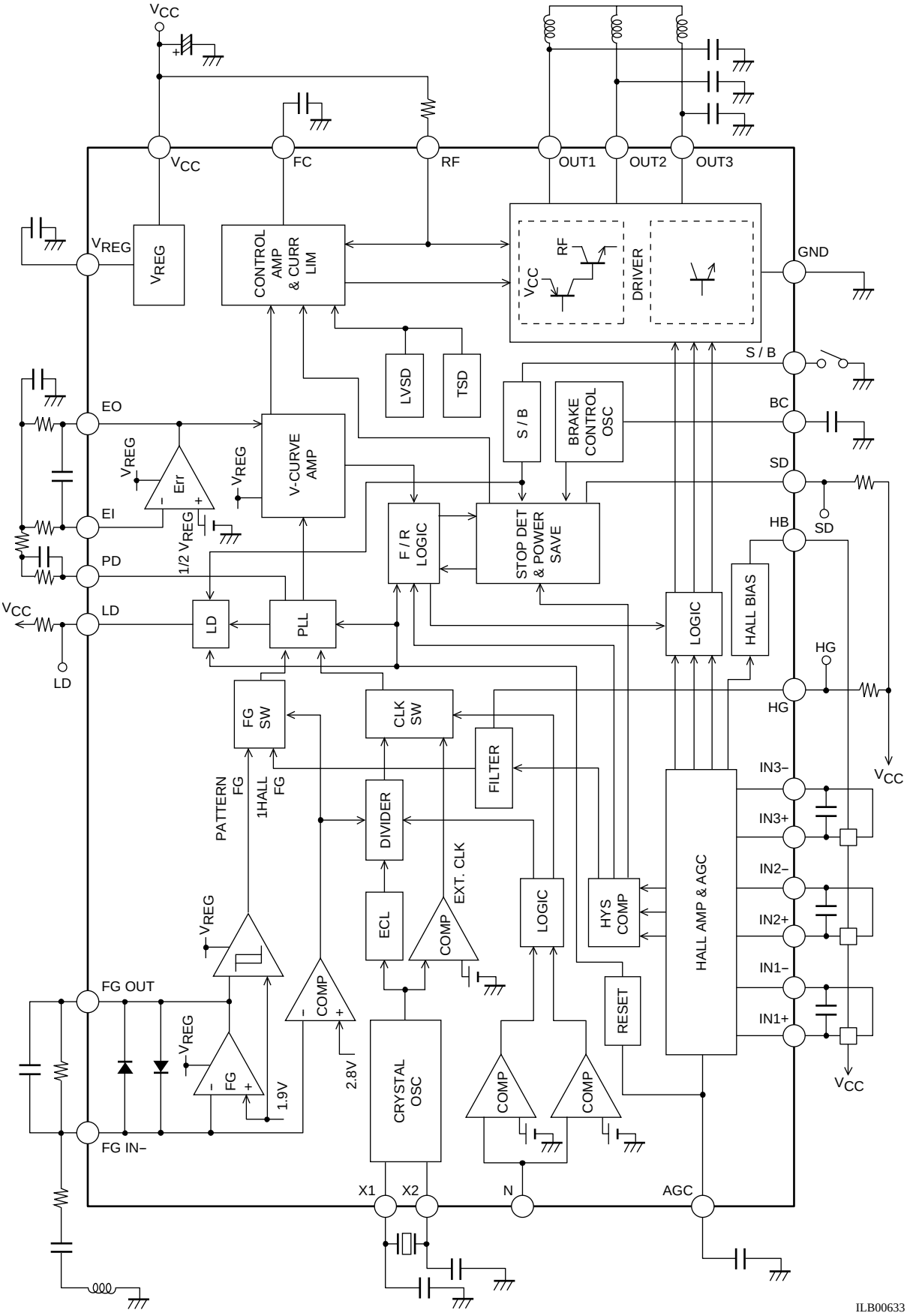
FG servo frequency = Crystal oscillation frequency/Divisor

Three-phase Logic Truth Value Table (Rotation direction: One direction only)

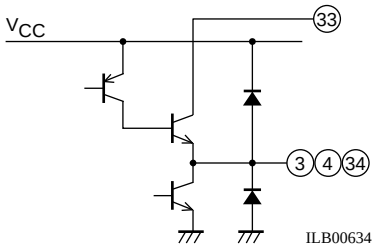
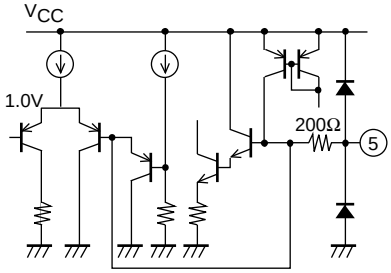
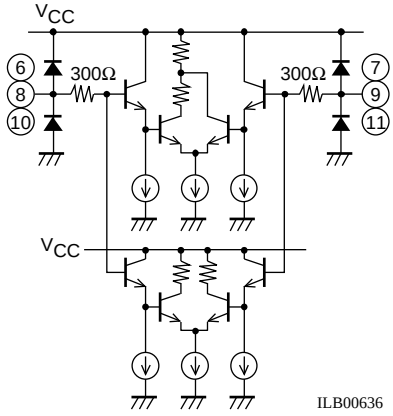
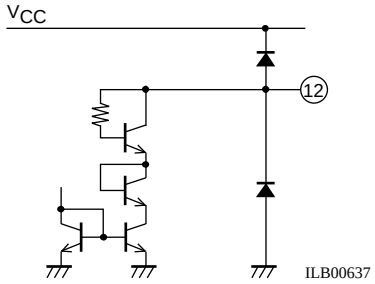
IN1	IN2	IN3	OUT1	OUT2	OUT3
H	L	H	L	H	M
H	L	L	L	M	H
H	H	L	M	L	H
L	H	L	H	L	M
L	H	H	H	M	L
L	L	H	M	H	L

Discontinued

Block Diagram

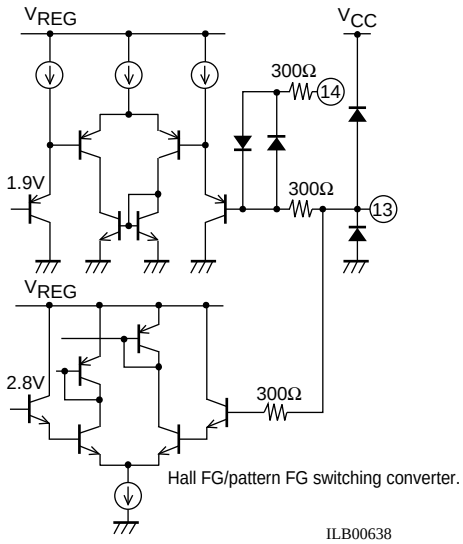
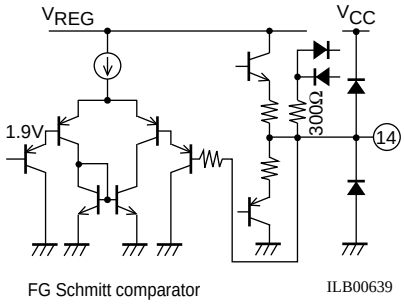
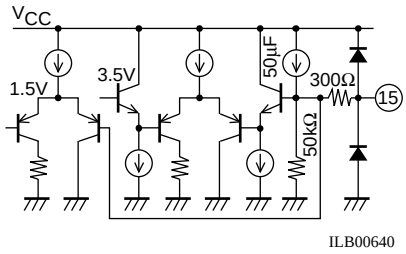
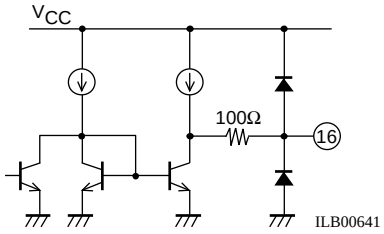
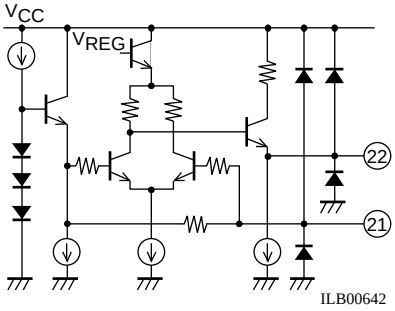


Pin Functions

Pin No	Symbol	Pin Voltage	Description	Equivalent Circuit
1, 2 17, 18 19, 20 35, 36	GND		Ground	
3 4 34	OUT2 OUT1 OUT3		OUT2 output OUT1 output OUT3 output	 ILB00634
33	RF		Output current detection. Connect a low resistance resistor (R_f) between this pin and V_{CC}. The forward rotation mode output current (I_{OUT}) is limited according to the equation $I_{OUT}=V_{RF}1/R_f$ (current limit operation).	
5	AGC		AGC amplifier frequency characteristics correction. Also serves as the initial reset pin. Connect a capacitor between this pin and ground. The AGC circuit operates in such a way that the Hall element output amplitude is kept constant (approx. 40mVp-p) by controlling the Hall element bias current (HB pin sink current). The IC enters and stays in the initial reset state after the S/B pin is set to the start mode till the AGC pin voltage goes up to 1.0V.	 Comparator for initial reset ILB00635
6 7 8 9 10 11	$IN3^-$ $IN3^+$ $IN2^-$ $IN2^+$ $IN1^-$ $IN1^+$	min 2.0V max V_{CC}	• IN1 Hall input High when $IN1^+ > IN1^-$ Low when $IN1^+ < IN1^-$ • IN2 Hall input High when $IN2^+ > IN2^-$ Low when $IN2^+ < IN2^-$ • IN3 Hall input High when $IN3^+ > IN3^-$ Low when $IN3^+ < IN3^-$	 ILB00636
12	HB		Hall bias. Held off in power save mode and Hall bias is cut off.	 ILB00637

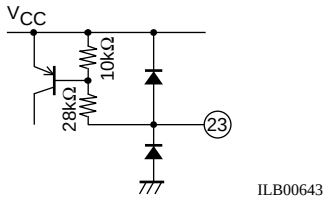
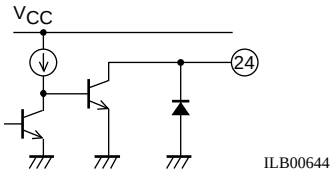
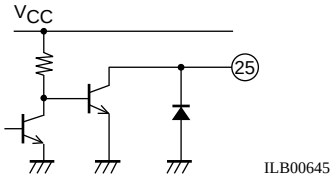
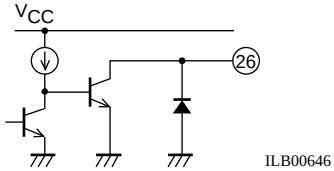
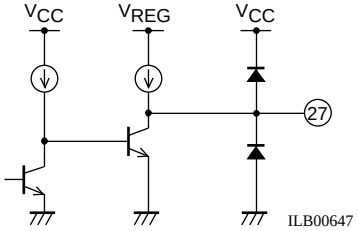
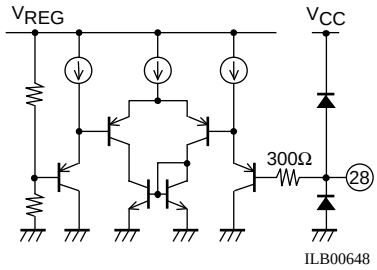
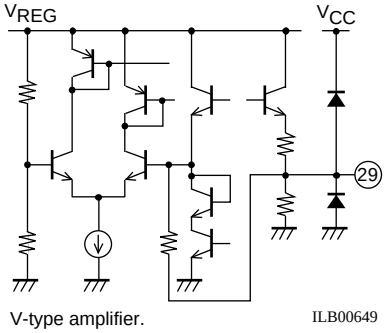
Continued on next page.

Continued from preceding page.

Pin No	Symbol	Pin Voltage	Description	Equivalent Circuit
13	FG_{IN}-		FG amplifier input. Also serves as the Hall FG/pattern FG switching pin. When in Fall FG mode, connect this pin to the V_{REG} pin.	
14	FG_{OUT}		FG amplifier output	
15	N	min 0.0V max V_{CC}	Divisor switching. Low: 0.0V to 1.0V. Medium: 2.0V to 3.0V. High: 4.0V to V_{CC}. "M" is selected when this pin is held open.	
16	BC		Brake control. Connect a capacitor between this pin and ground. Stopping characteristics of a motor is controlled by adjusting the capacitance.	
21 22	X1 X2		Crystal oscillator. These pins are used to generate the reference clock.	

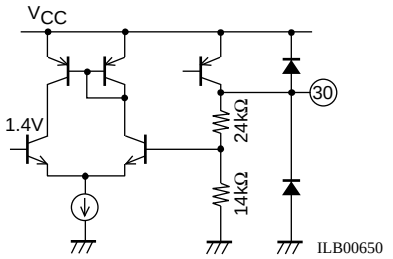
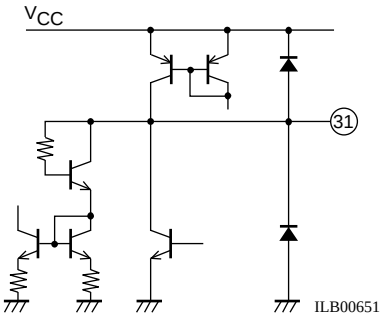
Continued on next page.

Continued from preceding page.

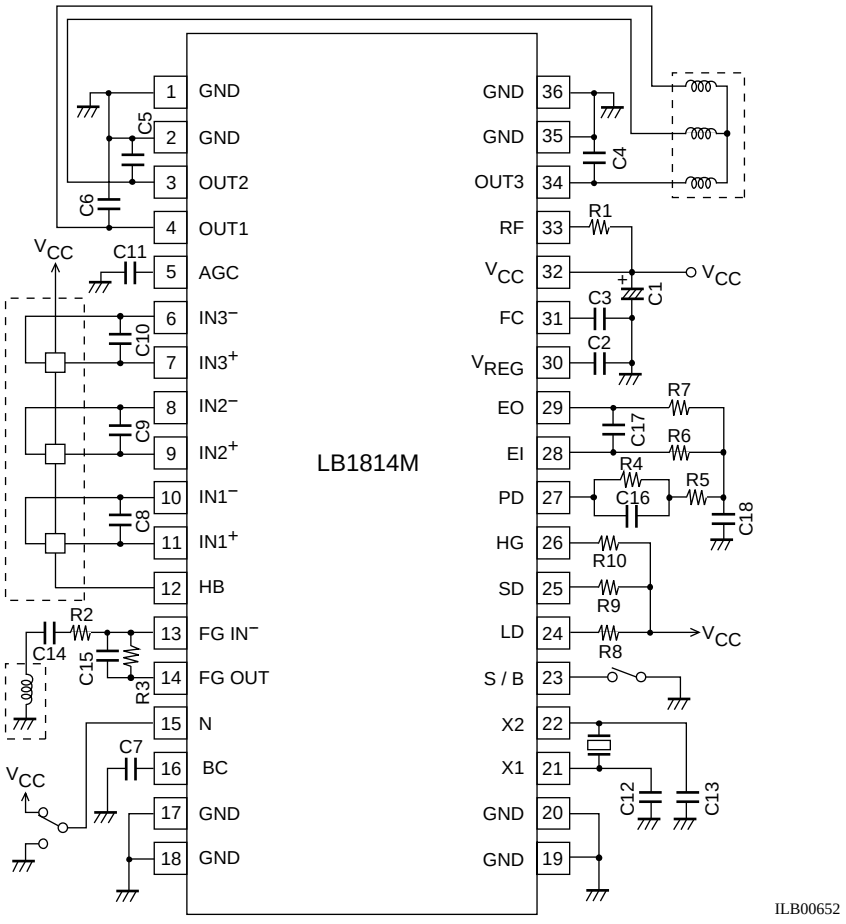
Pin No	Symbol	Pin Voltage	Description	Equivalent Circuit
23	S / B	min 0V max V_{CC}	Start/brake. Low: Start. High or open: Brake.	
24	LD		Phase lock detector output. On when the PLL phase is locked. This pin is an open collector output.	
25	SD		Stop detector output. On when the motor is stopped by the brake. This pin is an open collector output. Power save mode when this pin is on.	
26	HG		Rotation monitor output. Pulse output of the Hall input IN1. This pin is an open collector output.	
27	PD		Phase comparator output. PLL phase comparator output.	
28	EI		Error amplifier input	
29	EO		Error amplifier output	

Continued on next page.

Continued from preceding page.

Pin No	Symbol	Pin Voltage	Description	Equivalent Circuit
30	V_{REG}		Stabilized power supply output. Stabilizes the internal power supply. Connect a capacitor between this pin and ground.	
31	FC		Control amplifier frequency correction. Connect a capacitor between this pin and ground to prevent oscillation in the closed loop of the current control system.	
32	V_{CC}		Power supply	

Sample Application Circuit



External Components and Description

Components	Function	Description
C1	Power stabilization	Selects a value at which voltage fluctuations, due to motor driving current, are stabilized.
C2	Internal circuit power stabilization	Stabilizes voltage fluctuations in the 3.8V regulator output.
C3	Control amplifier frequency characteristics correction	Stops oscillation in the closed loop of the current control system.
R1	Current limiting	Limits output current according to the equation $I_{OUT}=V_{RF}1/R1$.
C4, C5, C6		Suppresses output oscillation.
C7	Brake control	Controls motor stop characteristics by adjusting the capacitance of this capacitor.
C8, C9, C10		Improves noise immunity of the Hall signal.
C11	AGC amplifier frequency characteristics correction. Initial reset pulse generation.	Smoothes out ripples. Generates an initialization reset to the IC's internal logic.
C12, C13	External crystal oscillator components	
R2, R3, C14, C15	FG amplifier gain and frequency characteristics setting	
R4, R5, R6, R7, C16, C17, C18	Servo constant	
R8, R9, R10	Pull-up resistors	

LB1814M Functional Description and External Components

1. Speed control circuit

This IC adopts a PLL speed control technique and provides stable motor operation with high precision and low jitter. This PLL circuit compares the phase at the falling edge of the reference clock signal and falling edge of the FG pulse, and outputs the phase error. The FG servo frequency is determined by the following formula, so the motor speed must be determined by the number of FG pulses and crystal oscillator frequency.

$$f_{FG}\text{ (servo)} = \text{Crystal oscillator frequency/Clock divisor}$$

2. Three-phase full-wave current linear drive

This IC adopts a three-phase full-wave current linear drive to hold motor noise to an absolute minimum.
It suppresses motor noise by smoothing the output current waveform. Since oscillation may occur in the output block depending on the motor used, the capacitors C4, C5 and C6 (of approx. 0.1μF) are connected between the OUT pins and ground.

3. Current limiting circuit

The current limiting circuit limits the current (i.e., the peak current) to the level determined by the formula $I_{OUT}=V_{RF}1/R1$. In the reverse torque mode (braking), the current is limited to the level determined by the formula $I_{OUT}=V_{RF}2/R1$. A scheme in which the output drive current is limited is adopted for limiting operation. This necessitates the phase compensation capacitor C3 (of approx. 0.1μF) connected between the FC pin and ground.

4. FG amplifier

The gain of the FG amplifier is determined by R2 and R3. G = R3/R2 defines the DC gain. C14 and C15 determine the frequency characteristics of the FG amplifier (R2 and C14 make up a high-pass filter and R3 and C15 a low-pass filter).
Since a Schmitt comparator follows the FG amplifier, it is necessary to determine the values of R2, R3 and C14, C15 so that the FG amplifier output is always 400mVp-p or higher. (It is desirable for the FG amplifier output to be set up to be between 1 and 3Vp-p during steady state rotation.) If the noise immunity level poses problems in noise evaluation, connect a capacitor of between 1000pF to 0.1μF between FGOUT pin and ground.
The FGIN- pin also serves to switch the Hall FG mode and pattern FG mode. When the Hall FG mode is selected, the pin must be connected to the VREG pin.

5. External capacitors

(1) C1 and C2

C1 is required for V_{CC} stabilization and C2 for constant-voltage power supply stabilization. A constant-voltage power supply is also used within the IC chip circuits. It is stabilized by a capacitor (C2 with a capacitance of approx 0.1μF). Select a capacitance for C1 at which the voltage fluctuations by the motor drive current are stabilized. Noise has an adverse effect on both the V_{CC} and constant-voltage power supplies so adequate stabilization measures need to be provided. C1 and C2 must be connected near the V_{CC} pin and V_{REG} pin of the IC and connected to the ground pin with a trace as short as possible.

(2) C7

The capacitance value of C7 serves to adjust the stop characteristics of the motor in the brake mode. To have the motor switched from the decelerated state to a full stop state smoothly when brake is on, it is necessary to select its capacitance value that is appropriate for the motor in use (approx. 0.001 to 0.01μF). If a slight reverse rotation tends to occur after the motor decelerates and almost halts, increase the capacitance value of C7. On the other hand, if a slight forward rotation tends to occur, decrease the capacitance value of C7.

This IC switches between the forward and reverse torques when the output is off whereby preventing through current from occurring when switching the torque. C7 is also used to determine the output off period. The output off time which occurs when switching between the forward and reverse torque modes is one period of BC oscillation. Since the switching between the forward and reverse torque modes occurs when shifting the motor into the constant speed mode or brake mode, too great a capacitance will increase the output off time, which adversely affects on the performance of shifting the motor into the constant speed mode or brake mode.

(3) C8, C9 and C10

The Hall signals are used for the speed control, braking, forward/reverse logic circuits, etc. If noise immunity poses problems in noise evaluation, connect a capacitor of approx. 0.01μF between the Hall input pins IN+ and IN- .

(4) C11

C11 is a the AGC (Automatic Gain Control) pin smoothing capacitor. The AGC pin outputs the three-phase Hall signal envelope, and is smoothed with a capacitor of approx. 0.1μF since it has ripple.

The capacitor C11 at the AGC pin is also used to generate the initial reset pulse to the IC internal logic circuit. The initial reset pulse is generated when the S/B pin is placed in the start mode and is held on till the AGC pin voltage (capacitor voltage) goes up to 1.0V. There are times when the LD pin is momentarily turned on at start time if the initial reset is not active. The capacitor C11 at the AGC pin is discharged in the power save mode (motor stopped and the SD pin is held on). In a mode in which the start and brake cycles alternate, if a restart is attempted after a brake is applied and before the motor stops (power save mode established), no initial reset pulse will be generated because the C11 is then not discharged. In such a case, the LD pin is likely to turn on momentarily at start time. In an application in which the start and brake cycles need to alternate, it is necessary to allow a power save time (discharging time of 10 ms or longer with a 0.1 μF capacitor).

6. Pins X1 and X2

A crystal oscillator and a capacitor are normally connected to the X1 and X2 pins of this IC. The authorization of the oscillator manufacturer must be obtained when selecting the oscillator and capacitor to be connected externally to avoid the problem.

When using an external input signal (CLK) without using a crystal oscillator element, connect a 13kΩ resistor to the X1 pin in series. In this case, the X2 pin must be held open.

f_{CLK}=10 MHz (max.)
Input signal level range
Low-level voltage: 0.0V to 0.8V
High-level voltage: 2.5V to 5.0V

When using the external clock mode (setting the N pin to the Medium-level, no frequency division), connect the external clock (EXT.CLK) to the X1 pin through a 13kΩ resistor which is connected in series. In this case, the X2 pin must be held open.

$f_{EXT.CLK}$=10kHz (max.) (pattern FG mode)
Input signal level range
Low-level voltage: 0.0V to 0.8V
High-level voltage: 2.5V to 5.0V

7. Servo constants

When calculating the servo constants, they will be heavily dependent on the motor actually used. Since experience is generally required, these constants should be determined by the motor manufacturer. We can provide the IC characteristics data required for the servo constants calculations as well as frequency characteristics simulation data for the filter constants set by the motor manufacturer.

8. IC internal power dissipation calculation example (calculated at standard ratings)

(1) Power save mode (V_{CC}=5V, S/B pin = open, N pin voltage V_N=5V)

$Ps = PI_{CC}2 + PN$

$=V_{CC} \times I_{CC}2 + V_N \times (V_N/50k\Omega)$

$=5V \times 180\mu A + 5V \times (5V/50k\Omega)$

$=1.4mW$

(2) In start mode

Example: V_{CC}=5V, I_O=0.1A

Intercoil voltage VRm=Rm × I_O + Reverse electromotive force =2.0V

Output source transistor C-to-E voltage $V_{CE}1$ = 2.9V

Output sink transistor C-to-E voltage $V_{CE}2$ = 0.1V

HB pin sink current = 1mA, HB pin voltage = 4V

1) Power dissipation due to current drain ICC: $P1 = V_{CC} \times I_{CC} = 5V \times 21mA = 0.105W$

2) Power dissipation due to the Hall bias current: $P2 = V_{HB} \times I_{HB} = 4V \times 1mA = 0.004W$

3) Power dissipation due to the output drive current: $P3 = (I_O/100) \times (V_{CE}1 - 0.7V) + (I_O/100 \times 1.5) \times (V_{CC} - 0.7V)$
$= 1mA \times 2.2V + 1.5mA \times 4.3V = 0.009W$

4) Power dissipation due to the output transistor: $P4 = V_{CE}1 \times I_O + V_{CE}2 \times I_O$
$= 2.9V \times 0.1A + 0.1V \times 0.1A = 0.300W$

5) The IC's total power dissipation in start mode: P = P1 + P2 + P3 + P4 = 0.42W

9. Measuring the IC's temperature rise

We recommend using the electrostatic breakdown prevention diode between the LD and ground pins of this IC. Disconnect the external pull-up resistor on LD pin when measuring.

(SANYO data: Approx. –2mV/°C at I_{LD} = –500μA, V_{CC} = 5V, LD pin off)