

# DATA SHEET

## **CBTS3253**

Dual 1-of-4 FET multiplexer/demultiplexer  
with Schottky diode clamping

Product data

2002 Nov 06

# Dual 1-of-4 FET multiplexer/demultiplexer with Schottky diode clamping

**CBTS3253**

## FEATURES

- 5  $\Omega$  switch connection between two ports
- TTL-compatible input levels
- Schottky diodes on I/O clamp undershoot
- Minimal propagation delay through the switch
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA

## DESCRIPTION

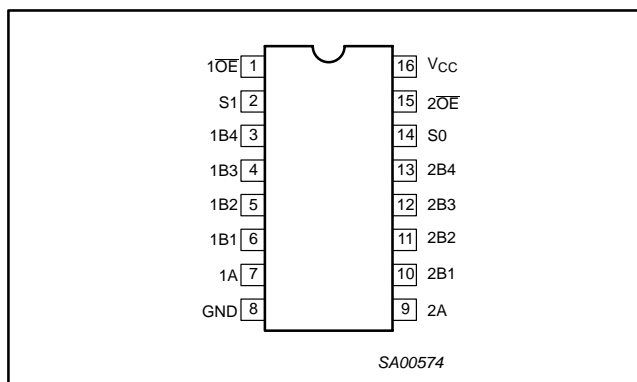
The CBTS3253 is a dual 1-of-4 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

1 $\overline{OE}$ , 2 $\overline{OE}$ , S0, and S1 select the appropriate B output for the A-input data.

Internal Schottky diode provides I/O undershoot protection

The CBTS3253 is characterized for operation from  $-40$  to  $+85^{\circ}\text{C}$ .

## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1 $\overline{OE}$	Output enable
2	S1	Select-control input
3, 4, 5, 6	1B[1–4]	B outputs
7	1A	A input
8	GND	Ground (0 V)
9	2A	A input
10, 11, 12, 13	2B[1–4]	Select-control input
14	S0	Select-control input
15	2 $\overline{OE}$	Output enable
16	V <sub>CC</sub>	Positive supply voltage

## ORDERING INFORMATION

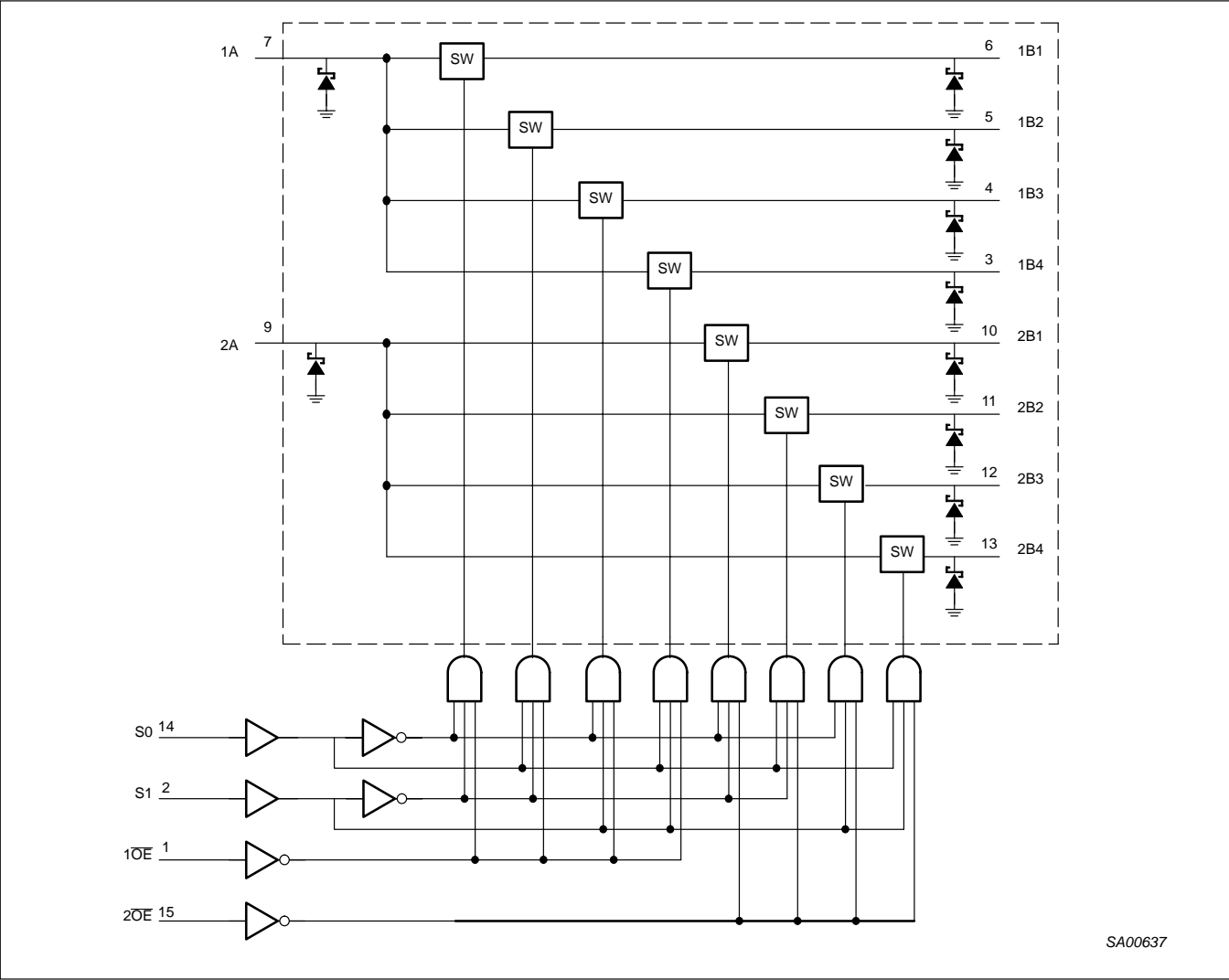
PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DWG NUMBER
16-pin plastic SO	$-40$ to $85^{\circ}\text{C}$	CBTS3253D	CBTS3257	SOT109-1
16-pin plastic SSOP	$-40$ to $85^{\circ}\text{C}$	CBTS3253DB	CS3253	SOT338-1
16-pin plastic SSOP (QSOP)	$-40$ to $85^{\circ}\text{C}$	CBTS3253DS	CBS3253	SOT519-1
16-pin plastic TSSOP	$-40$ to $85^{\circ}\text{C}$	CBTS3253PW	CBS3253	SOT403-1

Standard packing quantities and other packaging data is available at [www.philipslogic.com/packaging](http://www.philipslogic.com/packaging).

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CBTS3253

LOGIC DIAGRAM (positive logic)



FUNCTION TABLE

INPUTS				FUNCTION
OE1	OE2	S1	S0	
H	X	X	X	Disconnect 1A
X	H	X	X	Disconnect 2A
L	L	L	L	1A to 1B1 and 2A to 2B1
L	L	L	H	1A to 1B2 and 2A to 2B2
L	L	H	L	1A to 1B3 and 2A to 2B3
L	L	H	H	1A to 1B4 and 2A to 2B4

# Dual 1-of-4 FET multiplexer/demultiplexer with Schottky diode clamping

CBTS3253

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		−0.5 to +7.0	V
$V_I$	DC input voltage <sup>2</sup>		−0.5 to +7.0	V
	Continuous channel current		128	mA
$I_K$	Input clamp current	$V_{I/O} < 0$	−50	mA
$T_{stg}$	Storage temperature range		−65 to +150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2	—	V
$V_{IL}$	Low-level Input voltage	—	0.8	V
$T_{amb}$	Operating free-air temperature range	−40	+85	°C

### NOTE:

- All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNIT
				T <sub>amb</sub> = −40 to +85 °C			
				MIN	TYP <sup>1</sup>	MAX	
V <sub>IK</sub>	Input clamp voltage	A or B inputs	V <sub>CC</sub> = 4.5 V; I <sub>I</sub> = −18 mA	—	—	−0.8	V
		Control inputs		—	—	−1.2	
V <sub>P</sub>	Pass voltage		V <sub>I</sub> = V <sub>CC</sub> = 5.5 V; I/O = −100 μA	3.4	3.6	3.9	V
I <sub>I</sub>	Input leakage current		V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = 5.5 or GND	—	—	±1	μA
I <sub>CC</sub>	Quiescent supply current		V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	—	—	3	μA
ΔI <sub>CC</sub>	Control inputs <sup>2</sup>		V <sub>CC</sub> = 5.5 V, one input at 3.4 V, other inputs at V <sub>CC</sub> or GND	—	—	2.5	mA
C <sub>I</sub>	Control pins		V <sub>I</sub> = 3 V or 0	—	4.5	—	pF
C <sub>IO(OFF)</sub>	Power-off leakage current	A port	V <sub>O</sub> = 3 V or 0; $\overline{OE}$ = V <sub>CC</sub>	—	24.6	—	pF
		B port	V <sub>O</sub> = 3 V or 0; $\overline{OE}$ = V <sub>CC</sub>	—	7.6	—	
r <sub>on</sub> <sup>3</sup>	On-resistance	V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0 V; I <sub>I</sub> = 64 mA	—	5	7	Ω
			V <sub>I</sub> = 0 V; I <sub>I</sub> = 30 mA	—	5	7	
			V <sub>I</sub> = 2.4 V; I <sub>I</sub> = −15 mA	—	10	15	

### NOTES:

- All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_{amb} = 25 \text{ °C}$ .
- This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.
- Measured by the voltage drop between the A and the B terminals at the indicated current through the switch.  
On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

# Dual 1-of-4 FET multiplexer/demultiplexer with Schottky diode clamping

CBTS3253

## AC CHARACTERISTICS

 $T_{amb} = -40 \text{ to } +85 \text{ }^{\circ}\text{C}$ ;  $C_L = 50 \text{ pF}$ 

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	LIMITS		UNIT
				V <sub>CC</sub> = +5.0 V ±0.5 V		
				MIN	MAX	
t <sub>pd</sub>	Propagation delay <sup>1</sup>	A or B	B or A	—	0.25	ns
		S	A or B	1.2	6.2	
t <sub>en</sub>	Output enable time to High and Low level	S	A or B	1.3	6.3	ns
		OE		1.4	6.4	
t <sub>dis</sub>	Output disable time from High and Low level	S	A or B	1.1	7.2	ns
		OE		1.0	7	

### NOTE:

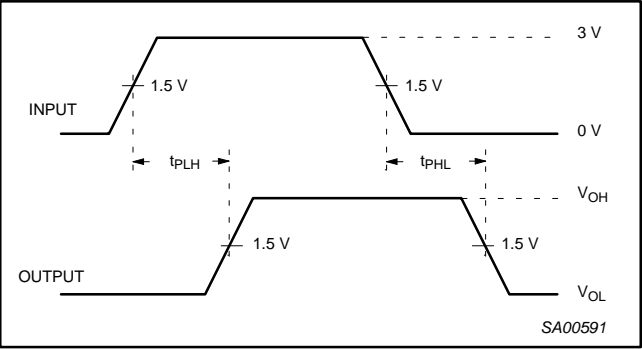
1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Dual 1-of-4 FET multiplexer/demultiplexer  
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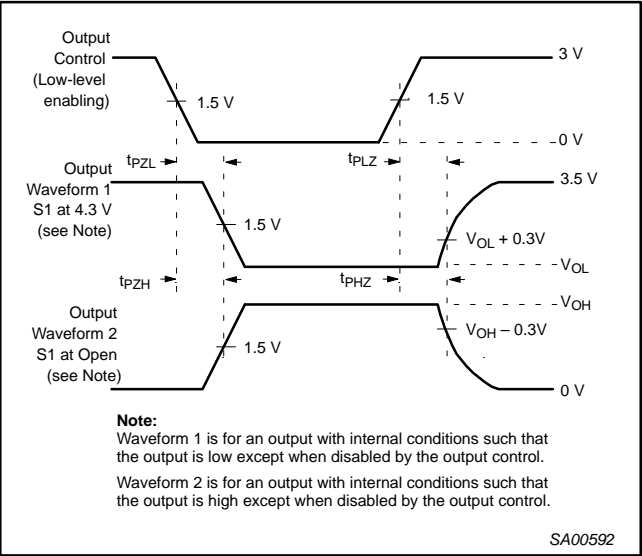
CBTS3253

AC WAVEFORMS

$V_M = 1.5\text{ V}$ ,  $V_{IN} = \text{GND to } 3.0\text{ V}$



Waveform 1. Pulse duration



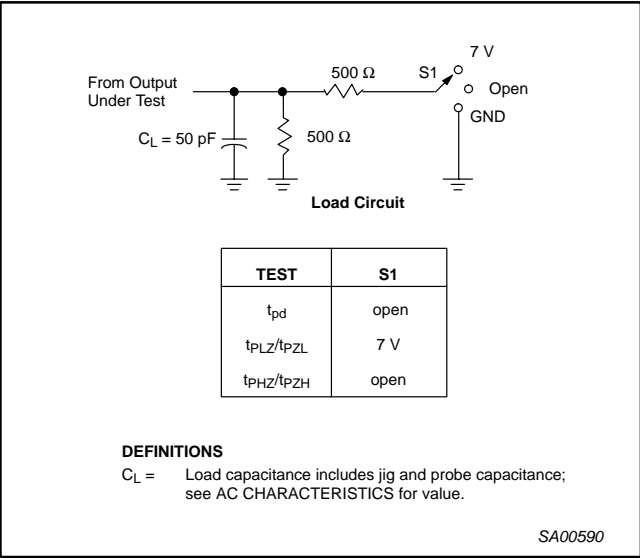
**Note:**  
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Waveform 2. 3-State Output Enable and Disable Times

NOTES:

- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

TEST CIRCUIT AND WAVEFORMS



NOTES:

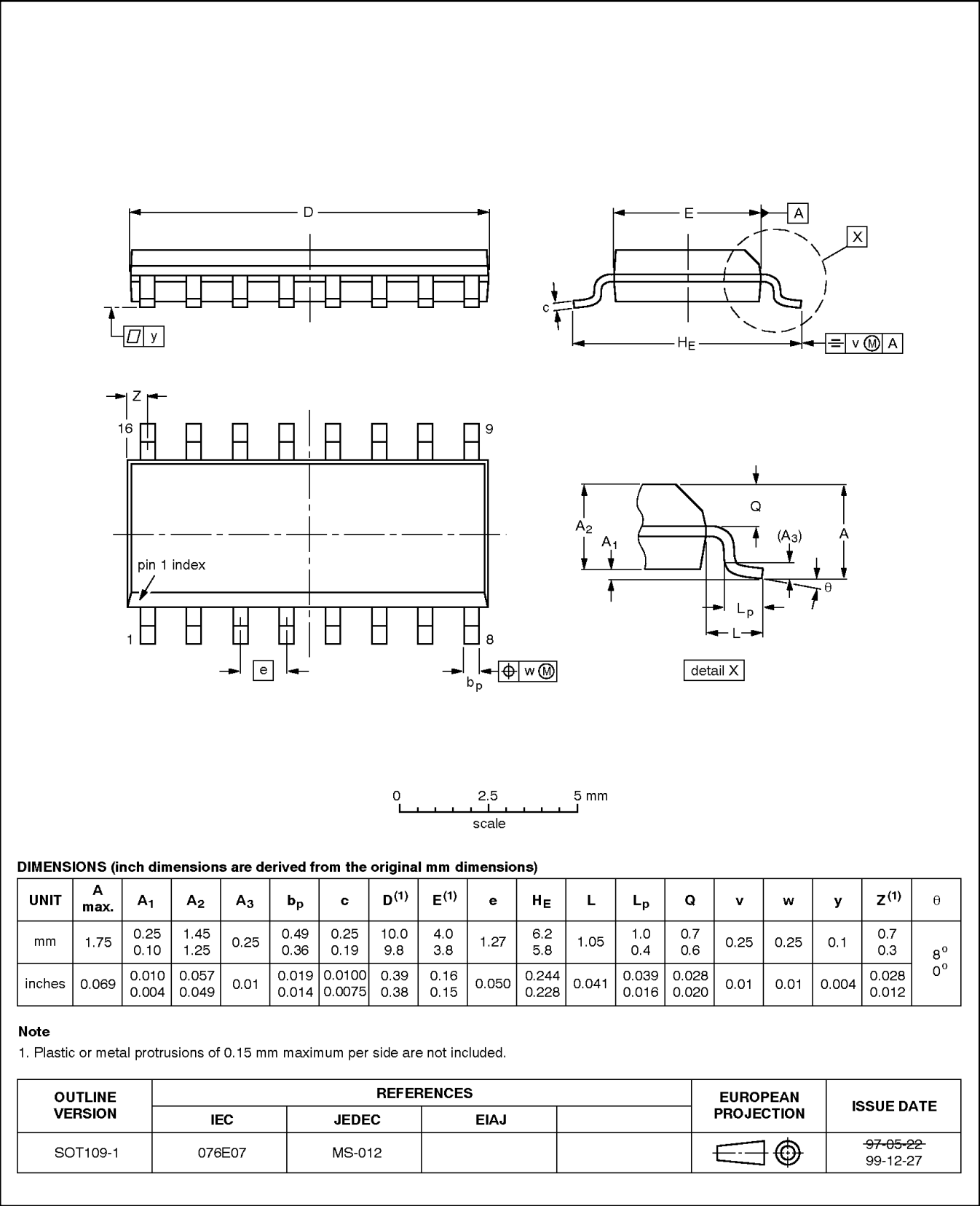
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
- The outputs are measured one at a time with one transition per measurement.

Dual 1-of-4 FET multiplexer/demultiplexer  
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CBTS3253

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

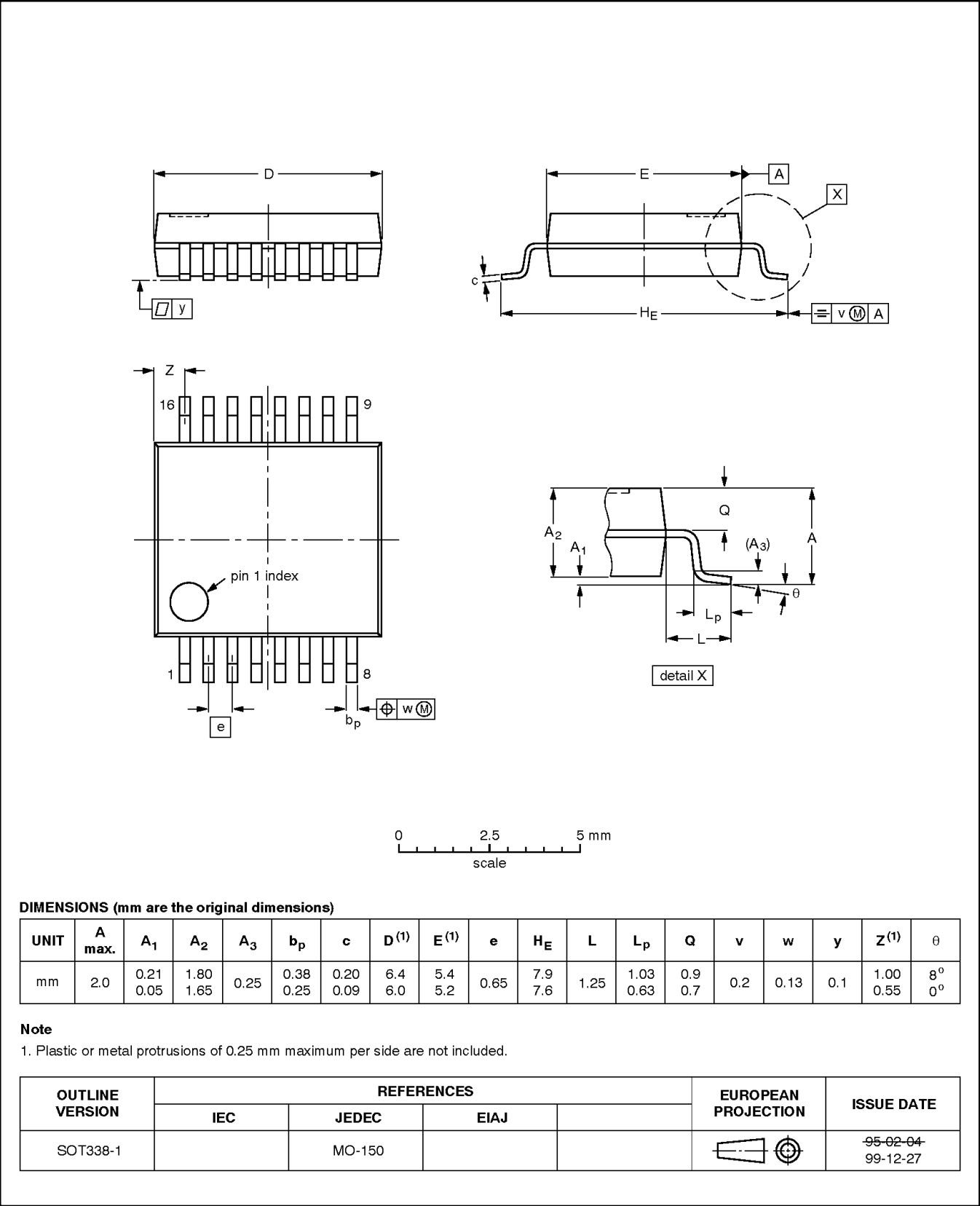


Dual 1-of-4 FET multiplexer/demultiplexer  
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CBTS3253

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



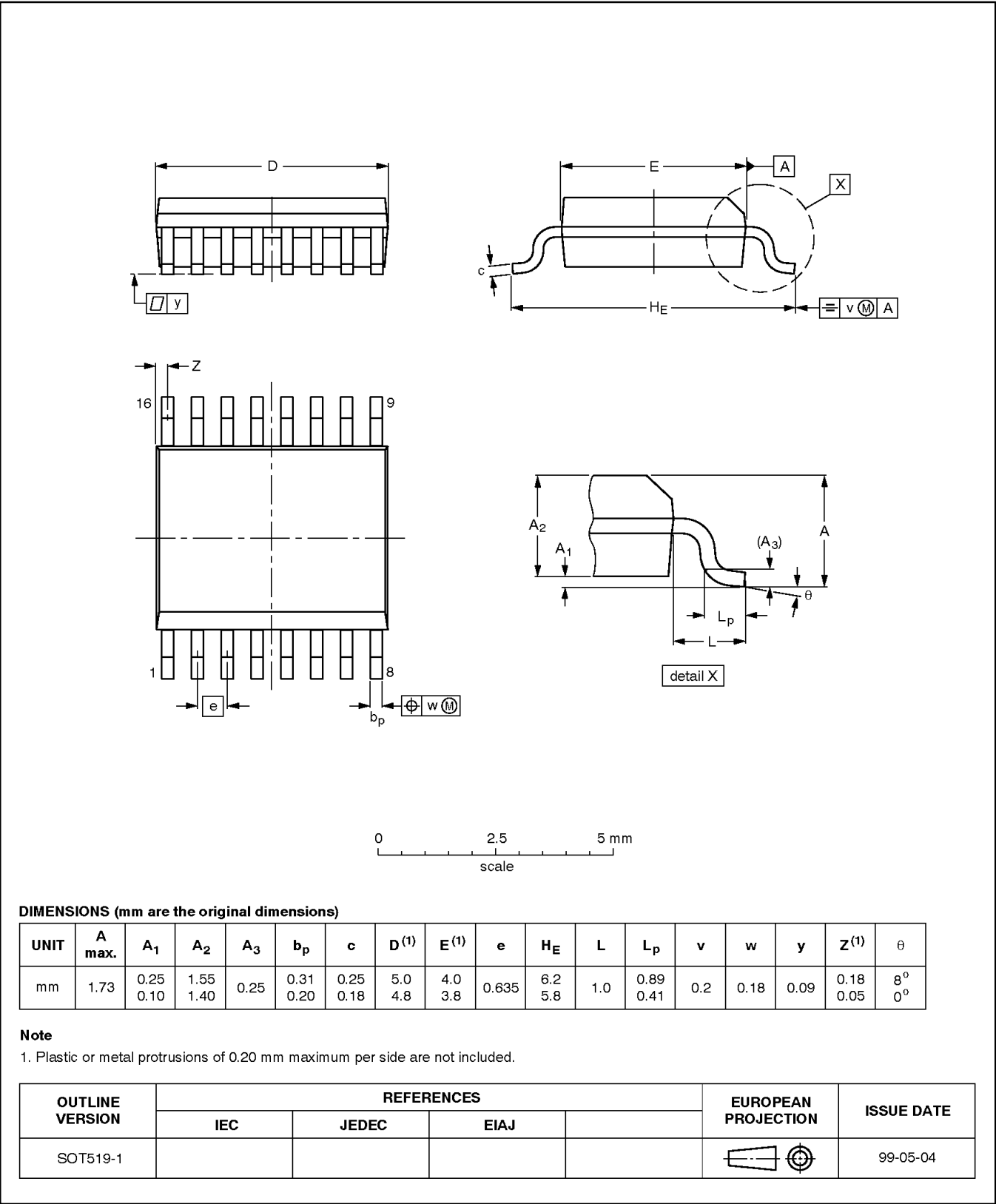


Dual 1-of-4 FET multiplexer/demultiplexer  
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CBTS3253

SSOP16: plastic shrink small outline package; 16 leads;  
body width 3.9 mm; lead pitch 0.635 mm

SOT519-1

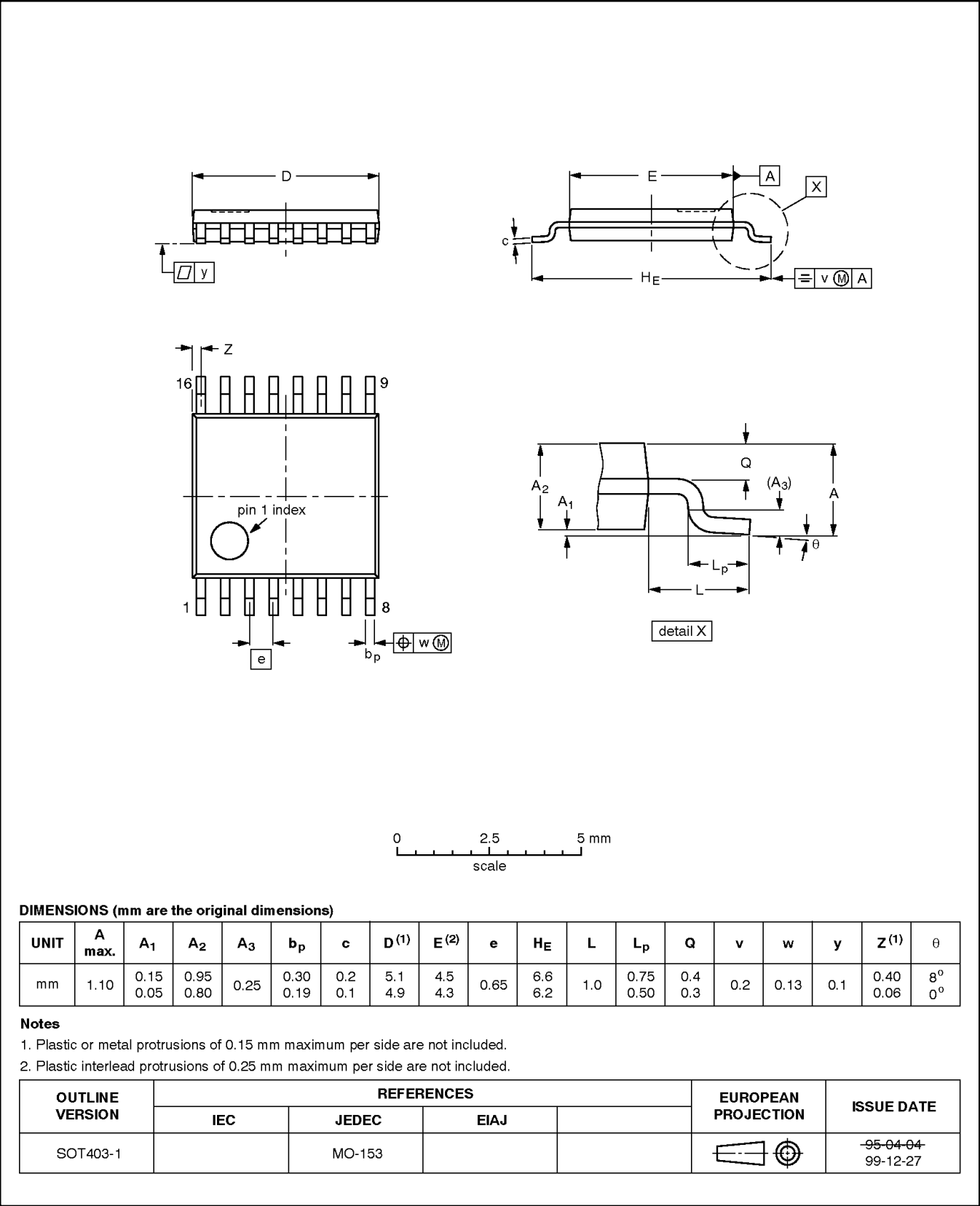


Dual 1-of-4 FET multiplexer/demultiplexer  
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CBTS3253

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



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**CBTS3253****REVISION HISTORY**

Rev	Date	Description
_1	2002 Nov 06	Product data (9397 750 10665); initial version Engineering Change Notice: 853–2390 29065 (2002 Oct 15)

# Dual 1-of-4 FET multiplexer/demultiplexer with Schottky diode clamping

CBTS3253

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