

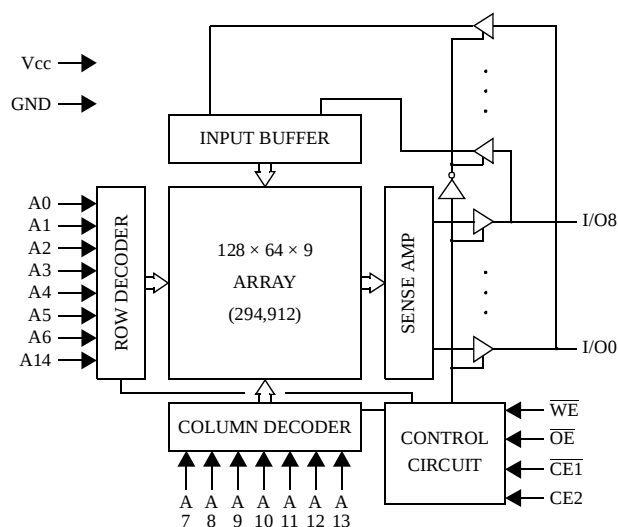


32K×9 CMOS SRAM (Common I/O)

FEATURES

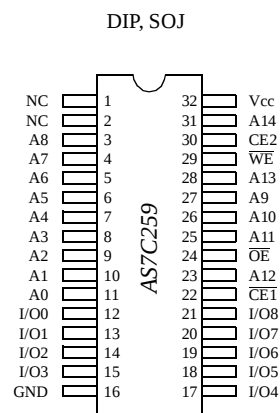
- Organization: 32,768 words × 9 bits
- High speed
 - 12/15/20/25/35 ns address access time
 - 3/4/5/6/8 ns output enable access time
- Low power consumption
 - Active: 633 mW max (10 ns cycle)
 - Standby: 11 mW max, CMOS I/O
2.75 mW max, CMOS I/O, L version
 - Very low DC component in active power
- 2.0V data retention (L version)
- Equal access and cycle times
- Easy memory expansion with $\overline{\text{CE1}}$, CE2, and $\overline{\text{OE}}$ inputs
- TTL-compatible, three-state I/O
- 32-pin JEDEC standard packages
 - 300 mil PDIP and SOJ
- ESD protection > 2000 volts
- Latch-up current > 200 mA

LOGIC BLOCK DIAGRAM



AS7C259-01

PIN ARRANGEMENT



AS7C259-02

SELECTION GUIDE

	7C259-12	7C259-15	7C259-20	7C259-25	7C259-35	Unit
Maximum Address Access Time	12	15	20	25	35	ns
Maximum Output Enable Access Time	4	4	5	6	8	ns
Maximum Operating Current	115	110	100	90	80	mA
Maximum CMOS Standby Current	2.0	2.0	2.0	2.0	2.0	mA
L	0.5	0.5	0.5	0.5	0.5	mA

Shaded areas contain advance information.



FUNCTIONAL DESCRIPTION

The AS7C259 is a high performance CMOS 294,912-bit Static Random Access Memory (SRAM) organized as 32,768 words $\times$ 9 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 12/15/20/25/35 ns with output enable access times (t_{OE}) of 3/4/5/6/8 ns are ideal for high performance applications. Active high and low chip enables ($\overline{CE1}$, CE2) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CE1}$ is HIGH or CE2 is LOW the device enters standby mode. The standard AS7C259 is guaranteed not to exceed 11 mW power consumption in standby mode; the L version is guaranteed not to exceed 1.1 mW. The L version also offers 2.0V data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and both chip enables ($\overline{CE1}$, CE2). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE1}$, CE2), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply. The AS7C259 is packaged in common industry standard packages.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Voltage on Any Pin Relative to GND	V_t	-0.5	+7.0	V
Power Dissipation	P_D	—	1.0	W
Storage Temperature (Plastic)	T_{stg}	-55	+150	$^{\circ}\text{C}$
Temperature Under Bias	T_{bias}	-10	+85	$^{\circ}\text{C}$
DC Output Current	I_{out}	—	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High Z	Standby (I_{SB} , I_{SB1})
X	L	X	X	High Z	Standby (I_{SB} , I_{SB1})
L	H	H	H	High Z	Output Disable
L	H	H	L	D_{out}	Read
L	H	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH



RECOMMENDED OPERATING CONDITIONS

 $(T_a = 0^{\circ}\text{C to } +70^{\circ}\text{C})$

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input Voltage	V_{IH}	2.2	–	$V_{CC}+1.0$	V
	V_{IL}	–0.5*	–	0.8	V

* V_{IL} min = –3.0V for pulse width less than $t_{RC}/2$.

DC OPERATING CHARACTERISTICS¹

 $(V_{CC} = 5V \pm 10\%, \text{GND} = 0V, T_a = 0^{\circ}\text{C to } +70^{\circ}\text{C})$

Parameter	Symbol	Test Conditions	–12		–15		–20		–25		–35		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	$ I_{LI} $	$V_{CC} = \text{Max},$ $V_{in} = \text{GND to } V_{CC}$	–	1	–	1	–	1	–	1	–	1	μA
Output Leakage Current	$ I_{LO} $	$\overline{CE1} = V_{IH} \text{ or } CE2 = V_{IL},$ $V_{CC} = \text{Max},$ $V_{out} = \text{GND to } V_{CC}$	–	1	–	1	–	1	–	1	–	1	μA
Operating Power Supply Current	I_{CC}	$\overline{CE1} = V_{IL}, CE2 = V_{IH},$ $f = f_{max}, I_{out} = 0 \text{ mA}$	–	115	–	110	–	100	–	90	–	80	mA
		L	–	110	–	105	–	95	–	85	–	75	mA
Standby Power Supply Current	I_{SB}	$\overline{CE1} = V_{IH} \text{ or } CE2 = V_{IL},$ $f = f_{max}$	–	40	–	30	–	30	–	25	–	25	mA
		L	–	35	–	25	–	25	–	20	–	20	mA
	I_{SB1}	$\overline{CE1} \geq V_{CC}-0.2V \text{ or } CE2 \leq 0.2V,$ $V_{in} \leq 0.2V \text{ or } V_{in} \geq V_{CC}-0.2V,$ $f = 0$	–	2.0	–	2.0	–	2.0	–	2.0	–	2.0	mA
		L	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5	mA
Output Voltage	V_{OL}	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	V

Shaded areas contain advance information.

CAPACITANCE²

 $(f = 1 \text{ MHz}, T_a = \text{room temperature}, V_{CC} = 5V)$

Parameter	Symbol	Signals	Test Conditions	Max	Unit
Input Capacitance	C_{IN}	A, $\overline{CE1}$, CE2, $\overline{WE}$, $\overline{OE}$	$V_{in} = 0V$	5	pF
I/O Capacitance	$C_{I/O}$	I/O	$V_{in} = V_{out} = 0V$	7	pF



READ CYCLE^{3, 9, 12}

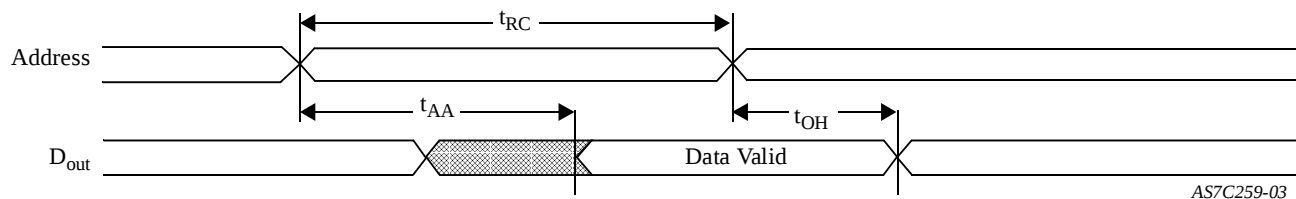
($V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0^\circ C$ to $+70^\circ C$)

Parameter	Symbol	-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	12	—	15	—	20	—	25	—	35	—	ns	
Address Access Time	t_{AA}	—	12	—	15	—	20	—	25	—	35	ns	3
Chip Enable ($\overline{CE1}$) Access Time	t_{ACE1}	—	12	—	15	—	20	—	25	—	35	ns	3, 12
Chip Enable (CE2) Access Time	t_{ACE2}	—	12	—	15	—	20	—	25	—	35	ns	3, 12
Output Enable ($\overline{OE}$) Access Time	t_{OE}	—	3	—	4	—	5	—	6	—	8	ns	
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	3	—	3	—	ns	5
$\overline{CE1}$ LOW to Output in Low Z	t_{CLZ1}	3	—	3	—	3	—	3	—	3	—	ns	4, 5, 12
CE2 HIGH to Output in Low Z	t_{CLZ2}	3	—	3	—	3	—	3	—	3	—	ns	4, 5, 12
$\overline{CE1}$ HIGH to Output in High Z	t_{CHZ1}	—	3	—	4	—	5	—	6	—	8	ns	4, 5, 12
CE2 LOW to Output in High Z	t_{CHZ2}	—	3	—	4	—	5	—	6	—	8	ns	4, 5, 12
$\overline{OE}$ LOW to Output in Low Z	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	4, 5
$\overline{OE}$ HIGH to Output in High Z	t_{OHZ}	—	3	—	4	—	5	—	6	—	8	ns	4, 5
Power Up Time	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	4, 5, 12
Power Down Time	t_{PD}	—	12	—	15	—	20	—	25	—	35	ns	4, 5, 12

Shaded areas contain advance information.

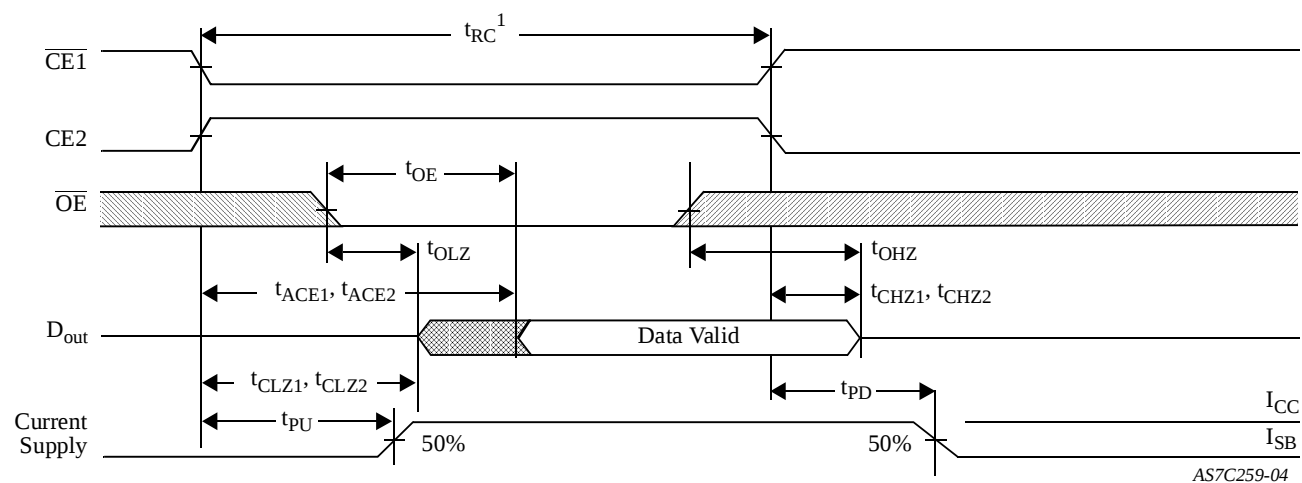
TIMING WAVEFORM OF READ CYCLE 1^{3, 6, 7, 9, 12}

(Address Controlled)



TIMING WAVEFORM OF READ CYCLE 2^{3, 6, 8, 9, 12}

($\overline{CE1}$ and CE2 Controlled)





WRITE CYCLE^{11, 12}

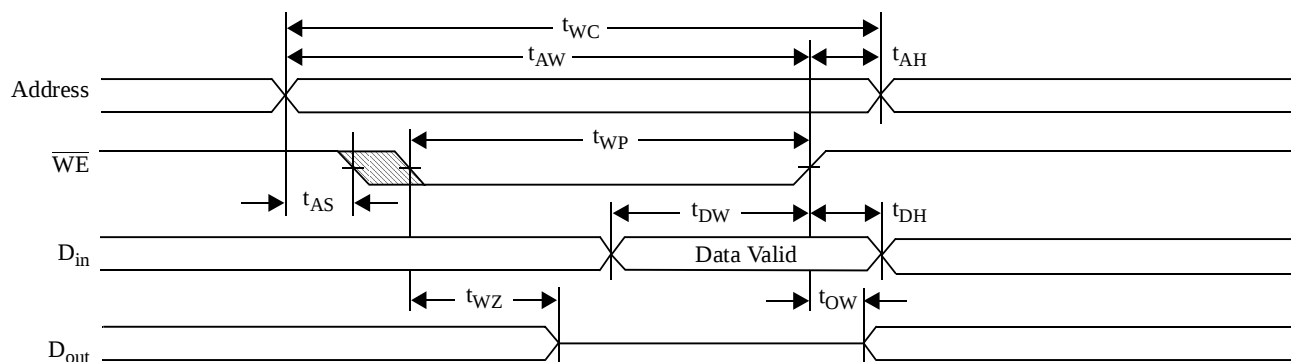
($V_{CC} = 5V \pm 10\%$, GND = 0V, $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{WC}	12	—	15	—	20	—	20	—	30	—	ns	
Chip Enable ($\overline{CE1}$) to Write End	t_{CW1}	10	—	12	—	12	—	15	—	20	—	ns	12
Chip Enable ($\overline{CE2}$) to Write End	t_{CW2}	10	—	12	—	12	—	15	—	20	—	ns	12
Address Setup to Write End	t_{AW}	10	—	12	—	12	—	15	—	20	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	12
Write Pulse Width	t_{WP}	8	—	9	—	12	—	15	—	17	—	ns	
Address Hold From End of Write	t_{AH}	0	—	0	—	0	—	0	—	0	—	ns	
Data Valid to Write End	t_{DW}	6	—	8	—	10	—	10	—	15	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	4, 5
Write Enable to Output in High Z	t_{WZ}	—	5	—	5	—	5	—	5	—	5	ns	4, 5
Output Active From Write End	t_{OW}	3	—	3	—	3	—	3	—	3	—	ns	4, 5

Shaded areas contain advance information.

TIMING WAVEFORM OF WRITE CYCLE 1^{10, 11, 12}

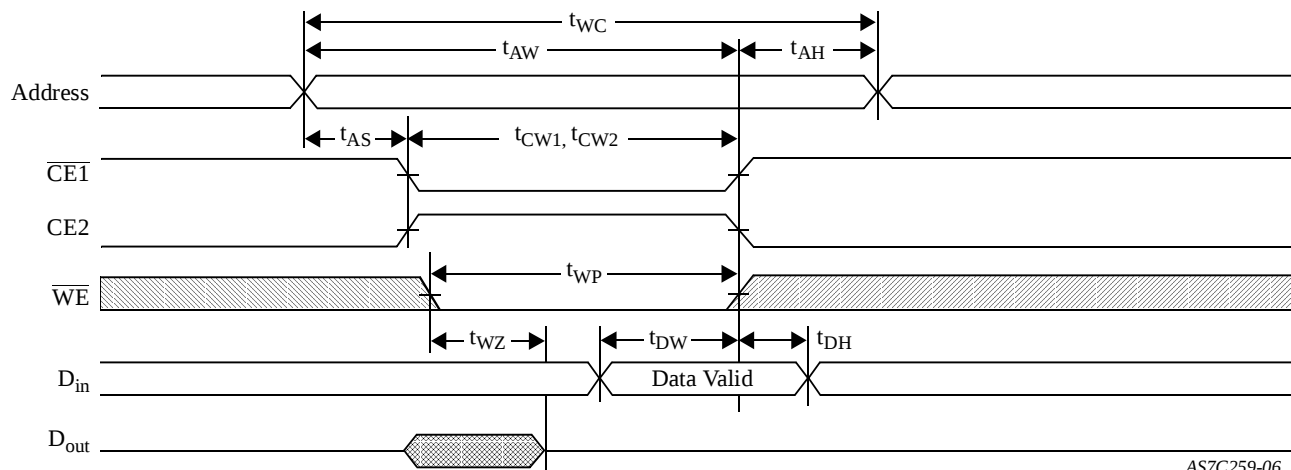
($\overline{WE}$ Controlled)



AS7C259-05

TIMING WAVEFORM OF WRITE CYCLE 2^{10, 11, 12}

($\overline{CE1}$ and $\overline{CE2}$ Controlled)



AS7C259-06



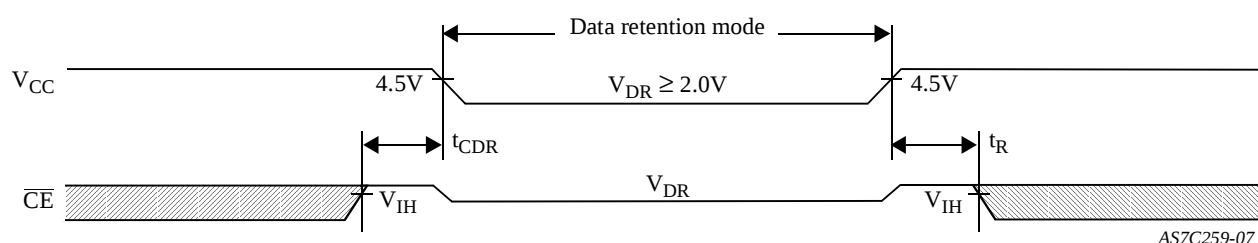
DATA RETENTION CHARACTERISTICS

(L Version Only)

Parameter	Symbol	Test Conditions	Min	Max	Unit
V_{CC} for Data Retention	V_{DR}	$V_{CC} = 2.0V$	2.0	–	V
Data Retention Current	I_{CCDR}	$\overline{CE1} \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$	–	150	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	–	ns
Operation Recovery Time	t_R	$V_{in} \geq V_{CC}-0.2V$ or $V_{in} \leq 0.2V$	t_{RC}	–	ns
Input Leakage Current	$ I_{LI} $		–	1	μA

DATA RETENTION WAVEFORM

(L Version Only)



AC TEST CONDITIONS

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

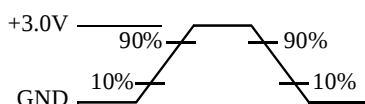


Figure A: Input Waveform
AS7C259-08

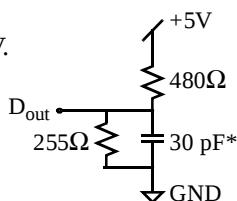


Figure B: Output Load
AS7C259-09

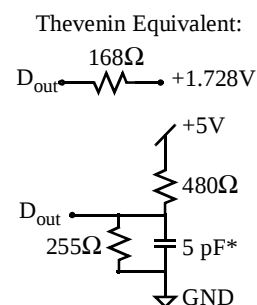


Figure C: Output Load for t_{CLZ} , t_{CHZ}
AS7C259-10

*including scope and jig capacitance

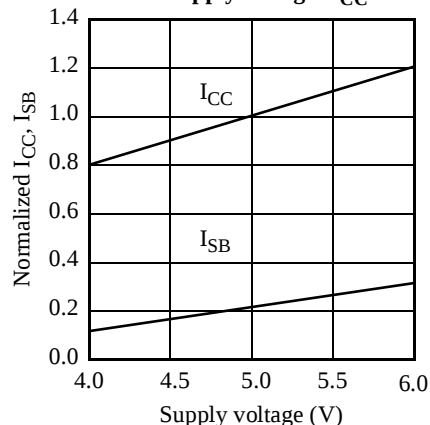
NOTES

1. During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE1}$ is required to meet I_{SB} specification.
2. This parameter is sampled and not 100% tested.
3. For test conditions, see *AC Test Conditions*, Figures A, B, C.
4. t_{CLZ} and t_{CHZ} are specified with $CL = 5pF$ as in Figure C. Transition is measured $\pm 500mV$ from steady-state voltage.
5. This parameter is guaranteed but not tested.
6. $\overline{WE}$ is HIGH for read cycle.
7. $\overline{CE1}$ and $\overline{OE}$ are LOW and $CE2$ is HIGH for read cycle.
8. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9. All read cycle timings are referenced from the last valid address to the first transitioning address.
10. $\overline{CE1}$ or $\overline{WE}$ must be HIGH or $CE2$ LOW during address transitions.
11. All write cycle timings are referenced from the last valid address to the first transitioning address.
12. $\overline{CE1}$ and $CE2$ have identical timing.

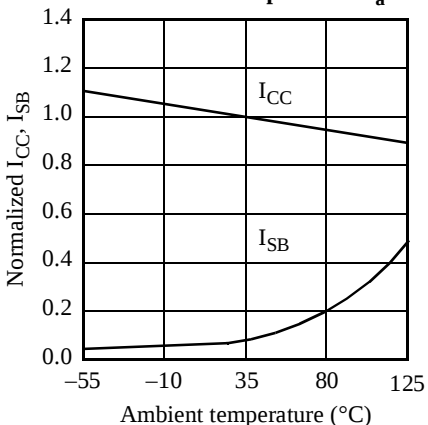


TYPICAL DC AND AC CHARACTERISTICS

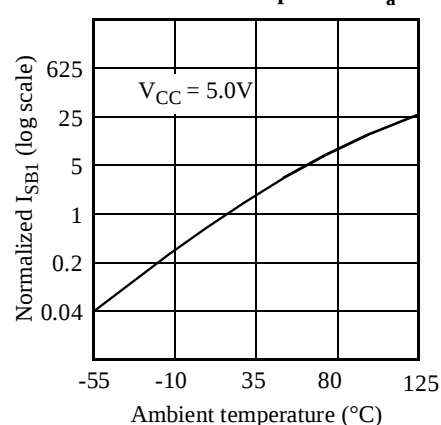
Normalized supply current I_{CC} , I_{SB}
vs. supply voltage V_{CC}



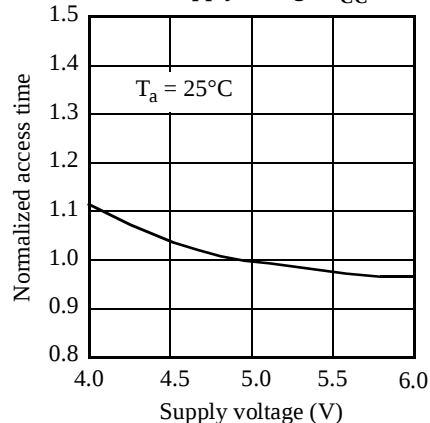
Normalized supply current I_{CC} , I_{SB}
vs. ambient temperature T_a



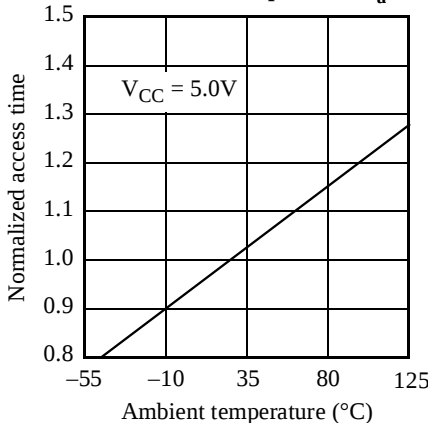
Normalized supply current I_{SB1}
vs. ambient temperature T_a



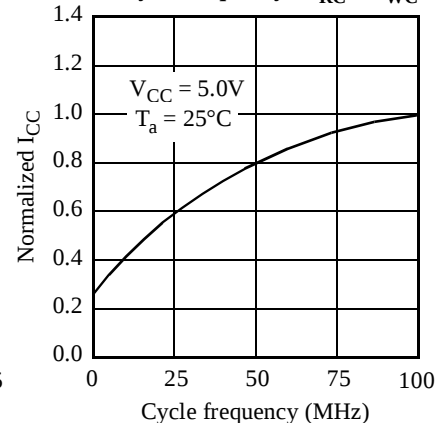
Normalized access time t_{AA}
vs. supply voltage V_{CC}



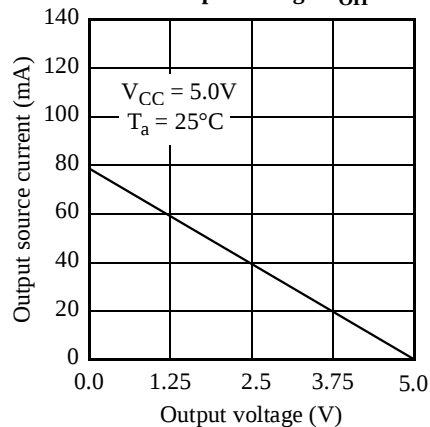
Normalized access time t_{AA}
vs. ambient temperature T_a



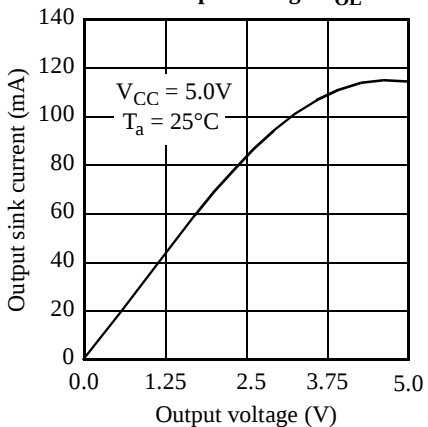
Normalized supply current I_{CC}
vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



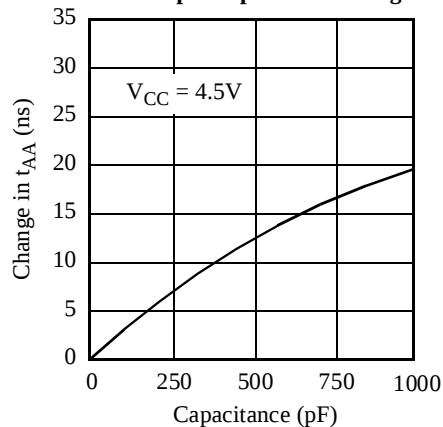
Output source current I_{OH}
vs. output voltage V_{OH}



Output sink current I_{OL}
vs. output voltage V_{OL}



Typical access time change Δt_{AA}
vs. output capacitive loading





ORDERING CODES

Package / Access Time	12 ns	15 ns	20 ns	25 ns	35 ns
Plastic DIP, 300 mil	AS7C259-12PC	AS7C259-15PC	AS7C259-20PC	AS7C259-25PC	AS7C259-35PC
	AS7C259L-12PC	AS7C259L-15PC	AS7C259L-20PC	AS7C259L-25PC	AS7C259L-35PC
Plastic SOJ, 300 mil	AS7C259-12JC	AS7C259-15JC	AS7C259-20JC	AS7C259-25JC	AS7C259-35JC
	AS7C259L-12JC	AS7C259L-15JC	AS7C259L-20JC	AS7C259L-25JC	AS7C259L-35JC

Shaded areas contain advance information.

PART NUMBERING SYSTEM

AS7C	256	X	-XX	X	C
SRAM Prefix	Device Number	Blank L	= Standard Power = Low Power	Access Time	Package: P = PDIP 300 mil J = SOJ 300 mil T = TSOP 8x14
					Commercial Temperature Range, 0°C to 70 °C

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