SanDisk CompactFlash Memory Card

OEM Product Manual

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Revision History

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June 2009	1.0	

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1 Introduction

1.1 General Description

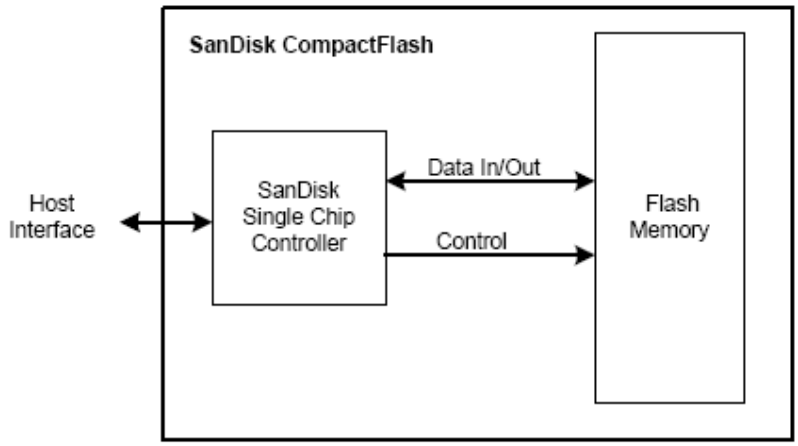
SanDisk CompactFlash® Memory Card products provide high capacity solid-state flash memory that electrically complies with the Personal Computer Memory Card International Association ATA (PC Card ATA) standard. (In Japan, the applicable standards group is JEIDA.) The CompactFlash Memory Card Series also supports a True IDE Mode that is electrically compatible with an IDE disk drive. The original CF form factor card can be used in any system that has a CF slot, and with a Type II PCMCIA adapter can be used in any system that has a PCMCIA Type II or Type III socket.

CompactFlash Memory cards use SanDisk Flash memory, which was designed by SanDisk specifically for use in mass storage applications. In addition to the mass storage-specific flash memory chips, CompactFlash Memory cards include an on-card intelligent controller that provides a high level interface to the host computer. This interface allows a host computer to issue commands to the memory card to read or write blocks of memory. The host addresses the card in 512 byte sectors. Each sector is protected by a powerful Error Correcting Code (ECC).

The on-card intelligent controller in the CompactFlash Memory Card manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management and clock control. Once the card has been configured by the host, it appears to the host as a standard ATA (IDE) disk drive. Additional ATA commands have been provided to enhance system performance.

The host system can support as many cards as there are CompactFlash and PCMCIA Type II or III card slots. The original form factor CompactFlash Memory cards require a PCMCIA Type II Adapter to be used in a PCMCIA Type II or Type III socket.

Figure 1-1 SanDisk CompactFlash Card Block Diagram



1.2 Features

SanDisk CompactFlash Memory cards provide the following system features:

- Up to 64 GB of mass storage data
- PC Card ATA protocol compatible
- True IDE Mode compatible
- Very low CMOS power
- Very high performance
- Very rugged
- Low weight
- Noiseless
- Low Profile
- +3.3 Volts operation +5.0 Volts Tolerant
- Automatic error correction and retry capabilities
- Supports power down commands and sleep modes
- Non-volatile storage (no battery required)

1.3 Scope

This document describes the key features and specifications of CompactFlash Memory cards, as well as the information required to interface this product to a host system. Retail CompactFlash specifications are not covered in this manual.

1.4 CompactFlash Standard

SanDisk CompactFlash Memory cards are fully compatible with the CompactFlash Specification published by the CompactFlash Association. Contact the CompactFlash Association for more information.

CompactFlash Association
P.O. Box 51537
Palo Alto, CA 94303
USA
Phone: 415-843-1220
Fax: 415-493-1871
www.compactflash.org

1.5 PCMCIA Standard

SanDisk CompactFlash Memory cards are fully electrically compatible with the PCMCIA specifications listed below:

- PCMCIA PC Card Standard, 7.0, February 1999
- PCMCIA PC Card ATA Specification, 7.0, February 1999

These specifications may be obtained from:

PCMCIA
2635 N. First Street, Suite 209
San Jose, CA 95131
USA
Phone: 408-433-2273
Fax: 408-433-9558

1.6 Related Documentation

ATA operation is governed by the ATA-4 specification published by ANSI. For more information, refer to the American National Standard X3.221: AT Attachment for Interface for Disk Drives document.

Documentation can be ordered from IHS by calling 1-800-854-7179 or accessing their Web site: http://global.ihs.com.

1.7 Functional Description

CompactFlash Memory cards contain a high level, intelligent subsystem as shown in the block diagram, Figure 1-1. This intelligent (microprocessor) subsystem provides many capabilities not found in other types of memory cards. These capabilities include the following:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Host independence from details of erasing and programming flash memory.
- Sophisticated system for managing defects (analogous to systems found in magnetic disk drives).
- Sophisticated system for error recovery including a powerful error correction code (ECC).
- Power management for low power operation.
- Implementation of dynamic and static wear-leveling to extend card's life.

1.7.1 Technology Independence

The 512-byte sector size of the CompactFlash Memory Card is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues a Read or Write command to the card. This command contains the address and the number of sectors to write/read. The host software then waits for the command to complete.

The host software does not get involved in the details of how the flash memory is erased, programmed or read. This is extremely important as flash devices are expected to get more and more complex in the future. Because the CompactFlash Memory Card Series uses an intelligent on-board controller, the host system software will not require changing as new flash memory evolves. In other words, systems that support CompactFlash Memory cards now, will be able to access future SanDisk cards built with new flash technology without having to update or change host software.

1.7.2 Defect and Error Management

CompactFlash Memory cards contain a sophisticated defect and error management system. This system is analogous to the systems found in magnetic disk drives and in many cases offers enhancements. If necessary, the cards will rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume any user data space.

The CompactFlash Memory Card soft error rate specification is much better than the magnetic disk drive specification. In the extremely rare case a read error does occur, CompactFlash Memory cards have innovative algorithms to recover the data by using hardware on-the-fly Error Detection Code/Error Correction Code (EDC/ECC), based on a BCH algorithm.

These defect and error management systems, coupled with the solid state construction, give SanDisk CompactFlash cards unparalleled reliability

1.7.3 Wear Leveling

Wear Leveling is an intrinsic part of the erase pooling functionality of SanDisk CompactFlash using NAND memory. The CF WEAR LEVEL command is supported as a NOP operation to maintain backward compatibility with existing software utilities. Advanced features of dynamic and static wear-leveling, and automatic block management are used to ensure high data reliability and maximize flash life expectancy.

1.7.4 Using Erase Sector and Write Commands

SanDisk CompactFlash Memory cards support the CF ERASE SECTOR and WRITE WITHOUT ERASE commands. In some applications, write operations may be faster if the addresses being written are first erased with the ERASE SECTOR command. WRITE WITHOUT ERASE behaves as a normal write command and no performance gain results from its use.

1.7.5 Automatic Sleep Mode

A unique feature of the SanDisk CompactFlash Memory Card is automatic entrance and exit from sleep mode. Upon completion of a command, the card will enter sleep mode to conserve power if no further commands are received within 5 msec. The host does not have to take any action for this to occur. In most systems, the CompactFlash Memory Card is in sleep mode except when the host is accessing it, thus conserving power. The delay from command completion to entering sleep mode is adjustable.

When the host is ready to access the card and is in sleep mode, any command issued to it will cause the card to exit sleep and respond. The host does not have to follow the ATA protocol of issuing a reset first. It may do this if desired, but it is not needed. By not issuing the reset, performance is improved through the reduction of overhead but this must be done only for the SanDisk products as other ATA products may not support this feature.

1.7.6 Dynamic Adjustment of Performance vs. Power Consumption

This feature is no longer supported. This command will be treated as a NOP (No Operation) to guarantee backward compatibility.

1.7.7 Power Supply Requirements

This is a dual voltage product, which means it will operate at a voltage range of 3.30 volts ± 5% or 5.00 volts ± 10%. Per the PCMCIA specification Section 2.1.1, the host system must apply 0 volts in order to change a voltage range. This same procedure of providing 0 volts to the card is required if the host system applies an input voltage outside the desired voltage by more than 15%. This means less than 4.25 volts for the 5.00-volt range and less than 2.75 volts for the 3.30 volt range.

2 Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1 System Environmental Specifications

Table 2-1 contains environmental specifications which include temperature, humidity, acoustic noise, vibration, shock and altitude.

Table 2-1 Environmental Specifications

	CompactFlash 200x		CompactFlash 400x
Temperature	Operating: Non-operating:	0º C to 70º C -25 º C to 85º	-25 º C to 85 º C -25 º C to 85 º C
Humidity	Operating: Non-operating:	8% to 95% non-condensing 8% to 95% non-condensing	8% to 95% non-condensing 8% to 95% non-condensing
Acoustic Noise	At 1 meter:	0 dB	0 dB
Vibration	Operating: Non-operating:	15 G peak to peak maximum 15 G peak to peak maximum	15 G peak to peak maximum 15 G peak to peak maximum
Shock	Operating: Non-operating:	2,000 G maximum 2,000 G maximum	2,000 G maximum 2,000 G maximum
Altitude (relative to sea level)	Operating: Non-operating:	80,000 ft. maximum 80,000 ft. maximum	80,000 ft. maximum 80,000 ft. maximum

2.2 System Power Requirements

All values quoted in Table 2-2 are typical at 25° C and nominal supply voltage unless otherwise stated.

Sleep mode currently is specified under the condition that all card inputs are static CMOS levels and in a "Not Busy" operating state.

Table 2-2 Power Requirements

DC Input Voltage (Vcc) 100 mV max. ripple (p-p)		3.3V +/- 5%	5V +/- 10%
Memory Subsystem[a]	CompactFlash 200x Memory Card		
	Sleep	1 mA	1.2 mA
	Read	500 mA	500 mA
	Write	500 mA	500 mA
	Read/ Write Peak	500 mA	500 mA
Memory Subsystem[a]	CompactFlash 400x Memory Card		
	Sleep	1 mA	1.2 mA
	Read	500 mA	500 mA
	Write	500 mA	500 mA
	Read/ Write Peak	500 mA	500 mA

a. Maximum Average Value.

2.3 System Performance

All performance timings assume the CompactFlash Memory Card Series controller is in the default (i.e., fastest) mode.

Table 2-3 Performance

CompactFlash 200x Memory Card	
Start-up Times	
Sleep to Write	2.5 ms maximum
Sleep to Read	20 ms maximum
Reset to Ready	120 ms typical; 400 ms maximum
Data Transfer Rate To/From Host	66.0 MB/sec burst
Maximum Performance	
Sequential Read	30.0 MB/sec
Sequential Write	30.0 MB/sec
CompactFlash 400x Memory Card	
Start-up Times	
Sleep to Write	2.5 ms maximum
Sleep to Read	20 ms maximum
Reset to Ready	120 ms typical; 400 ms maximum
Data Transfer Rate To/From Host	100.0 MB/sec burst
Maximum Performance	
Sequential Read	60.0 MB/sec
Sequential Write	60.0 MB/sec

NOTE: The Sleep to Write and Sleep to Read times are the times it takes the CompactFlash Memory Card to exit sleep mode when any command is issued by the host to when the card is reading or writing. CompactFlash Memory cards do not require a reset to exit sleep mode.

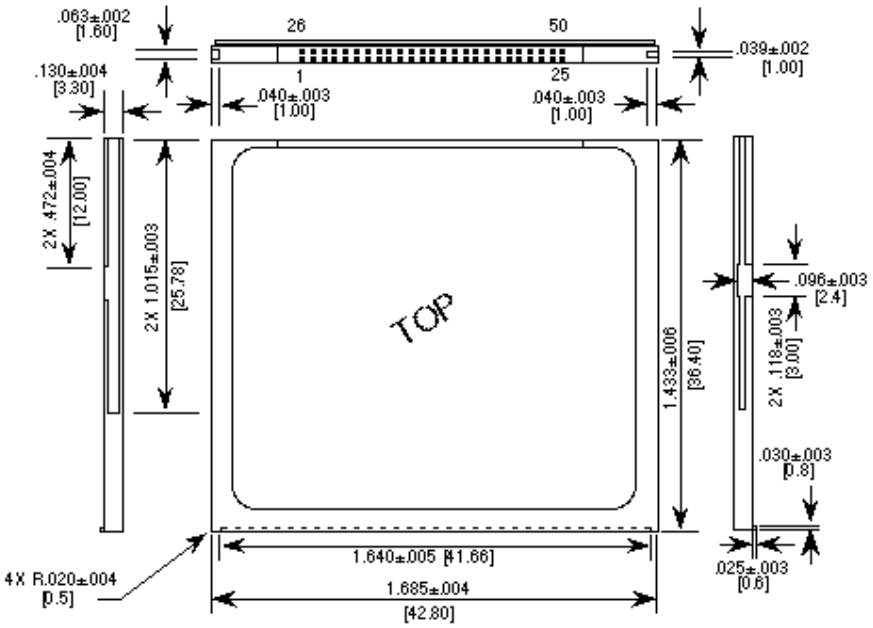
2.4 Physical Specifications

Refer to Table 2-5 and see Figure 2-1 for CompactFlash Memory Card physical specifications and dimensions.

Table 2-5 CompactFlash Physical Dimensions

Weight	11.4 g (.40 oz) typical, 14.2 g (.50 oz) maximum
Length	36.40 ± 0.15 mm (1.433 ± .006 in)
Width	42.80 ± 0.10 mm (1.685 ± .004 in)
Thickness	3.3 mm ± 0.10 mm (.130 ± .004 in) (Excluding Lip)

Figure 2-1 CompactFlash Memory Card Dimensions



3 Interface Description

3.1 Physical Description

The host connects to SanDisk CompactFlash Memory cards using a standard 50-pin connector consisting of two rows of 25 female contacts each on 50 mil (1.27 mm) centers.

3.1.1 Pin Assignments and Types

The signal/pin assignments are listed in Table 3-1. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Sections 3.3.1 and 3.3.2 define the DC characteristics for all input and output type structures..

Table 3-1 PC Card Memory Mode Pin Assignments

Pin No.	Signal Name	Pin Type	I/O Type	Pin No.	Signal Name	Pin Type	I/O Type
1	GND		Ground	26	-CD1	O	Ground
2	D03	I/O	I1Z, OZ3	27	D11	I/O	I1Z, OZ3
3	D04	I/O	I1Z, OZ3	28	D12	I/O	I1Z, OZ3
4	D05	I/O	I1Z, OZ3	29	D13	I/O	I1Z, OZ3
5	D06	I/O	I1Z, OZ3	30	D14	I/O	I1Z, OZ3
6	D07	I/O	I1Z, OZ3	31	D15	I/O	I1Z, OZ3
7	-CE1	I	I3U	32	-CE2	I	I3U
8	A10	I	I1Z	33	-VS1	O	Ground
9	-OE	I	I3U	34	-IORD	I	I3U
					HSTROBE		
					-HDMARDY		
10	A09	I	I1Z	35	-IOWR	I	I3U
11	A08	I	I1Z	36	-WE	I	I3U
12	A07	I	I1Z	37	READY	O	OT1
13	VCC		Power	38	VCC		Power
14	A06	I	I1Z	39	-CSEL	I	I2Z
15	A05	I	I1Z	40	-VS2	O	OPEN
16	A04	I	I1Z	41	RESET	I	I2Z
17	A03	I	I1Z	42	-WAIT	O	OT1
					-DDMARDY[10]		
					DSTROBE[11]		
18	A02	I	I1Z	43	-INPACK	O	OT1
					-DMARQ [12]		
19	A01	I	I1Z	44	-REG	I	I3U
					-DMACK [12]		
20	A00	I	I1Z	45	BVD2	O	OT1
21	D00	I/O	I1Z, OZ3	46	BVD1	O	OT1
22	D01	I/O	I1Z, OZ3	47	D08[1]	I/O	I1Z, OZ3
23	D02	I/O	I1Z, OZ3	48	D09[1]	I/O	I1Z, OZ3
24	WP	O	OT3	49	D10[1]	I/O	I1Z, OZ3
25	-CD2	O	Ground	50	GND		Ground

PC Card I/O Pin Assignments are contained in Table 3-2.

Table 3-2 PC Card I/O Mode Pin Assignments

Pin No.	Signal Name	Pin Type	I/O Type	Pin No.	Signal Name	Pin Type	I/O Type
1	GND		Ground	26	-CD1	O	Ground
2	D03	I/O	I1Z, OZ3	27	D11	I/O	I1Z, OZ3
3	D04	I/O	I1Z, OZ3	28	D12	I/O	I1Z, OZ3
4	D05	I/O	I1Z, OZ3	29	D13	I/O	I1Z, OZ3
5	D06	I/O	I1Z, OZ3	30	D14	I/O	I1Z, OZ3
6	D07	I/O	I1Z, OZ3	31	D15	I/O	I1Z, OZ3
7	-CE1	I	I3U	32	-CE2	I	I3U
8	A10	I	I1Z	33	-VS1	O	Ground
9	-OE	I	I3U	34	-IORD	I	I3U
					HSTROBE		
					-HDMARDY		
10	A09	I	I1Z	35	-IOWR	I	I3U
					STOP		
11	A08	I	I1Z	36	-WE	I	I3U
12	A07	I	I1Z	37	READY	O	OT1
13	VCC		Power	38	VCC		Power
14	A06	I	I1Z	39	-CSEL[5]	I	I2Z
15	A05	I	I1Z	40	-VS2	O	OPEN
16	A04	I	I1Z	41	RESET	I	I2Z
17	A03	I	I1Z	42	-WAIT	O	OT1
					-DDMARDY		
					DSTROBE		
18	A02	I	I1Z	43	-INPACK	O	OT1
					-DMARQ		
19	A01	I	I1Z	44	-REG	I	I3U
					-DMACK		
20	A00	I	I1Z	45	BVD2	O	OT1
21	D00	I/O	I1Z, OZ3	46	BVD1	O	OT1
22	D01	I/O	I1Z, OZ3	47	D08	I/O	I1Z, OZ3
23	D02	I/O	I1Z, OZ3	48	D09	I/O	I1Z, OZ3
24	WP	O	OT3	49	D10	I/O	I1Z, OZ3
25	-CD2	O	Ground	50	GND		Ground

True IDE Mode Pin Assigments are contained in Table 3-3.

Table 3-3 True IDE Mode Pin Assignments

Pin No.	Signal Name	Pin Type	I/O Type	Pin No.	Signal Name	Pin Type	I/O Type
1	GND		Ground	26	-CD1	O	Ground
2	D03	I/O	I1Z, OZ3	27	D11	I/O	I1Z, OZ3
3	D04	I/O	I1Z, OZ3	28	D12	I/O	I1Z, OZ3
4	D05	I/O	I1Z, OZ3	29	D13	I/O	I1Z, OZ3
5	D06	I/O	I1Z, OZ3	30	D14	I/O	I1Z, OZ3
6	D07	I/O	I1Z, OZ3	31	D15	I/O	I1Z, OZ3
7	-CS0	I	I3Z	32	-CS1	I	I3Z
8	A10	I	I1Z	33	-VS1	O	Ground
9	-ATA SEL	I	I3U	34	-IORD	I	I3Z
					HSTROBE		
					-HDMARDY		
10	A09	I	I1Z	35	-IOWR	I	I3Z
					STOP		
11	A08	I	I1Z	36	-WE	I	I3U
12	A07	I	I1Z	37	INTRQ	O	OZ1
13	VCC		Power	38	VCC		Power
14	A06	I	I1Z	39	-CSEL	I	I2U
15	A05	I	I1Z	40	-VS2	O	OPEN
16	A04	I	I1Z	41	-RESET	I	I2Z
17	A03	I	I1Z	42	IORDY	O	ON1
					-DDMARDY		OT1
					DSTROBE		
18	A02	I	I1Z	43	DMARQ	O	OZ1
19	A01	I	I1Z	44	-DMACK	I	I3U
20	A00	I	I1Z	44	-DMACK	I	I3U
21	D00	I/O	I1Z, OZ3	46	-PDIAG	I/O	I1U,ON1
22	D01	I/O	I1Z, OZ3	45	-DASP	I/O	I1U, ON1
23	D02	I/O	I1Z, OZ3	46	-PDIAG	I/O	I1U, ON1
24	-IOCS16	O	ON3	47	D08	I/O	I1Z, OZ3
25	-CD2	O	Ground	48	D09	I/O	I1Z, OZ3

3.2 Electrical Description

The CompactFlash Memory Card Series is optimized for operation with hosts, which support the PCMCIA I/O interface standard conforming to the PC Card ATA specification. However, the card may also be configured to operate in systems that support only the memory interface standard. The CompactFlash card configuration is controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the card.

Table 3-4 describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the card sources are outputs. SanDisk CompactFlash Memory Card logic levels conform to those specified in Section 3.3 of the PCMCIA Release 2.1 Specification.

NOTE: The sleep-to-write and sleep-to-read times are the time it takes the card to exit sleep mode when any command is issued by the host to when the card is reading or writing. CompactFlash Memory cards do not require a reset to exit sleep mode.

The SanDisk CompactFlash Memory Card signals are described in Table 3-4.

Table 3-4 Signal Description

Signal Name	Dir.	Pin	Description
A10 – A00 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers.
A10 – A00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A02 - A00 (True IDE Mode)	I	18,19,20	In True IDE Mode, only A [02:00] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high, as BVD1 is not supported.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card I/O Mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompactFlash Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash Storage Card or CF+ Card is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.

Signal Name	Dir.	Pin	Description
-CD1, -CD2 (True IDE Mode)			This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. While (-) DMACK is asserted, -CE1 and -CE2 shall be held negated and the width of the transfers shall be 16 bits.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode, -CS0 is the address range select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2, 23, 22, 21	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15 - D00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
D15 - D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode)	--	1,50	Ground.
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.
-INPACK (PC Card Memory Mode except Ultra DMA Protocol Active)	O	43	This signal is not used in this mode.

Signal Name	Dir.	Pin	Description
-INPACK (PC Card I/O Mode except Ultra DMA Protocol Active) Input Acknowledge			The Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF+ Card and the CPU. Hosts that support a single socket per interface logic, such as for Advanced Timing Modes and Ultra DMA operation may ignore the –INPACK signal from the device and manage their input buffers based solely on Card Enable signals.
-DMARQ (PC Card Memory Mode - Ultra DMA Protocol Active) -DMARQ (PC Card I/O Mode - Ultra DMA Protocol Active) DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with (-) DMACK, i.e., the device shall wait until the host asserts (-) DMACK before negating (-) DMARQ, and re-asserting (-) DMARQ if there is more data to transfer. In PCMCIA I/O Mode, the -DMARQ shall be ignored by the host while the host is performing an I/O Read cycle to the device. The host shall not initiate an I/O Read cycle while -DMARQ is asserted by the device. In True IDE Mode, DMARQ shall not be driven when the device is not selected in the Drive-Head register. While a DMA operation is in progress, -CS0 (-CE1) and -CS1 (-CE2) shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for True IDE DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode operation. A host that does not support DMA mode and implements both PC Card and True IDE modes of operation need not alter the PC Card mode connections while in True IDE mode as long as this does not prevent proper operation in any mode.
-IORD (PC Card Memory Mode except Ultra DMA Protocol Active)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode except Ultra DMA Protocol Active)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF+ Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.

Signal Name	Dir.	Pin	Description
-HDMARDY (All Modes - Ultra DMA Protocol DMA Read)			In all modes when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate –HDMARDY to pause an Ultra DMA transfer.
HSTROBE (All Modes - Ultra DMA Protocol DMA Write)			In all modes when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
-IOWR (PC Card Memory Mode – Except Ultra DMA Protocol Active)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode – Except Ultra DMA Protocol Active)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
STOP (All Modes – Ultra DMA Protocol Active)			In All Modes, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA data burst.
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.

Signal Name	Dir.	Pin	Description
READY (PC Card Memory Mode)	O	37	In Memory Mode, this signal is set high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.
-IREQ (PC Card I/O Mode)			I/O Operation – After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode – Except Ultra DMA Protocol Active) Attribute Memory Select	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. In PC Card Memory Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal negated during the execution of any DMA Command by the device.
-REG (PC Card I/O Mode – Except Ultra DMA Protocol Active)			The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus. In PC Card I/O Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal asserted during the execution of any DMA Command by the device.
-DMACK (PC Card Memory Mode when Ultra DMA Protocol Active) DMACK (PC Card I/O Mode when Ultra DMA Protocol Active) -DMACK (True IDE Mode)			This is a DMA Acknowledge signal that is asserted by the host in response to (-) DMARQ to initiate DMA transfers. In True IDE Mode, while DMA operations are not active, the card shall ignore the (-) DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PC Card and True-IDE modes of operation need not alter the PC Card mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.

Signal Name	Dir.	Pin	Description
RESET (PC Card Memory Mode)	I	41	The CompactFlash Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode, this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode)	--	13,38	+5 V, +3.3 V power.
VCC (PC Card I/O Mode)			This signal is the same for all modes.
VCC (True IDE Mode)			This signal is the same for all modes.
-VS1 -VS2 (PC Card Memory Mode)	O	33 40	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the CompactFlash Storage Card or CF+ Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.
-VS1 -VS2 (PC Card I/O Mode)			This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)			This signal is the same for all modes.
-WAIT (PC Card Memory Mode – Except Ultra DMA Protocol Active)	O	42	The -WAIT signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card I/O Mode – Except Ultra DMA Protocol Active)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.
-DDMARDY (All Modes – Ultra DMA Write Protocol Active)			In all modes, when Ultra DMA mode DMA Write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive Ultra DMA data out bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer.

Signal Name	Dir.	Pin	Description
DSTROBE (All Modes – Ultra DMA Read Protocol Active)			In all modes, when Ultra DMA mode DMA Read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst.
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect	O	24	Memory Mode – The CompactFlash Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation – When the CompactFlash Storage Card or CF+ Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

3.3 Electrical Specification

All D.C. Characteristics for the CompactFlash Memory Card Series are defined as follows:

Typical conditions unless otherwise stated:

V_{CC} = 5V +/- 10% Tolerant

V_{CC} = 3.3V +/- 5%

Ta = 0° C to 60° C

Absolute Maximum Conditions:

V_{CC} = -0.3V min. to 6.5V max.

V* = 0.5V min. to V_{CC} + 0.5V max.

*Voltage on any pin except V_{CC} with respect to GND.

3.3.1 Input Leakage Control and Input Characteristics

In Table 3-5, “x” refers to the characteristics described in Table 3-6. For example–"I1U" indicates a pull-up resistor with a Type 1 input characteristic.

Table 3-5 Input Leakage Control

Type	Parameter	Symbol	Conditions	MIN	MAX	Unit
IxZ	Input Leakage Current	IL	Vih=VCC/Vil=GND	-1	1	uA
IxU	Pull Up Resistor	RPU1	VCC=5.0V	50k	500k	Ohm
IxD	Pull Down Resistor	RPD1	VCC=5.0V	50k	500k	Ohm

NOTE: The minimum pull-up resistor input leakage is 50k ohms rather than the 10k ohms stated in the PCMCIA PC Card specification.

Table 3-6 defines the input characteristics of the parameters in Table 3-5.

Table 3-6 Input Characteristics

Type	Parameter	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
			VCC=3.3V			VCC=5.0V			
1	Input Voltage CMOS	Vih Vil	2.0		 0.8	2.0		 0.8	Volts
2	Input Voltage CMOS	Vih Vil	2.0		 0.8	2.0		 0.8	Volts
3	Input Voltage CMOS Schmitt Trigger	Vt+(Vp)[1] Vt-(Vn)[2] Vh(ΔVt)[3]	0.9 0.7 0.2		2.1 1.9 1.4	0.9 0.7 0.2		2.1 1.9 1.4	Volts

Notes:

1) Vt+(Vp) is the positive going threshold voltage.

2) Vt-(Vn) is the negative going threshold voltage.

3) Vh(ΔVt) is the hysteresis voltage

In UDMA modes greater than 4, the following characteristics apply. Voltage output high and low values shall be met at the source connector to include the effect of series termination.

Table 3-7 Input Characteristics (UDMA Mode > 4)

Parameter	Symbol	MIN	MAX	Units
DC supply voltage to receivers	V_{DD3}	3.3 - 8%	3.3 + 8%	Volts
Low to high input threshold	V+	1.5	2.0	Volts
High to low input threshold	V–	1.0	1.5	Volts
Difference between input thresholds: $((V+_{current\ value}) - (V-_{current\ value}))$	V_{HYS}	320		mV
Average of thresholds: $((V+_{current\ value}) + (V-_{current\ value}))/2$	V_{THRAVG}	1.3	1.7	Volts

3.3.2 Output Drive Type and Characteristics

In Table 3-8 "x" refers to the characteristics described in Table 3-8. For example–"OT3" refers to Totempole output with a Type 3 output drive characteristic.

Table 3-8 Output Drive Type

Type	Output Type	Valid Conditions
OTx	Totempole	Ioh & Iol
OZx	Tri-state N-P Channel	Ioh & Iol
OPx	P-Channel Only	Ioh only
ONx	N-Channel Only	Ioh Only

Table 3-9 Output Drive Characteristics

Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
1	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	2.4V		 0.4V	Volts

2	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	2.4V		 0.4V	Volts
3	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	2.4V		 0.4V	Volts
X	Tri-State Leakage Current	Ioz	Vol = Gnd Voh = Vcc	-10		10	µA

In UDMA modes greater than 4, the characteristics specified in the following table apply. Voltage output high and low values shall be met at the source connector to include the effect of series termination.

Table 3-10 Output Drive Characteristics (UDMA Mode > 4)

Parameter	Symbol	MIN	MAX	Units
DC supply voltage to drivers	V_{DD3}	3.3 - 8%	3.3 + 8%	Volts
Voltage output high at -6 mA to +3 mA (at V_{oH2} the output shall be able to supply and sink current to V_{DD3})	V_{oH2}	VDD_3 - 0.51	VDD_3 + 0.3	Volts
Voltage output low at 6 mA	V_{oL2}		0.51	Volts

Notes:

1) I_{oLDASP} shall be 12 mA minimum to meet legacy timing and signal integrity.

2) I_{oH} value at 400 µA is insufficient in the case of DMARQ that is pulled low by a 5.6 kΩ resistor.

3) Voltage output high and low values shall be met at the source connector to include the effect of series termination.

4) A device shall have less than 64 µA of leakage current into a 6.2 KΩ pull-down resistor while the INTRQ signal is in the released state.

4 ATA Command Set

The following table defines the complete list of commands supported by the CompactFlash card. Specifics of each command's operation can be found in the CF+ & CF SPECIFICATION REV. 4.1.

Table 5-1 Primary and Secondary I/O Decoding

Class	Command	Code
1	Check Power Mode	E5h or 98h
1	Execute Drive Diagnostic	90h
1	Erase Sector(s)[a]	C0h
2	Format Track	50h
1	Identify Device	ECh
1	Idle	E3h or 97h
1	Idle Immediate	E1h or 95h
1	Initialize Drive Parameters	91h
1	Read Buffer	E4h
1	Read DMA	C8 or C9
1	Read Multiple	C4h
1	Read Sector(s)	20h or 21h
1	Read Verify Sector(s)	40h or 41h
1	Recalibrate	1Xh
1	Request Sense[b]	03h
1	Seek	7Xh
1	Set Features	EFh
1	Set Multiple Mode	C6h
1	Set Sleep Mode	E6h or 99h
1	Stand By	E2h or 96h
1	Stand By Immediate	E0h or 94h
1	Translate Sector	87h
1	Wear Level	F5h
2	Write Buffer	E8h
2	Write DMA	CA or CB
3	Write Multiple	C5h
3	Write Multiple w/o Erase	CDh
2	Write Sector(s)	30h or 31h
2	Write Sector(s) w/o Erase	38h
2	Write Verify	3Ch

5 Identify Device–ECH

The following table defines the specifics of the Identify Data returned by the CompactFlash card. Specifics of each word can be found in the CF+ & CF SPECIFICATION REV. 4.1.

Table 5-8 Identify Device Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General configuration bit-significant information
	0XXX	2	General configuration – Bit Significant with ATA-4 definitions.
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0000h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	XXXXh	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (right justified)
20	0000h	2	Obsolete
21	0000h	2	Obsolete
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	Firmware revision in ASCII (Rev M.ms) set by code Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (left justified) Big Endian Byte Order in Word
47	000Xh	2	Maximum of 1 sector on Read/Write Multiple command
48	0000h	2	Reserved
49	XX00h	2	Capabilities
50	0000h	2	Reserved

Table 5-8 Identify Device Information

Word Address	Default Value	Total Bytes	Data Field Type Information
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Single word DMA data transfer cycle timing mode (not supported)
53	0003h	2	Field validity
54	XXXXh	2	Current number of cylinders
55	XXXXh	2	Current number of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	010Xh	2	Multiple sector setting is valid
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Single word DMA transfer (not supported)
63	0X07h	2	0-7: Multiword DMA modes supported 15-8: Multiword DMA mode active
64	0003h	2	Advanced PIO modes supported
65	0078h (IDE Mode only)	2	Minimum multiword DMA transfer cycle time per word in ns
66	0078h (IDE Mode only)	2	Recommended multiword DMA transfer cycle time per word in ns
67	0078h	2	Minimum PIO transfer without flow control
68	0078h	2	Minimum PIO transfer with IORDY flow control
69-79	0000h	20	Reserved
80	00XXh	2	Major ATA version
81	0000h	2	Minor ATA version
82	00X0h	2	Features/command sets supported
83	4004h	2	Features/command sets supported
84	4000h	2	Features/command sets supported
85	0000h	2	Features/command sets enabled
86	0004h	2	Features/command sets enabled
87	4000h	2	Features/command sets enabled
88	XXXXh	2	Ultra DMA Mode supported and selected
89	XXXXh	2	Time required for security erase-unit completion
90	0000h	2	Time required for enhanced security erase-unit completion
91	XXXXh	2	Current advanced power management value
92-127	0000h	72	Reserved
128-159	0000h	64	Reserved vendor-unique bytes
160	0000h	2	Power requirement description
161	0000h	2	Reserved for assignment by the CFA
162	0000h	2	Key management schemes supported

Table 5-8 Identify Device Information

Word Address	Default Value	Total Bytes	Data Field Type Information
163	XXXXh	2	CF Advanced True IDE Timing Mode Capability and Setting
164	XXXXh	2	CF Advanced PCMCIA I/O and Memory Timing Mode Capability
165-175	0000h	22	Reserved for assignment by the CFA
176-255	0000h	140	Reserved

a. Multiword DMA is supported by SanDisk PCMCIA. For all unsupported cases, 0100H is reported in word 49, and 0000H is reported in words 52, 63, and 65. CompactFlash products will support multi-word.

6 CIS Description

This section describes the Card Information Structure (CIS) for SanDisk CompactFlash Memory cards.

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
000h	01h	CISTPL_DEVICE								Device Info Tuple	Tuple Code
002h	04h									Link is 4 bytes	Link to next tuple
004h	DFh	Dev ID Type Dh = I/O				W 1	Speed 7h = Ext			I/O Device, Wait State, Extended Speed	Device ID, WPS, Speed
006h	12h	X	Speed Mantissa = 2h				Speed Exponent = 2h			120 ns if no wait	Extended Speed
	79h Extreme III	X	Speed Mantissa = Fh				Speed Exponent = 1h			80 ns if no wait	Extended Speed
008h	01h	# Address Unit – 1 = 1x					Side Code = 2k units			(One) 2 kB of Address Space	Device Size
00Ah	FFh	List End Marker								End of Devices	End Marker
00Ch	1Ch	CISTPL_DEVICE_OC								Other Conditions Info Tuple	Tuple Code
00Eh	04h									Link is 4 Bytes	Link to Next Tuple
010h	03h	Reserved = 0					V_{CC}		W A I T	Conditions: 3V operation is allowed and WAIT is used	3 V Operation, Wait Function
012h	D9h	Dev ID Type Dh = I/O				W 1	Speed = 1h			I/O Device, WPS, Speed = 250 ns	Device ID, WPS, Speed
014h	01h	# Address Unit – 1 = 1x					Side Code = 2k units			2 kB of Address Space	Device Size
016h	FFh	List End Marker								End of Devices	End Marker
018h	18h	CISTPL_JEDEC_C								JEDEC ID Common Memory	Tuple Code
01Ah	02h									Link is 2 bytes	Link Length
01Ch	DFh	PCMCIA JEDEC Manufacturer's ID								First byte of JEDEC ID for SanDisk PC Card ATA 12V	Byte 1, JEDEC ID of Device 1 (0-2K)
01Eh	01h	PCMCIA Code for PC Card-ATA No Vpp Required								Second Byte of JEDEC ID	Byte 2, JEDEC ID
020h	20h	CISTPL_MANFID								Manufacturer's ID Tuple	Tuple Code
022h	04h									Link is 4 bytes	Link Length
024h	45h	Low Byte of PCMCIA Manufacturer's Code								SanDisk JEDEC Manufacturer's ID	Low Byte of PCMCIA Mfg ID

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
026h	00h	High Byte of PCMCIA Manufacturer's Code								Code of 0 because other byte is JEDEC 1 byte Manufacturer's ID	High Byte of PCMCIA Mfg ID
028h	01h	Low Byte of Product Code								SanDisk Code for SDP Series	Low Byte Product Code
02Ah	04h	High Byte of Product Code								SanDisk Code for PC Card ATA	High Byte Product Code
02Ch	15h	CISTPL_VER_1								Level 1 Version/Product Info	Tuple Code
02Eh	17h									Link to next tuple is 23 bytes	Link Length
030h	04h	TPPLV1_MAJOR								PCMCIA 2.0/JEIDA 4.1	Major Version
032h	01h	TPPLV1_MINOR								PCMCIA 2.0/JEIDA 4.1	Minor Version
034h	53h	ASCII Manufacturer String								'S'	String 1
036h	61h									'a'[a]	
038h	6Eh									'n'	
03Ah	44h									'D'	
03Ch	69h									'i'	
03Eh	73h									's'	
040h	6Bh									'k'	
042h	00h	End of Manufacturer String								Null Terminator	
044h	53h	ASCII Product Name String								'S'	Info String 2
046h	44h									'D'	
048h	50h									'P'	
04Ah	00h	End of Product Name String								Null Terminator	
04Ch	35h									'5'	Info String 3
04Eh	2Fh									'/'	
050h	33h									'3'	
052h	20h									' '	
054h	30h	SanDisk Card CIS Revision Number								'0'	
056h	2Eh									'.'	
058h	36h									'6'	
05Ah	00h	End of CIS Revision Number								Null Terminator	
05Ch	FFh	End of List Marker								FFh List Terminator	No Info String 4
05Eh	80h	CISTPL_VEND_SPECIF_80								SanDisk Parameters Tuple	Tuple Code
060h	03h	(Field Bytes 3-4 taken as 0)								Link Length is 3 Bytes	Link to Next Tuple and Length of Info in this Tuple

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
062h	14h	W 0	12 0	NI 1	PP 1	PDNA 0	R I A 1	R I R 0	SP 0	No Wear Level & NO V_{pp} W: No Wear Level 12: Vpp not used on Write NI: -INPACK connected PP: Programmable Power PDNA: Pwr Down Not Abort--Cmd RIA: RBsy, ATBsy connected RIR: RBsy Inhibited at Reset SP: No Security Present This definition applies only to cards with Manufacturer's ID tuple 1st 3 bytes 45 00 01.	SanDisk Fields, 1 to 4 Bytes limited by link length
064h	08h	R 0	R 0	R 0	R 0	E 1	TPR 0	TAR 0	R8 0	R8: 8 bit ROM present TAR: Temp Bsy on AT Reset TPR: Temp Bsy on PCMCIA – Reset E: Erase Ahead Avail-able R: Reserved, 0 for now This definition applies only to cards with Manufacturer's ID tuple 1st 3 bytes 45 00 01.	SanDisk Fields, 1 to 4 bytes limited by link length
066h	00h										For specific platform use only
068h	21h	CISTPL_FUNCID								Function ID Tuple	Tuple Code
06Ah	02h									Link Length is 2 Bytes	Link to Next Tuple
06Ch	04h	Function Type Code								Disk Function	Function Code
06Eh	01h	R 0	R 0	R 0	R 0	R 0	R 0	R 0	P 1	Attempt installation at POST: P: Install at POST R: Reserved (0)	
070h	22h	CISTPL_FUNCE								Function Extension Tuple	Tuple Code
072h	02h									Link Length is 2 Bytes	Link to Next Tuple

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
074h	01h	Disk Function Extension Tuple Type								Extension Tuple describes the Interface Protocol	Extension Tuple Type for Disk
076h	01h	Interface Type Code								PC Card–ATA Interface	Extension Info
078h	22h	CISTPL_FUNCE								Function Extension tuple	Tuple Code
07Ah	03h									Tuple has 3 Info Bytes	Link Length
07Ch	02h	Disk Function Extension Tuple Type								Basic PCMCIA-ATA Extension Tuple	Extension Tuple Type for Disk
07Eh	0Ch	R 0	R 0	R 0	R 0	U 1	S 1	V 0		Unique Manufacturer/ Serial Number combined string: V = 0: No Vpp Required V = 1: Vpp on Modified Media V = 2: Vpp on Any Operation V = 3: Vpp Continuous S: Silicon, else Rotating Drive U: ID Drive Mfg/SN Unique	Basic ATA Option Parameters
080h	0Fh	R 0	I 0	E 0	N 0	P3 1	P2 1	P1 1	P0 1	All power-down modes and power commands are not needed to minimize power. P0: Sleep Mode Supported P1: Standby Mode Supported P2: Idle Mode Supported P3: Drive Auto Power Control N: Some Config Excludes 3X7 E: Index Bit is Emulated I: Twin–-IOis16 Data Reg Only	Extended ATA Option Parameters
082h	1Ah	CISTPL_CONF								Configuration Tuple	Tuple Code
084h	05h									Link Length is 5 Bytes	Link to Next Tuple

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
086h	01h	RFS 00			RMS 00		RAS 01			Size of Reserved Field is 0 Bytes Size of Register Mask is 1 Byte Size of Config Base Address is 2 Bytes RFS: Bytes in Reserved Field RMS: Bytes in Reg Mask–1 RAS: Bytes in Base Addr–1	Size of Fields Byte (TPCC_SZ)
088h	07h	TPCC_LAST								Entry with Config Index 07h is final entry in table	Last Entry of Config. Table
08Ah	00h	TPCC_RADR (LSB)								Configuration Registers located at 200h in Reg. Space	Location of Config. Registers
08Ch	02h	TPCC_RADR (MSB)									
08Eh	0Fh	R 0	R 0	R 0	R 0	S 1	P 1	C 1	I 1	First (4) Configuration Registers are present: I: Configuration Index C: Configuration and Status P: Pin Replacement S: Socket and Copy R: Reserved for future use	TPCC_RMSK
090h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
092h	0Bh									Link to Next Tuple is 11 Bytes. Also limits size of this tuple to 13 bytes.	Link to Next Tuple
094h	C0h	I 1	D 1	Configuration Index 0						Memory Mapped I/O Configuration Configuration Index for this entry is 0. Interface Byte follows this byte. Default Configuration, so is not dependent on previous Default Configuration. D: Default Configuration I: Interface Byte follows	TPCE_INDX

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
096h	C0h	W 1	R 1	P 0	B 0	Interface Type				Memory Only Interface(0), Bvd's and wProt not used, Ready/-Busy and Wait for memory cycles active. B: Battery Volt Detects Used P: Write Protect Used R: Ready/-Busy Used W: Wait Used for Memory Cycles	TPCE_IF
098h	A1h	M 1	MS 1		IR 0	IO 0	T 0	P 1		V_{CC} only Power; No Timing, I/O, or IRQ; 2 Byte Memory Space Length; Misc Entry Present. P: Power Info type T: Timin Info present IO: I/O Port Info present IR: Interrupt Info present MS: Mem Space Info type M: Misc Info Byte(s) present	TPCE_FS
09Ah	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage follows: NV: Nominal Voltage LV: Mimimum Voltage HB: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for V_{CC}
09Ch	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			V_{CC} Nominal is 5 V	V_{CC} Nominal Value
09Eh	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V			V_{CC} Nominal is 4.5 V	V_{CC} Min. Value
0A0h	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V			V_{CC} Nominal is 5.5 V	V_{CC} Max. Value
0A2h	75h	X 0	Mantissa Eh = 8.0				Exponent 5h = 10			Max. Average Current over 10 ms is 80 mA	Max. Average Current
0A4h	08h	Length in 256 Bytes Pages (LSB)								Length of Memory Space is 2 kB	TPCE_MS Length LSB
0A6h	00h	Length in 256 Bytes Pages (MSB)								Start at 0 on card	TPCE_MS Length MSB

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
0A8h	21h	X 0	R 0	P 1	RO 0	A 0	T 1			Power-Down and Twin Card. T: Twin Cards Allowed A: Audio Supported RO: Read Only Mode P: Power Down Supported R: Reserved X: More Miscellaneous Fields Bytes	TPCE_MI
0AAh	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0ACh	06h									Link to Next Tuple is 6 Bytes. Also limits size of this tuple to 8 bytes.	Link to Next Tuple
0AEh	00h	I 0	D 0	Configuration Index 0						Memory Mapped I/O 3.3V Configuration.	TPCE_INDX
0B0h	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P: Power Info type	TPCE_FS
0B2h	21h	R 0	DI 0	PI 1	AI 0	SI 0	H 0	LV 0	NV 1	PI: Peak Current NV: Nominal Operation Supply Voltage	TPCE_PD
0B4h	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 10			Nominal Operation Supply Voltage = 3.0V	Nominal Operation Supply Voltage
0B6h	1Eh	X 0	1Eh							+.30	Nominal Operation Supply Voltage Extension Byte
0B8h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max. Average Current over 10 ms is 45 mA	Max. Average Current
0BAh	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0BCh	0Dh									Link to Next Tuple is 13 Bytes. Also limits size of this tuple to 15 bytes.	Link to Next Tuple

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
0BEh	C1h	I 1	D 1	Configuration Index 1						I/O Mapped Contiguous 16 Registers Configuration. Configuration Index for this entry is 1. Interface Byte follows this byte. Default Configuration, therefore is not dependent on previous Default Configuration. D: Default Configuration I: Interface Byte follows	TPCE_INDX
0C0h	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B: Battery Volt Detects Used P: Write Protect Used R: Ready/-Busy Used W: Wait Used for Memory Cycles	TPCE_IF
0C2h	99h	M 1	MS 0		IR 1	IO 1	T 0	P 1		V_{CC} Only Power Descriptors; No Timing; I/O and IRQ present; No Memory Space; Misc Entry Present P: Power Info type T: Timing Info present IO :I/O Port Info present IR: Interrupt Info present MS: Memory Space Info type M: Misc Info Byte(s) present	TPCE_FS
0C4h	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV: Nominal Voltage LV: Mimimum Voltage HB: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for V_{CC}
0C6h	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			V_{CC} Nominal is 5V	V_{CC} Nominal Value

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
0C8h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V			V_{CC} Nominal is 4.5V	V_{CC} Min. Value
0CAh	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V			V_{CC} Nominal is 5.5V	V_{CC} Max. Value
0CCh	75h	X 0	Mantissa Eh = 8.0				Exponent 5h = 10			Max. Average Current over 10 ms is 80 mA	Max. Average Current
0CEh	64h	R 0	S 1	E 1	IO AddeLines 4					Supports both 8 and 16 bit I/O hosts. 4 Address lines & no range so 16 registers and host must do all of the selection decoding. IO AddrLines:#lines decoded. E: 8-bit Only Hosts Supported S: 16-bit Hosts Supported R: Range follows	TPCE_IO
0D0h	F0h	S 1	P 1	L 1	M 1	V 0	B 0	I 0	N 0	IRQ Sharing Logic Active in Card Control & Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S: Share Logic Active P: Pulse Mode IRQ Supported L: Level Mode IRQ Supported M: Bit Mask of IRQs Present V: Vendor Unique IRQ B: Bus Error IRQ I: IO Check IRQ N: Non-Maskable IRQ	TPCE_IR
0D2h	FFh	7 1	6 1	5 1	4 1	3 1	2 1	1 1	0 1	IRQ Levels to be routed 0 - 15 recommended.	TPCE_IR Mask Extension Byte 1
0D4h	FFh	F 1	E 1	D 1	C 1	B 1	A 1	9 1	8 1	Recommended routing to any "normal, maskable" IRQ.	TPCE_IR Mask Extension Byte 2

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
0D6h	21h	X 0	R 0	P 1	RO 0	A 0	T 1			Power-Down and Twin Card. T: Twin Cards Allowed A: Audio Supported RO: Read Only Mode P: Power Down Supported R: Reserved X: More Misc Fields Bytes	TPCE_MI
0D8h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0DAh	06h									Link to Next Tuple is 6 Bytes. Also limits size of this tuple to 8 bytes.	Link to Next Tuple
0DCh	01h	I 0	D 0	Configuration Index 1						I/O Mapped Contiguous 16 3.3V Configuration	TPCE_INDX
0DEh	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P: Power Info type	TPCE_FS
0E0h	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	PI: Peak Current NV: Nominal Operation Supply Voltage	Power Parameters for VCC
0E2h	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V	Nominal Operation Supply Voltage
0E4h	1Eh	X 0	1Eh							+.30	Nominal Operation Supply Voltage Extension Byte
0E6h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max. Average Current over 10 ms is 45 mA	Max. Average Current
0E8h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
0EAh	12h									Link to Next Tuple is 18 Bytes. Also limits size of this tuple to 20 bytes	Link to Next Tuple
0ECh	C2h	I 1	D 1	Configuration Index 2						AT Fixed Disk Primary I/O Address Configuration Configuration Index for this entry is 2. Interface Byte follows this byte. Default Configuration	TPCE_INDX

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
0EEh	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles . B: Battery Volt Detects Used P: Write Protect Used R: Ready/-Busy Used W: Wait Used for Memory Cycles	TPCE_IF
0F0h	99h	M 1	MS 0		IR 1	IO 1	T 0	P 1		V_{CC} Only Power Description; No Timing; I/O and IRQ present; No Memory Space; Misc Entry present. P: Power Info type T: Timing Info present IO: I/O Port Info present IR: Interrupt Info present MS: Memory Space Info type M: Misc Info Byte(s) present	TPCE_FS
0F2h	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage follows: NV: Nominal Voltage LV: Mimimum Voltage HB: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for V_{CC}
0F4h	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			V_{CC} Nominal is 5V	V_{CC} Nominal Value
0F6h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V			V_{CC} Nominal is 4.5V	V_{CC} Min. Value
0F8h	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V			V_{CC} Nominal is 5.5V	V_{CC} Max. Value
0FAh	75h	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max. Average Current over 10 ms is 80 mA	Max. Average Current

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
0FCH	EAh	R 1	S 1	E 1	IO AddeLines Ah = 10					Supports both 8- and 16-bit I/O hosts. 10 Address Lines with range so card will respond only to indicated (1F0-1F7, 3F6-3F7) on A9 through A0 for I/O cycles. IO AddrLines:#lines decoded E: 8-bit Only Hosts Supported S: 16-bit Hosts Supported R: Range follows	TPCE_IO
0FEh	61h	LS 1		AS 2	N Ranges - 1 1					Number of Ranges is 2; Size of each address is 2 bytes; size of each length is 1 byte. AS: Size of Addresses 0: No Address Present 1: 1Byte (8 bit) Addresses 2: 2Byte (16 bit) Addresses 3: 4Byte (32 bit) Addresses LS: Size of length 0: No Lengths Present 1: 1Byte (8 bit) Lengths 2: 2Byte (16 bit) Lengths 3: 4Byte (32 bit) Lengths	I/O Range Format Description
100h	F0h	1st I/O Base Address (isb)								First I/O Range Base is 1F0h	
102h	01h	1st I/O Base Address (msb)									
104h	07h	1st I/O Range Length – 1								8 Bytes Total ➔ 1F0-1F7h	I/O Length -1
106h	F6h	2nd I/O Base Address (isb)								2nd I/o Range base is 3F6h	
108h	03h	2nd I/O Base Address (msb)									
10Ah	01h	2nd I/O Range Length – 1								2 Bytes Total ➔ 3F6-3F7h	I/O Length-1

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
10Ch	EEh	S 1	P 1	L 1	M 0	Recommend IRQ Level Eh = 14				IRQ Sharing Logic Active in Card Control & Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S: Share Logic Active P: Pulse Mode IRQ Supported L: Level Mode IRQ Supported M: Bit Mask of IRQs Present M=0 so bits 3-0 are single level, binary encoded	TPCE_IR
10Eh	21h	X 0	R 0	P 1	RO 0	A 0	T 1			Power-Down and Twin Card. T: Twin Cards Allowed A: Audio Supported RO: Read Only Mode P: Power Down Supported R: Reserved X: More Misc Fields Bytes	TPCE_MI
110h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
112h	06h									Link to Next Tuple is 6 Bytes. Also limits size of this tuple to 8 bytes.	Link to Next Tuple
114h	02h	I 0	D 0	Configuration Index 2						AT Fixed Disk Primary I/O 3.3V Configuration	TPCE_INDX
116h	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P: Power Info type	TPCE_FS
118h	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV	NV 1	PI: Peak Current NV: Nominal Operation Supply Voltage	Power Parameters for V_{CC}
11AH	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V	Nominal Operation Supply Voltage

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
11Ch	1Eh	X 0	1Eh							+.30	Nominal Operation Supply Voltage Extension Byte
11Eh	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max. Average Current over 10 ms is 45 mA	Max. Average Current
120h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
122h	12h									Link to Next Tuple is 18 Bytes. Also limits size of this tuple to 20 bytes.	Link to Next Tuple
124h	C3h	I 1	D 1	Configuration Index 3						AT Fixed Disk Secondary I/O Address Configuration Configuration Index for this entry is 3. Interface Byte follows this byte. Default Configuration	TPCE_INDX
126h	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B: Battery Volt Detects Used P: Write Protect Used R: Ready/-Busy Used W: Wait Used for Memory Cycles	TPCE_IF
128h	99h	M 1	MS 0		IR 1	IO 1	T 0	P 1		V_{CC}-Only Power Descriptors; No Timing; I/O and IRQ present; No Memory Space; Misc Entry Present. P: Power Info type T: Timing Info present IO: I/O Port Info present IR: Interrupt Info present MS: Memory Space Info type M: Misc Info Byte(s) present	TPCE_FS

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
12Ah	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV: Nominal Voltage LV: Mimimum Voltage HB: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for V_{CC}
12Ch	55h	X 0	Mantissa Ah = 5.0				Exponent 5h = 1V			V_{CC} Nominal is 5V	V_{CC} Nominal Value
12Eh	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 1V			V_{CC} Nominal is 4.5V	V_{CC} Min. Value
130h	5Dh	X 0	Mantissa Bh = 5.5				Exponent 5h = 1V			V_{CC} Nominal is 5.5V	V_{CC} Max. Value
132h	75h	X 0	Mantissa Eh = 1.0				Exponent 5h = 10			Max. Average Current over 10 ms is 80 mA	Max. Average Current
134h	EAh	R 1	S 1	E 1	IO AddeLines \Ah = 10					Supports both 8- and 16-bit I/O hosts. 10 Address Lines with Range so card will respond only to indicated (170-177, 376377) on A9 through A0 for I/O cycles. IO AddrLines:#lines decoded E: 8-bit Only Hosts Supported S: 16-bit Hosts Supported R: Range follows	TPCE_IO

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
136h	61h	LS 1		AS 2		N Ranges–1 1				Number of Ranges is 2; Size of each address is 2 bytes; size of each length is 1 byte. AS: Size of Addresses 0: No Address Present 1: 1Byte (8 bit) Addresses 2: 2Byte (16 bit) Addresses 3: 4Byte (32 bit) Addresses LS: Size of length 0: No Lengths Present 1: 1Byte (8 bit) Lengths 2: 2Byte (16 bit) Lengths 3: 4Byte (32 bit) Lengths	I/O Range Format Description
138h	70h	1st I/O Base Address (LSB)								First I/O Range Base is 170h	
13Ah	01h	1st I/O Base Address (MSB)									
13Ch	07h	1st I/O Range Length -1								8 Bytes Total →170—177h	I/O Length-1
13Eh	76h	2nd I/O Base Address (LSB)								Second I/O Range Base is 376h	
140h	03h	2nd I/O Base Address (MSB)									
142h	01h	2nd I/O Range Length-1								2 Bytes Total →3766-377	I/O Length-1
144h	EEh	S 1	P 1	L 1	M 0	Recommend IRQ Level Eh = 14				IRQ Sharing Logic Active in Card Control & Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F). S: Share Logic Active P: Pulse Mode IRQ Supported L: Level Mode IRQ Supported M: Bit Mask of IRQs Present M=0 therefore bits 3-0 are single level, binary encoded	TPCE_IR

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
146h	21h	X 0	R 0	P 1	RO 0	A 0	T 1			Power-Down, and Twin Card. T: Twin Cards Allowed A: Audio Supported RO: Read Only Mode P: Power Down Supported R: Reserved X: More Misc Fields Bytes	TPCE_MI
148h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
14Ah	06h									Link to Next Tuple is 6 Bytes. Also limits size of this tuple to 8 bytes.	Link to Next Tuple
14Ch	03h	I 0	D 0	Configuration Index 3						AT Fixed Disk Secondary I/O 3.3V Configuration	TPCE_INDX
14Eh	01h	M 0	MS 0		IR 0	IO 0	T 0	P 1		P: Power Info type	TPCE_FS
150h	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	PI: Peak Current NV: Nominal Operation Supply Voltage	Power Parameters for V_{CC}
152h	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V	Nominal Operation Supply Voltage
154h	1Eh	X 0	1Eh							0.3	Nominal Operation Supply Voltage Extension Byte
156h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10			Max. Average Current over 10 ms is 45 mA	Max. Average Current
158H	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code
15Ah	04h									Link to Next Tuple is 4 bytes	Link to Next Tuple
15Ch	07h	I 0	D 0	Configuration Index 7						AT Fixed Disk Secondary I/O 3.3V Configuration	TPCE_INDX
15Eh	00h	M 0	MS 0		IR 0	IO 0	T 0	P 0		P: Power Info type	TPCE_FS
160h	028h									SanDisk Code	Reserved
162h	0D3h									SanDisk Code	Reserved

Table 6-1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Content Description	CIS Function
164h	014h	CISTPL_NO_LINK								Prevent scan of common memory	Tuple Code
166h	000h	No Bytes following								Link Length is 0 Bytes	Link to Next Tuple
168h	0FFh	End of Tuple Chain								End of CIS	Tuple Code

a. Legacy CompactFlash products may report “SunDisk” as the ASCII manufacture string

Appendix: Ordering Information

A1. SanDisk CompactFlash Memory Card[1]

SanDisk products directly from SanDisk, call (408) 801-1000.

Part Number	Product	Capacity	Capacity (formatted in bytes)	Sectors/Card (Max. LBA+1)	No. of Heads	No. of Sectors/ Tracks	No. of Cylinders
SDCFAA-004G	CF 200x	4GB	4,011,614,208	7,835,184	16	63	7,773
SDCFAA-008G	CF200x	8GB	8,012,309,400	15,649,200	16	63	15,525
SDCFAA-016G	CF200x	16GB	16,013,942,784	31,277,232	16	63	31,029
SDCFAB-008G	CF400x	8GB	8,012,309,400	15,649,200	16	63	15,525
SDCFAB-016G	CF400x	16GB	16,013,942,784	31,277,232	16	63	31,029
SDCFAB-032G	CF400x	32GB	32,017,047,552	62,553,296	16	63	62,037
SDCFAB-064G	CF400x	64GB	64,023,257,088	125,045,424	16	63	65,535

[1] 1 megabyte (MB) = 1 million bytes; 1 gigabyte (GB) = 1 billion bytes. Some of the listed capacity is used for formatting and other functions, and thus is not available for data storage.

