

International

IR Rectifier

RADIATION HARDENED

POWER MOSFET

THRU-HOLE (Low-Ohmic TO-254AA)

PD-94283E

IRHMS597160

JANSR2N7550T1

100V, P-CHANNEL

REF: MIL-PRF-19500/713

R5 TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	ID	QPL Part Number
IRHMS597160	100K Rads (Si)	0.05Ω	-45A	JANSR2N7550T1
IRHMS593160	300K Rads (Si)	0.05Ω	-45A	JANSF2N7550T1



International Rectifier's R5™ technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm²)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Identical Pre- and Post-Electrical Test Conditions
- Repetitive Avalanche Ratings
- Dynamic dv/dt Ratings
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Ceramic Eyelets
- Light Weight
- High Electrical Conductive Package

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
ID @ VGS = -12V, TC=25°C	Continuous Drain Current	-45	A
ID @ VGS = -12V, TC=100°C	Continuous Drain Current	-28.5	
IDM	Pulsed Drain Current ①	-180	
PD @ TC = 25°C	Max. Power Dissipation	208	W
	Linear Derating Factor	1.67	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	480	mJ
IAR	Avalanche Current ①	-45	A
EAR	Repetitive Avalanche Energy ①	20.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-6.0	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.063in./1.6mm from case for 10s)	
	Weight	9.3 (Typical)	g

For footnotes refer to the last page

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Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V _{GS} = 0V, I _D = -1.0mA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	-0.13	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.05	Ω	V _{GS} = -12V, I _D = -28.5A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -1.0mA
g _{fs}	Forward Transconductance	24	—	—	S	V _{DS} > -15V, I _{DS} = -28.5A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-10	μA	V _{DS} = -80V, V _{GS} = 0V
		—	—	-25		V _{DS} = -80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V _{GS} = 20V
Q _g	Total Gate Charge	—	—	170	nC	V _{GS} = -12V, I _D = -45A
Q _{gs}	Gate-to-Source Charge	—	—	65		V _{DS} = -50V
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	30		
t _{d(on)}	Turn-On Delay Time	—	—	35	ns	V _{DD} = -50V, I _D = -45A
t _r	Rise Time	—	—	100		V _{GS} = -12V, R _G = 1.2Ω
t _{d(off)}	Turn-Off Delay Time	—	—	100		
t _f	Fall Time	—	—	100		
L _S + L _D	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad
C _{iss}	Input Capacitance	—	6110	—	pF	V _{GS} = 0V, V _{DS} = -25V
C _{oss}	Output Capacitance	—	1574	—		f = 1.0MHz
C _{rss}	Reverse Transfer Capacitance	—	115	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-45	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	-180		
V _{SD}	Diode Forward Voltage	—	—	-5.0	V	T _j = 25°C, I _S = -45A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	200	ns	T _j = 25°C, I _F = -45A, di/dt ≤ -100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	1.6	μC	V _{DD} ≤ -50V ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	0.6	°C/W	
R _{thCS}	Case-to-Sink	—	0.21	—		
R _{thJA}	Junction-to-Ambient	—	—	48		Typical socket mount

Note: Corresponding Spice and Saber models are available on International Rectifier Website.

For footnotes refer to the last page

Radiation Characteristics

IRHMS597160, JANSR2N7550T1

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ $T_j = 25^\circ\text{C}$, Post Total Dose Irradiation ⑤⑥

	Parameter	100KRads(Si) ¹		300KRads(Si) ²		Units	Test Conditions
		Min	Max	Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	-100	—	V	$V_{GS} = 0V, I_D = -1.0mA$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	-4.0	-2.0	-5.0		$V_{GS} = V_{DS}, I_D = -1.0mA$
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	$V_{GS} = -20V$
I_{GSS}	Gate-to-Source Leakage Reverse	—	100	—	100		$V_{GS} = 20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	-10	—	-10	μA	$V_{DS} = -80V, V_{GS} = 0V$
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.05	—	0.05	Ω	$V_{GS} = -12V, I_D = -28.5A$
V_{SD}	Diode Forward Voltage ④	—	-5.0	—	-5.0	V	$V_{GS} = 0V, I_S = -45A$

1. Part number IRHMS597160 (JANSR2N7550T1)

2. Part number IRHMS593160 (JANSF2N7550T1)

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	V_{DS} (V)					
				@ $V_{GS}=0V$	@ $V_{GS}=5V$	@ $V_{GS}=10V$	@ $V_{GS}=15V$	@ $V_{GS}=17.5V$	@ $V_{GS}=20V$
Br	37.9	252.6	33.1	-100	-100	-100	-100	-100	-100
I	59.7	314	30.5	-100	-100	-100	-100	-75	-25
Au	82.3	350	28.4	-100	-100	-100	-30	—	—

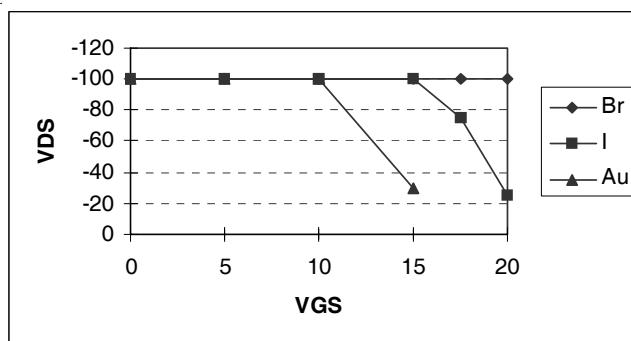


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

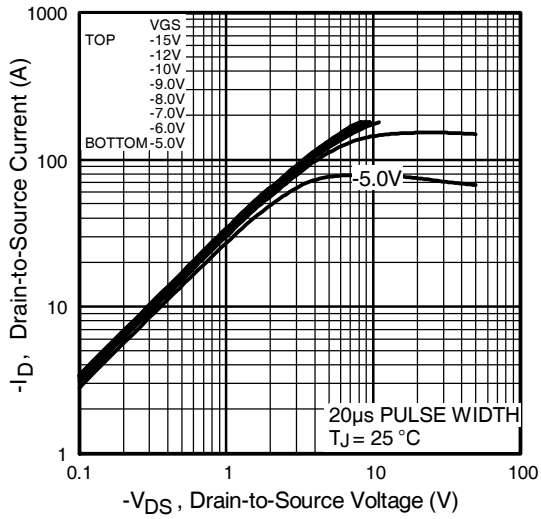


Fig 1. Typical Output Characteristics

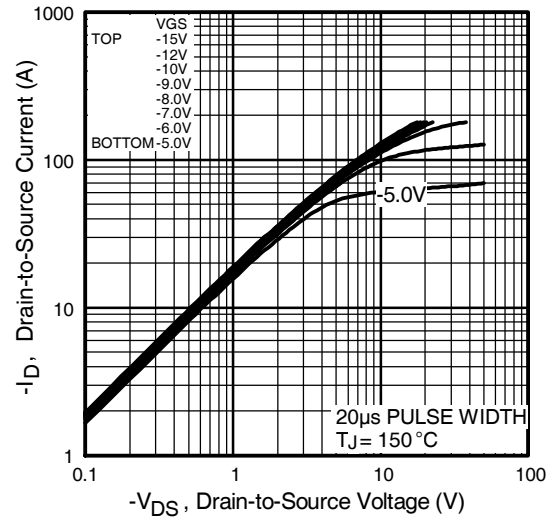


Fig 2. Typical Output Characteristics

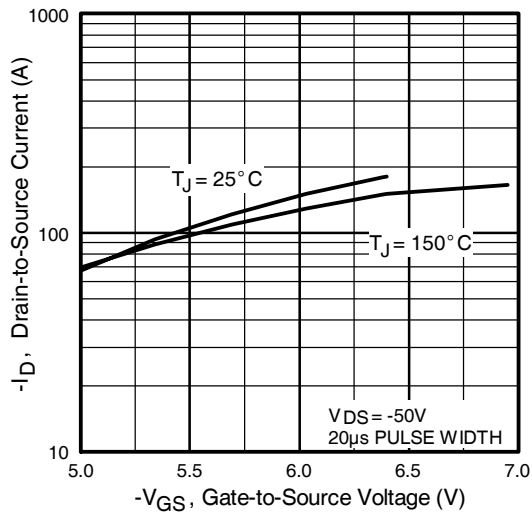


Fig 3. Typical Transfer Characteristics

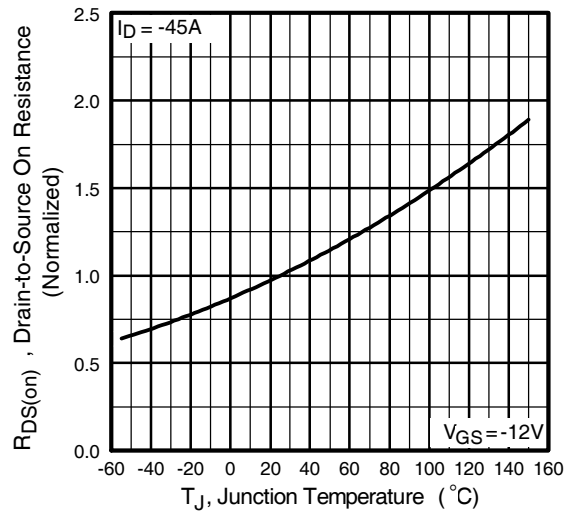


Fig 4. Normalized On-Resistance Vs. Temperature

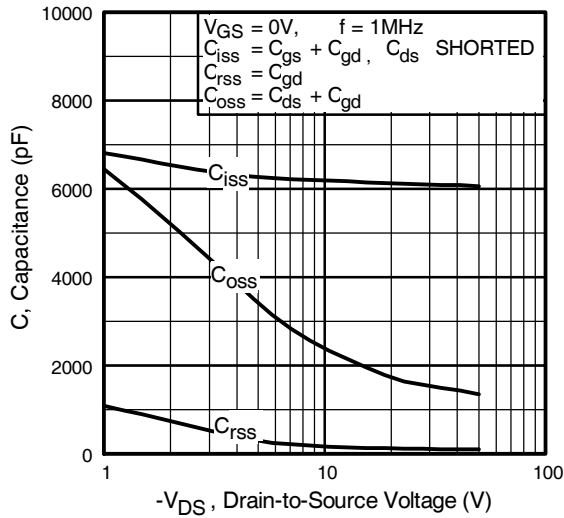


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

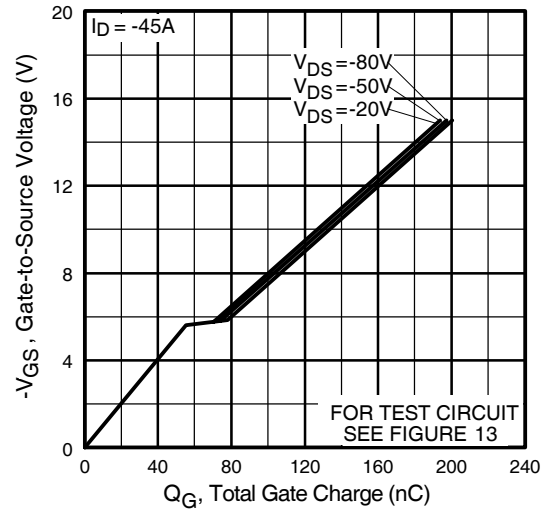


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

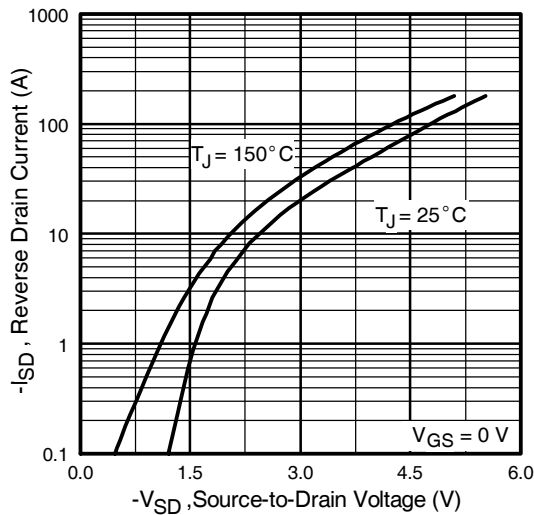


Fig 7. Typical Source-Drain Diode Forward Voltage

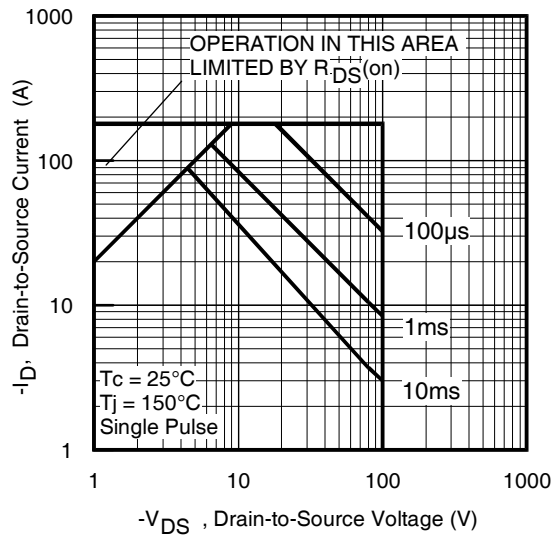


Fig 8. Maximum Safe Operating Area

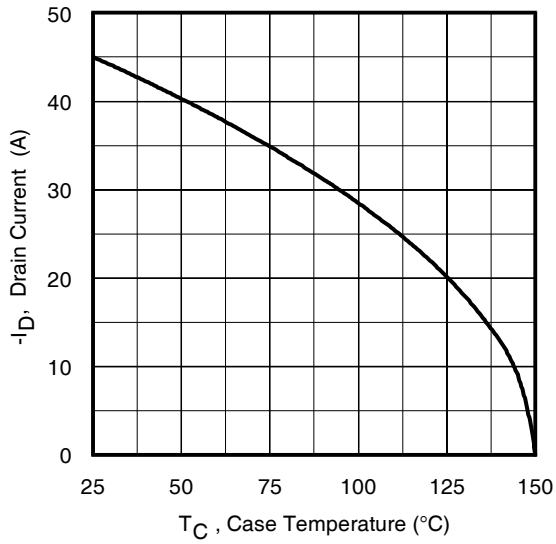


Fig 9. Maximum Drain Current Vs. Case Temperature

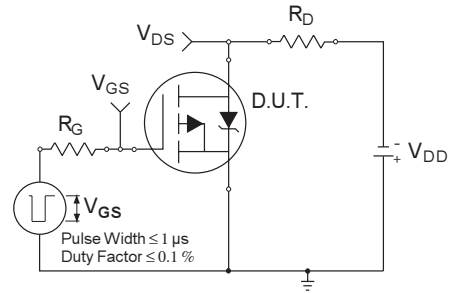


Fig 10a. Switching Time Test Circuit

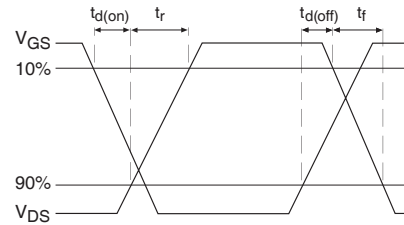


Fig 10b. Switching Time Waveforms

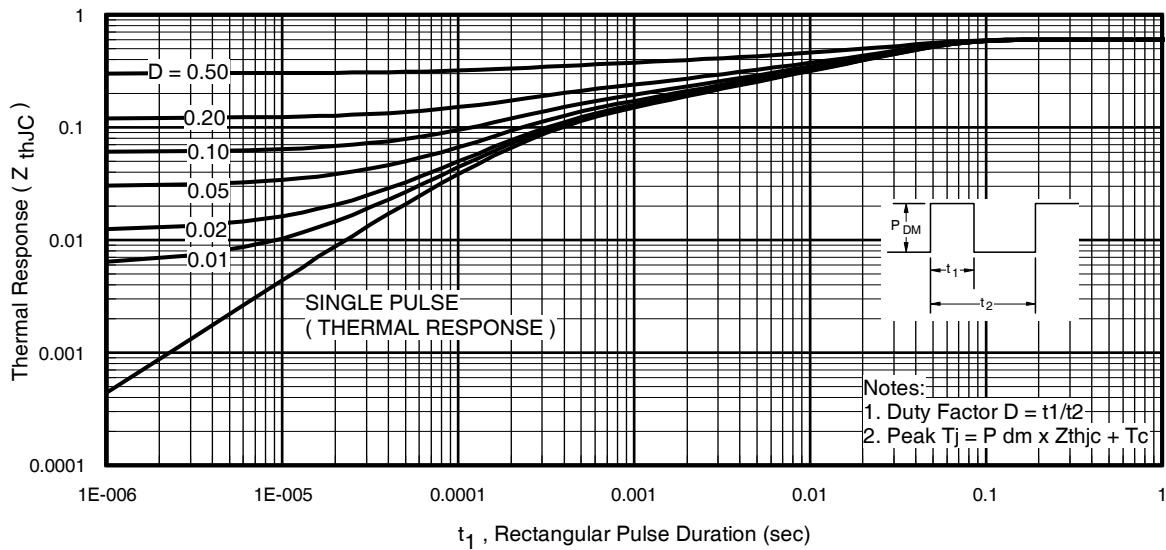


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

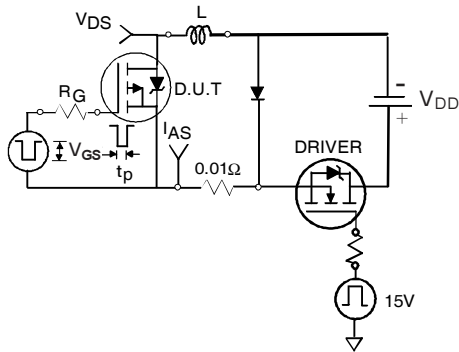


Fig 12a. Unclamped Inductive Test Circuit

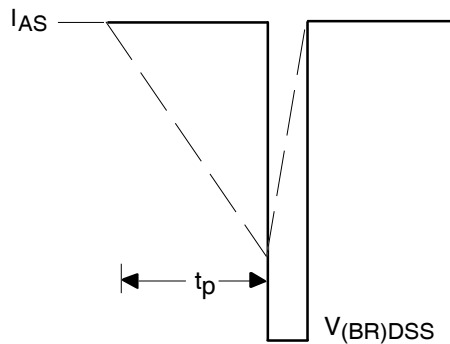


Fig 12b. Unclamped Inductive Waveforms

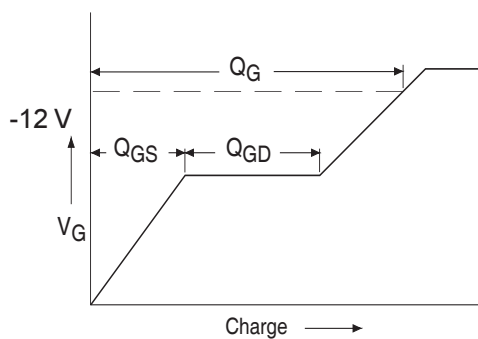


Fig 13a. Basic Gate Charge Waveform

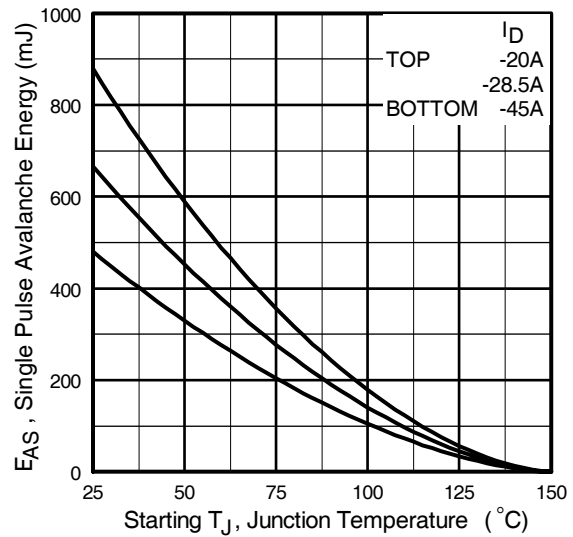


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

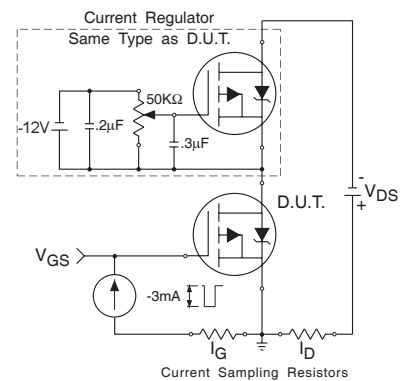
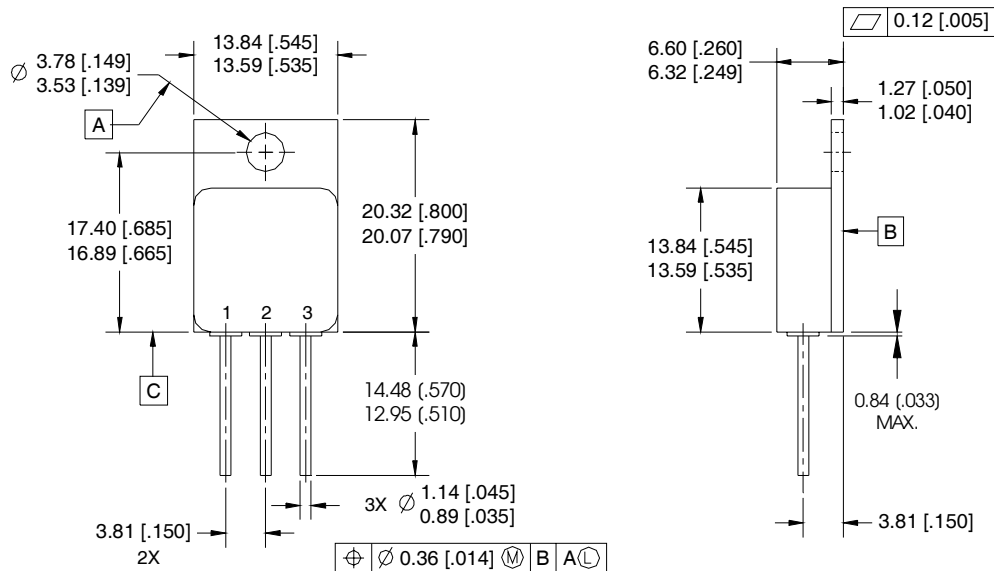


Fig 13b. Gate Charge Test Circuit

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -50V$, starting $T_J = 25^\circ C$, $L = 0.48mH$
Peak $I_L = -45A$, $V_{GS} = -12V$
- ③ $I_{SD} \leq -45A$, $di/dt \leq -365A/\mu s$,
 $V_{DD} \leq -100V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300\mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
-12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
-80 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — Low-Omic TO-254AA**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.

PIN ASSIGNMENTS

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

CAUTION**BERYLLIA WARNING PER MIL-PRF-19500**

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

International
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Data and specifications subject to change without notice. 12/2007