

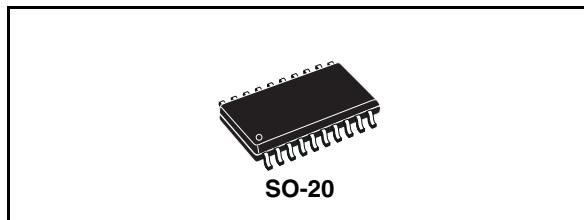
## 5-Bit programmable step down controller with synchronous rectification

### Features

- Operating supply IC voltage from 5V to 12V buses
- Up to 1.3A gate current capability
- TTL-compatible 5 bit programmable output compliant with VRM 8.5 : 1.050V to 1.825V with 0.025V binary steps
- Voltage mode PWM control
- Excellent output accuracy:  $\pm 1\%$  over line and temperature variations
- Very fast load transient response: from 0% to 100% Duty Cycle
- Power good output voltage
- Overvoltage protection and monitor
- Overcurrent protection realized using the upper MOSFET's  $R_{ds(ON)}$
- 200kHz internal oscillator
- Oscillator externally adjustable from 50kHz to 1MHz
- Soft start and inhibit functions

### Applications

- Power supply for advanced microprocessor core
- Distributed power supply



### Description

The device is a power supply controller specifically designed to provide a high performance DC/DC conversion for high current microprocessors. A precise 5 bit digital to analog converter (DAC) allows to adjust the output voltage from 1.050 to 1.825 with 25mV binary steps.

The high precision internal reference assures the selected output voltage to be within  $\pm 1\%$ . The high peak current gate drive affords to have fast switching to the external power mos providing low switching losses.

The device assures a fast protection against load overcurrent and load over-voltage. An external SCR is triggered to crowbar the input supply in case of hard overvoltage. An internal crowbar is also provided turning on the low side mosfet as long as the over-voltage is detected. In case of over-current detection, the soft start capacitor is discharged and the system works in HICCUP mode.

**Table 1. Device summary**

| Part Number | Package | Packaging     |
|-------------|---------|---------------|
| L6911E      | TSSOP8  | Tube          |
| L6911ETR    | TSSOP8  | Tape and reel |

## Contents

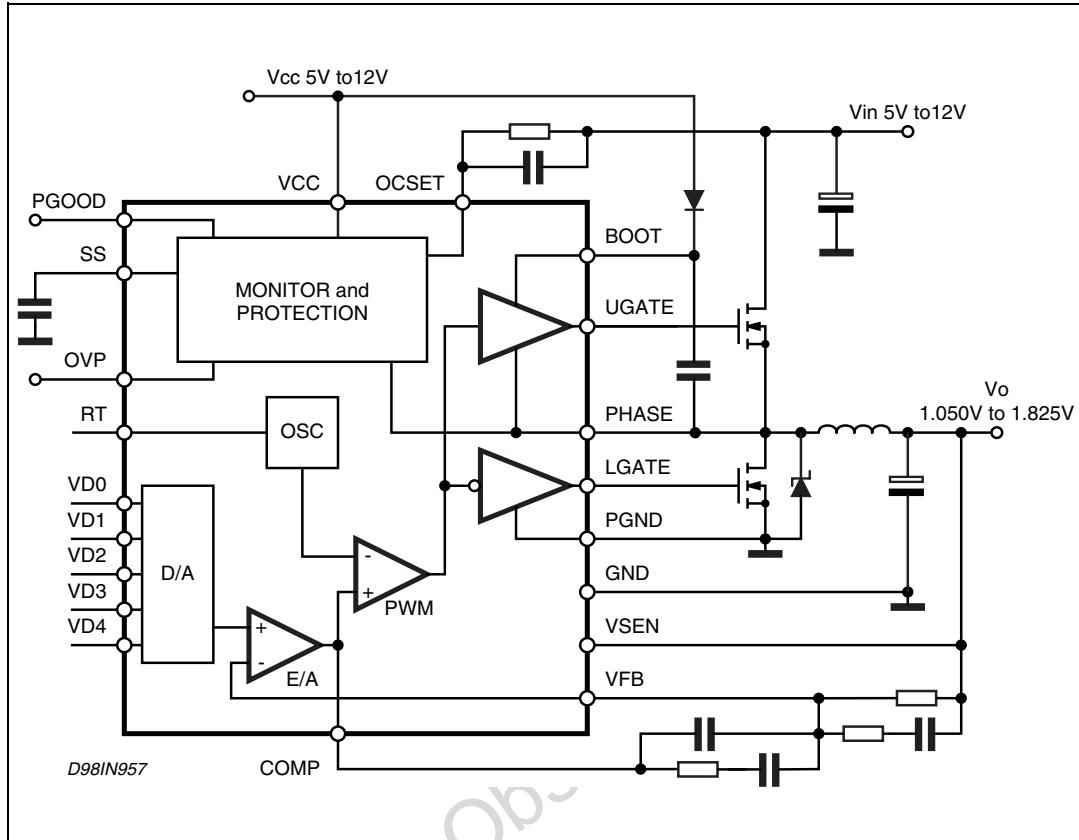
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Obsolete Product(s) - Obsolete Product(s)

# 1 Block diagram

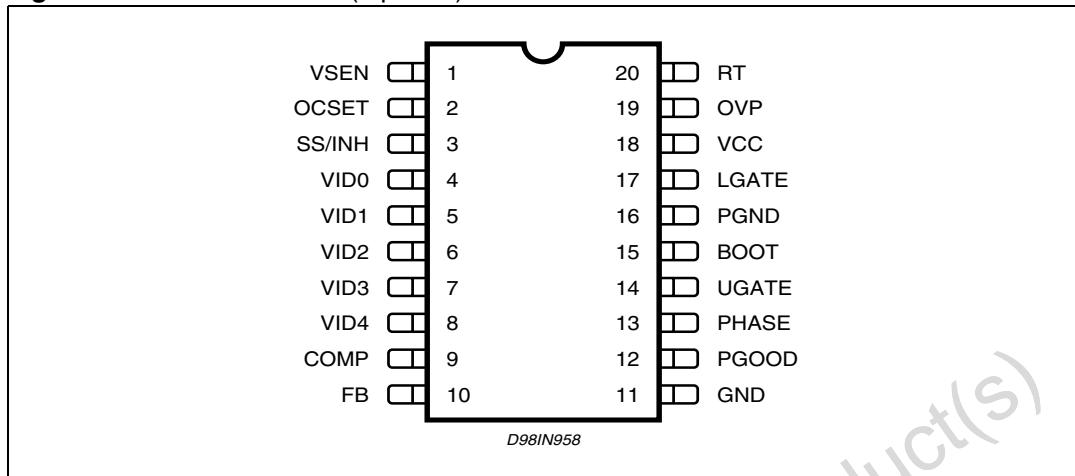
Figure 1. Block diagram



## 2 Pin settings

### 2.1 Pin connection

Figure 2. Pin connection (top view)



### 2.2 Pin description

Table 2. Pin description

| N°    | Name     | Description   |
|-------|----------|---|
| 1     | VSEN     | Connected to the output voltage is able to manage over-voltage conditions and the PGOOD signal.   |
| 2     | OCSET    | A resistor connected from this pin and the upper Mos Drain sets the current limit protection. The internal 200 $\mu$ A current generator sinks a current from the drain through the external resistor. The Over-Current threshold is due to the following equation:<br>$I_P = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{DSon}}$ |
| 3     | SS/INH   | The soft start time is programmed connecting an external capacitor from this pin and GND. The internal current generator forces through the capacitor 10 $\mu$ A.<br>This pin can be used to disable the device forcing a voltage lower than 0.4V   |
| 4 - 8 | VID0 - 4 | Voltage Identification Code pins. These input are internally pulled-up and TTL compatible. They are used to program the output voltage as specified in <a href="#">Table 6 on page 9</a> and to set the overvoltage and power good thresholds. Connect to GND to program a '0' while leave floating to program a '1'.     |
| 9     | COMP     | This pin is connected to the error amplifier output and is used to compensate the voltage control feedback loop.  |
| 10    | FB       | This pin is connected to the error amplifier inverting input and is used to compensate the voltage control feedback loop.   |

**Table 2. Pin description** (continued)

| N° | Name  | Description   |
|----|-------|---|
| 11 | GND   | All the internal references are referred to this pin. Connect it to the PCB signal ground.  |
| 12 | PGOOD | This pin is an open collector output and is pulled low if the output voltage is not within the above specified threshlds.<br>If not used may be left floating.  |
| 13 | PHASE | This pin is connected to the source of the upper mosfet and provides the return path for the high side driver. This pin monitors the drop across the upper mosfet for the current limit.  |
| 14 | UGATE | High side gate driver output.   |
| 15 | BOOT  | Bootstrap capacitor pin. Through this pin is supplied the high side driver and the upper mosfet. Connect through a capacitor to the PHASE pin and through a diode to Vcc (catode vs boot).  |
| 16 | PGND  | Power ground pin. This pin has to be connected closely to the low side mosfet source in order to reduce the noise injection into the device   |
| 17 | LGATE | This pin is the lower mosfet gate driver output   |
| 18 | VCC   | Device supply voltage. The operative supply voltage range is from 4.5 to 12V.<br>DO NOT CONNECT $V_{IN}$ to 12V if $V_{CC}$ IS 5V.  |
| 19 | OVP   | Over voltage protection. If the output voltage reach the 15% above the programmed voltage this pin is driven high and can be used to drive an external SCR that crowbar the supply voltage.<br>If not used, it may be left floating.  |
| 20 | RT    | Oscillator switching frequency pin. Connecting an external resistor from this pin to GND, the external frequency is increased according to the equation:<br>$f_S = 200\text{kHz} + \frac{5 \cdot 10^6}{R_T(\text{k}\Omega)}$ Connecting a resistor from this pin to Vcc (12V), the switching frequency is reduced according to the equation:<br>$f_S = 200\text{kHz} - \frac{4 \cdot 10^7}{R_T(\text{k}\Omega)}$ If the pin is not connected, the switching frequency is 200KHz.<br>The voltage at this pin is fixed at 1.23V. Forcing a 50 $\mu$ A current into this pin, the built in oscillator stops to switch. |

### 3 Electrical data

#### 3.1 Maximum ratings

Table 3. Absolute maximum ratings

| Symbol                                 | Parameter <sup>(1)</sup>     | Value                        | Unit |
|--|------------------------------|------------------------------|------|
| V <sub>CC</sub>                        | V <sub>CC</sub> to GND, PGND | 15                           | V    |
| V <sub>BOOT</sub>                      | Boot Voltage                 | 15                           | V    |
| V <sub>HGATE</sub> -V <sub>PHASE</sub> |                              | 15                           | V    |
|  | OCSET, PHASE, LGATE          | -0.3 to V <sub>CC</sub> +0.3 | V    |
|  | ROSC, SS, FB, PGOOD, VSEN    | 7                            | V    |
|  | COMP, OVP                    | 6.5                          | V    |

1. ESD immunity for pins 2 to 9 and 18 to 20 is guaranteed up to 1500V (Human Body Model).

#### 3.2 Thermal data

Table 4. Thermal data

| Symbol            | Parameter                              | Value      | Unit |
|-------------------|--|------------|------|
| R <sub>thJA</sub> | Thermal resistance junction to ambient | 110        | °C/W |
| T <sub>max</sub>  | Maximum junction temperature           | 150        | °C   |
| T <sub>STG</sub>  | Storage temperature range              | -40 to 150 | °C   |
| T <sub>J</sub>    | Junction temperature range             | 0 to 125   | °C   |

## 4 Electrical characteristics

**Table 5. Electrical characteristic** ( $V_{CC} = 12V$ ;  $T_A = 25^\circ C$  unless otherwise specified)

| Symbol                                    | Parameter                              | Test condition  | Min | Typ  | Max | Unit             |
|---|--|---|-----|------|-----|------------------|
| <b><math>V_{CC}</math> supply current</b> |  |   |     |      |     |                  |
| I <sub>CC</sub>                           | V <sub>CC</sub> supply current         | UGATE and LGATE open  |     | 5    |     | mA               |
| <b>Power-ON</b>                           |  |   |     |      |     |                  |
|   | Turn-On $V_{CC}$ threshold             | $V_{OCSET} = 4.5V$  |     |      | 4.6 | V                |
|   | Turn-Off $V_{CC}$ threshold            | $V_{OCSET} = 4.5V$  | 3.6 |      |     | V                |
|   | Rising $V_{OCSET}$ threshold           |   |     | 1.26 |     | V                |
| I <sub>SS</sub>                           | Soft start current                     |   |     | 10   |     | µA               |
| <b>Oscillator</b>                         |  |   |     |      |     |                  |
|   | Free running frequency                 | RT = OPEN   | 180 | 200  | 220 | kHz              |
|   | Total Variation                        | $6\text{ K}\Omega < R_T \text{ to GND } < 200\text{ K}\Omega$   | -15 |      | 15  | %                |
| ΔV <sub>OSC</sub>                         | Ramp amplitude                         | RT = OPEN   |     | 1.9  |     | V <sub>p-p</sub> |
| <b>Reference and DAC</b>                  |  |   |     |      |     |                  |
|   | DACOUT voltage accuracy                | VID0, VID1, VID2, VID3, VID25mV<br>see <a href="#">Table 6 on page 9</a> ;<br>$T_A = 0$ to $70^\circ C$ | -1  |      | 1   | %                |
|   | VID Pull-Up voltage                    |   |     | 3.1  |     | V                |
| <b>Error amplifier</b>                    |  |   |     |      |     |                  |
|   | DC gain                                |   |     | 88   |     | dB               |
| GBWP                                      | Gain-bandwidth product                 |   |     | 15   |     | MHz              |
| SR  | Slew-rate                              | COMP = 10pF   |     | 10   |     | V/µS             |
| <b>Gate drivers</b>                       |  |   |     |      |     |                  |
| I <sub>UGATE</sub>                        | High side source current               | $V_{BOOT} - V_{PHASE} = 12V$ ,<br>$V_{UGATE} - V_{PHASE} = 6V$  | 1   | 1.3  |     | A                |
| R <sub>UGATE</sub>                        | High side sink resistance              | $V_{BOOT} - V_{PHASE} = 12V$ ,<br>$I_{UGATE} = 300mA$   |     | 2    | 4   | Ω                |
| I <sub>LGATE</sub>                        | Low side source current                | $V_{CC} = 12V$ , $V_{LGATE} = 6V$   | 0.9 | 1.1  |     | A                |
| R <sub>LGATE</sub>                        | Low side sink resistance               | $V_{CC} = 12V$ , $I_{LGATE} = 300mA$  |     | 1.5  | 3   | Ω                |
|   | Output driver dead time                | PHASE connected to GND  |     | 120  |     | nS               |
| <b>Protections</b>                        |  |   |     |      |     |                  |
|   | Over voltage trip ( $V_{SEN}/DACOUT$ ) | $V_{SEN}$ rising  |     | 117  | 120 | %                |
| I <sub>OCSET</sub>                        | OCSET current source                   | $V_{OCSET} = 4.5V$  | 170 | 200  | 230 | µA               |

**Table 5. Electrical characteristic ( $V_{CC} = 12V$ ;  $T_A = 25^\circ C$  unless otherwise specified) (continued)**

| Symbol            | Parameter                               | Test condition                       | Min | Typ | Max | Unit |
|-------------------|---|--------------------------------------|-----|-----|-----|------|
| $I_{OVP}$         | OVP sourcing current                    | $V_{SEN} > OVP$ trip, $V_{OVP} = 0V$ | 60  |     |     | mA   |
| <b>Power GOOD</b> |   |                                      |     |     |     |      |
|                   | Upper threshold<br>( $V_{SEN}/DACOUT$ ) | $V_{SEN}$ rising                     | 108 | 110 | 112 | %    |
|                   | Lower threshold<br>( $V_{SEN}/DACOUT$ ) | $V_{SEN}$ falling                    | 88  | 90  | 92  | %    |
|                   | Hysteresis<br>( $V_{SEN}/DACOUT$ )      | Upper and lower threshold            |     | 2   |     | %    |
| $V_{PGOOD}$       | PGOOD voltage low                       | $I_{PGOOD} = -5mA$                   |     | 0.5 |     | V    |

## 4.1 VID Setting

**Table 6. VID Setting**

| VID4<br>(25mV) | VID3 | VID2 | VID1 | VID0 | Output<br>Voltage (V) | VID4<br>(25mV) | VID3 | VID2 | VID1 | VID0 | Output<br>Voltage (V) |
|----------------|------|------|------|------|-----------------------|----------------|------|------|------|------|-----------------------|
| 0              | 0    | 1    | 0    | 0    | <b>1.050</b>          | 0              | 1    | 1    | 0    | 0    | <b>1.450</b>          |
| 1              | 0    | 1    | 0    | 0    | <b>1.075</b>          | 1              | 1    | 1    | 0    | 0    | <b>1.475</b>          |
| 0              | 0    | 0    | 1    | 1    | <b>1.100</b>          | 0              | 1    | 0    | 1    | 1    | <b>1.500</b>          |
| 1              | 0    | 0    | 1    | 1    | <b>1.125</b>          | 1              | 1    | 0    | 1    | 1    | <b>1.525</b>          |
| 0              | 0    | 0    | 1    | 0    | <b>1.150</b>          | 0              | 1    | 0    | 1    | 0    | <b>1.550</b>          |
| 1              | 0    | 0    | 1    | 0    | <b>1.175</b>          | 1              | 1    | 0    | 1    | 0    | <b>1.575</b>          |
| 0              | 0    | 0    | 0    | 1    | <b>1.200</b>          | 0              | 1    | 0    | 0    | 1    | <b>1.600</b>          |
| 1              | 0    | 0    | 0    | 1    | <b>1.225</b>          | 1              | 1    | 0    | 0    | 1    | <b>1.625</b>          |
| 0              | 0    | 0    | 0    | 0    | <b>1.250</b>          | 0              | 1    | 0    | 0    | 0    | <b>1.650</b>          |
| 1              | 0    | 0    | 0    | 0    | <b>1.275</b>          | 1              | 1    | 0    | 0    | 0    | <b>1.675</b>          |
| 0              | 1    | 1    | 1    | 1    | <b>1.300</b>          | 0              | 0    | 1    | 1    | 1    | <b>1.700</b>          |
| 1              | 1    | 1    | 1    | 1    | <b>1.325</b>          | 1              | 0    | 1    | 1    | 1    | <b>1.725</b>          |
| 0              | 1    | 1    | 1    | 0    | <b>1.350</b>          | 0              | 0    | 1    | 1    | 0    | <b>1.750</b>          |
| 1              | 1    | 1    | 1    | 0    | <b>1.375</b>          | 1              | 0    | 1    | 1    | 0    | <b>1.775</b>          |
| 0              | 1    | 1    | 0    | 1    | <b>1.400</b>          | 0              | 0    | 1    | 0    | 1    | <b>1.800</b>          |
| 1              | 1    | 1    | 0    | 1    | <b>1.425</b>          | 1              | 0    | 1    | 0    | 1    | <b>1.825</b>          |

## 5 Device description

The device is an integrated circuit realized in BCD technology. It provides complete control logic and protections for a high performance step-down DC-DC converter optimized for microprocessor power supply. It is designed to drive N Channel Mosfets in a synchronous-rectified buck topology. The device works properly with Vcc ranging from 5V to 12V and regulates the output voltage starting from a 1.26V power stage supply voltage (Vin). The output voltage of the converter can be precisely regulated, programming the VID pins, from 1.050V to 1.825V with 25mV binary steps, with a maximum tolerance of  $\pm 1\%$  over temperature and line voltage variations. The device provides voltage-mode control with fast transient response. It includes a 200kHz free-running oscillator that is adjustable from 50kHz to 1MHz. The error amplifier features a 15MHz gain-bandwidth product and 10V/ms slew rate which permits high converter bandwidth for fast transient performance. The resulting PWM duty cycle ranges from 0% to 100%. The device protects against over-current conditions entering in HICCUP mode. The device monitors the current by using the  $r_{ds(ON)}$  of the upper MOSFET which eliminates the need for a current sensing resistor.

The device is available in SO20 package.

### 5.1 Oscillator

The switching frequency is internally fixed to 200kHz. The internal oscillator generates the triangular waveform for the PWM charging and discharging with a constant current an internal capacitor. The current delivered to the oscillator is typically  $50\mu A$  ( $F_{SW} = 200\text{KHz}$ ) and may be varied using an external resistor ( $R_T$ ) connected between RT pin and GND or VCC. Since the RT pin is maintained at fixed voltage (typ. 1.235V), the frequency is varied proportionally to the current sunked (forced) from (into) the pin.

In particular connecting it to GND the frequency is increased (current is sunked from the pin), according to the following relationship:

#### Equation 1

$$f_S = 200\text{kHz} + \frac{4.94 \cdot 10^6}{R_T(\text{k}\Omega)}$$

Connecting  $R_T$  to  $V_{CC} = 12V$  or to  $V_{CC} = 5V$  the frequency is reduced (current is forced into the pin), according to the following relationships:

**Equation 2**

$$f_S = 200\text{kHz} + \frac{4.306 \cdot 10^7}{R_T(\text{k}\Omega)} \quad V_{CC} = 12\text{V}$$

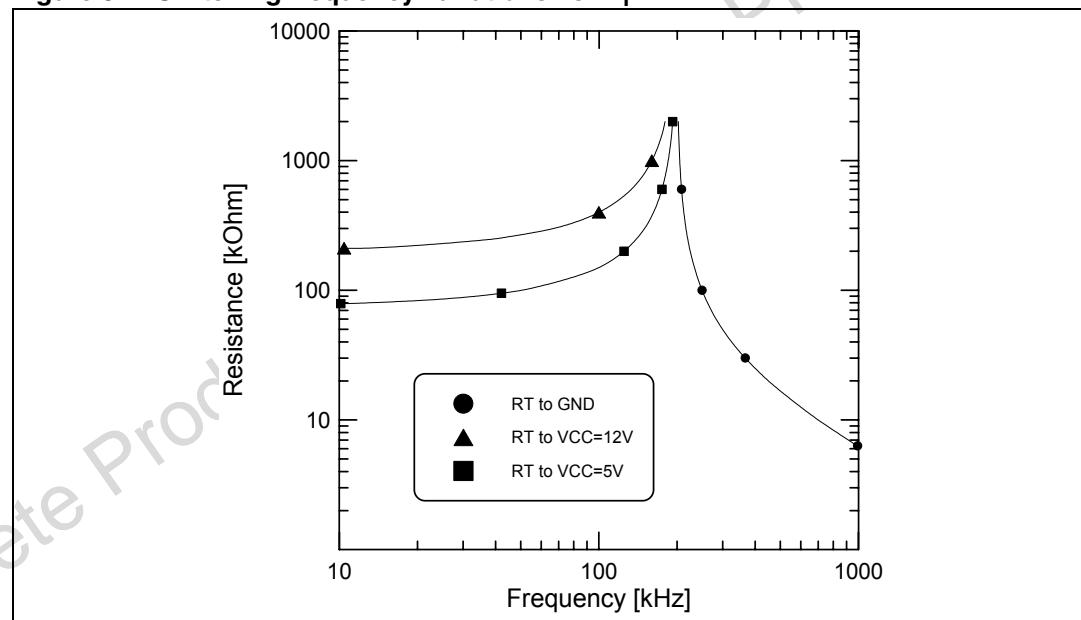
**Equation 3**

$$f_S = 200\text{kHz} + \frac{15 \cdot 10^7}{R_T(\text{k}\Omega)} \quad V_{CC} = 5\text{V}$$

Switching frequency variations vs.  $R_T$  are reported in [Figure 3 on page 11](#).

*Note: That forcing a  $50\mu\text{A}$  current into this pin, the device stops switching because no current is delivered to the oscillator.*

**Figure 3. Switching frequency variations vs.  $R_T$**



## 5.2 Digital to analog converter

The built-in digital to analog converter allows the adjustment of the output voltage from 1.050V to 1.825V with 25mV binary steps as shown in the previous [Table 6: VID Setting on page 9](#). The internal reference is trimmed to ensure the precision of 1%.

The internal reference voltage for the regulation is programmed by the voltage identification (VID) pins. These are TTL compatible inputs of an internal DAC that is realised by means of a series of resistors providing a partition of the internal voltage reference. The VID code drives a multiplexer that selects a voltage on a precise point of the divider. The DAC output is delivered to an amplifier obtaining the VPROG voltage reference (i.e. the set-point of the error amplifier). Internal pull-ups are provided (realized with a  $5\mu\text{A}$  current generator); in this way, to program a logic "1" it is enough to leave the pin floating, while to program a logic "0" it is enough to short the pin to GND.

The voltage identification (VID) pin configuration also sets the power-good thresholds (PGOOD) and the over- voltage protection (OVP) thresholds.

## 5.3 Soft start and inhibit

At start-up a ramp is generated charging the external capacitor  $C_{SS}$  by means of a  $10\mu\text{A}$  constant current, as shown in [Figure 4 on page 13](#)

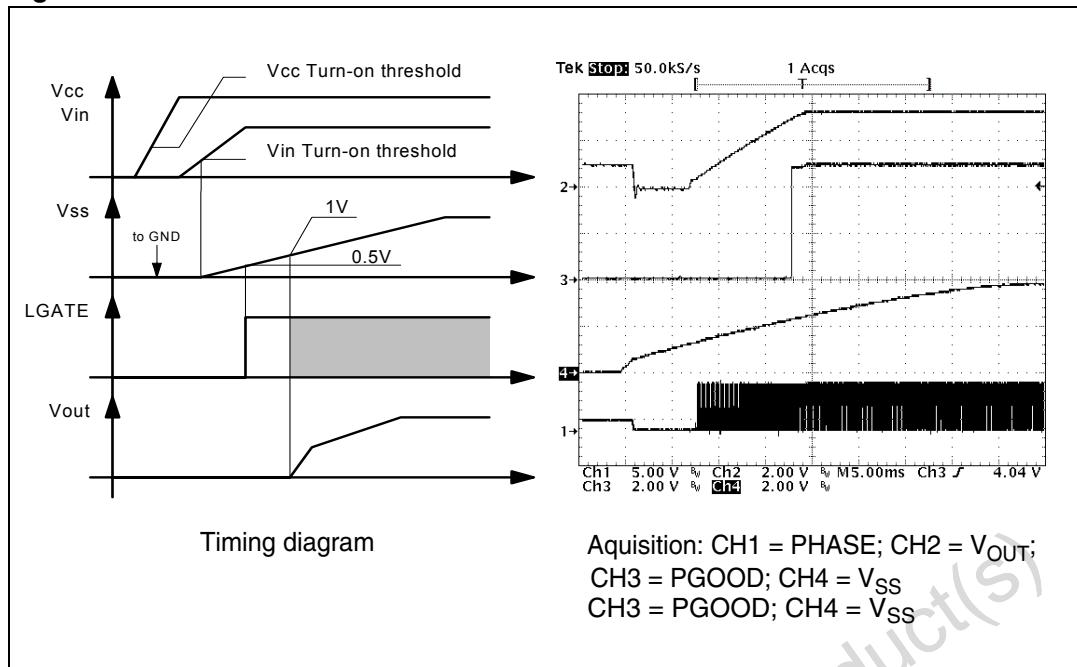
When the voltage across the soft start capacitor ( $V_{SS}$ ) reaches 0.5V the lower power MOS is turned on to discharge the output capacitor. As  $V_{SS}$  reaches 1V (i.e. the oscillator triangular wave inferior limit) also the upper MOS begins to switch and the output voltage starts to increase.

The VSS growing voltage initially clamps the output of the error amplifier, and consequently VOUT linearly increases, as shown in [Figure 4 on page 13](#). In this phase the system works in open loop. When VSS is equal to VCOMP the clamp on the output of the error amplifier is released. In any case another clamp on the non-inverting input of the error amplifier remains active, allowing to VOUT to grow with a lower slope (i.e. the slope of the VSS voltage, see [Figure 4 on page 13](#)). In this second phase the system works in closed loop with a growing reference. As the output voltage reaches the desired value VPROG, also the clamp on the error amplifier input is removed, and the soft start finishes. Vss increases until a maximum value of about 4V.

The Soft-Start will not take place, and the relative pin is internally shorted to GND, if both VCC and OCSET pins are not above their own Turn-On thresholds; in this way the device starts switching only if both the power supplies are present. During normal operation, if any under-voltage is detected on one of the two supplies, the SS pin is internally shorted to GND and so the SS capacitor is rapidly discharged.

The device goes in INHIBIT state forcing SS pin below 0.4V. In this condition both external MOSFETS are kept OFF.

Figure 4. Soft start



## 5.4 Driver section

The driver capability on the high and low side drivers allows to use different types of power MOS (also multiple MOS to reduce the  $R_{ds(ON)}$ ), maintaining fast switching transition.

The low-side mos driver is supplied directly by  $V_{CC}$  while the high-side driver is supplied by the **BOOT** pin.

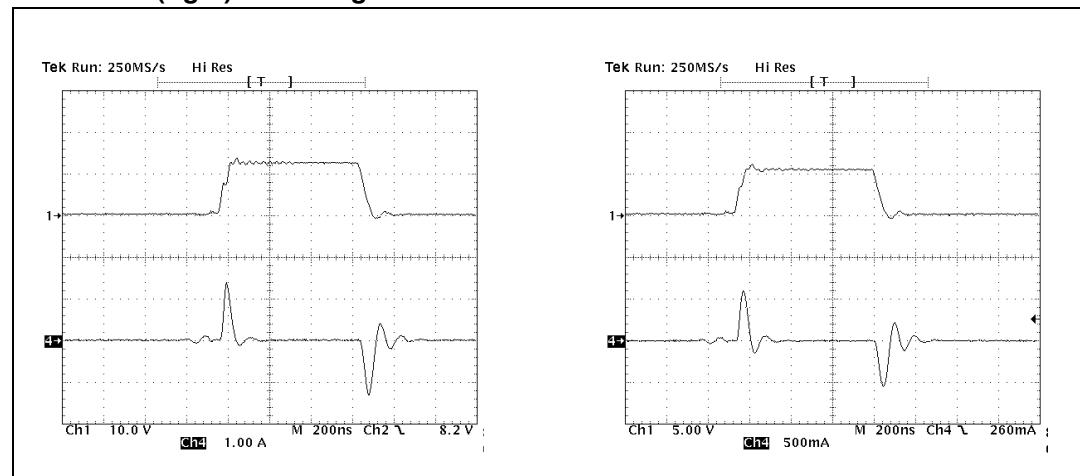
Adaptative dead time control is implemented to prevent cross-conduction and allow to use many kinds of mosfets. The upper mos turn-on is avoided if the lower gate is over about 200mV while the lower mos turn-on is avoided if the **PHASE** pin is over about 500mV. The upper mos is in any case turned-on after 200nS from the low side turn-off.

The peak current is shown for both the upper ([Figure 5 on page 14](#)) and the lowr ([Figure 6 on page 14](#)) driver at 5V and 12V. a 4nF capacitive load has been used in these measurements.

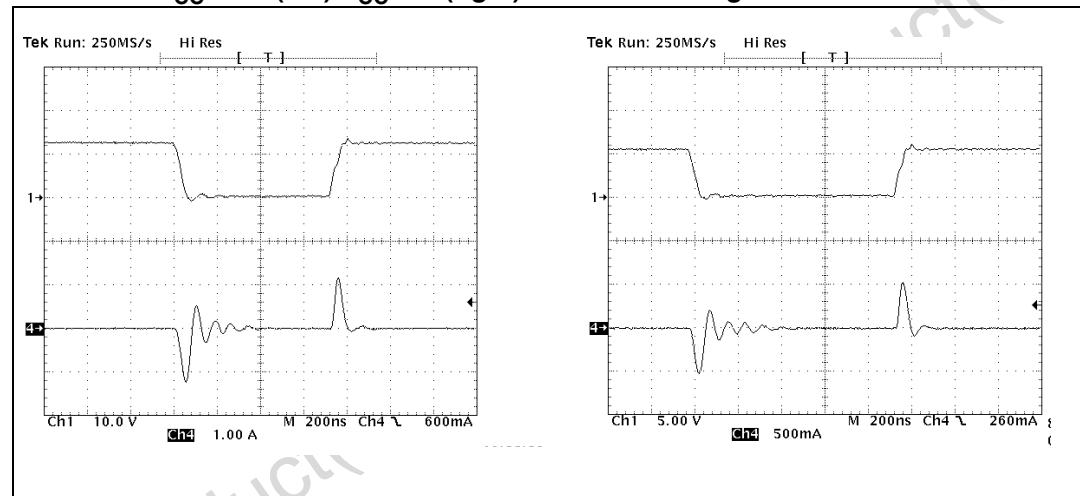
For the lower driver, the source peak current is 1.1A @  $V_{CC} = 12V$  and 500mA @  $V_{CC} = 5V$ , and the sink peak current is 1.3A @  $V_{CC} = 12V$  and 500mA @  $V_{CC} = 5V$ .

Similary, for the upper driver, the source peak current is 1.3A @  $V_{boot}-V_{phase} = 12V$  and 600mA @  $V_{boot}-V_{phase} = 5V$ , and the sink peak current is 1.3A @  $V_{boot}-V_{phase} = 12V$  and 550mA @  $V_{boot}-V_{phase} = 5V$ .

**Figure 5. High side driver peak current,  $V_{boot}-V_{phase}=12V$  (left)  $V_{boot}-V_{phase}=5V$  (right) CH1 = High Side Gate CH4 = inductor current**



**Figure 6. Low side driver peak current,  $V_{CC}=12V$  (left)  $V_{CC}=5V$  (right) CH1 = Low side gate CH4 = inductor current**



## 5.5 Monitor and protection

The output voltage is monitored by means of pin 1 (VSEN). If it is not within  $\pm 10\%$  (typ.) of the programmed value, the powergood output is forced low.

The device provides overvoltage protection, when the output voltage reaches a value 17% (typ.) greater than the nominal one. If the output voltage exceed this threshold, the OVP pin is forced high (5V) and the lower driver is turned on as long as the over-voltage is detected. The OVP pin is capable to deliver up to 60mA (min) in order to trigger an external SCR connected to burn the input fuse. The low-side mosfet turn-on implement this function when the SCR is not used and helps in keeping the ouput low.

To perform the overcurrent protection the device compares the drop across the high side MOS, due to its

$R_{DSON}$ , with the voltage across the external resistor ( $R_{OCS}$ ) connected between the OCSET pin and drain of the upper MOS. Thus the overcurrent threshold ( $I_P$ ) can be calculated with the following relationship:

### Equation 4

$$I_P = \frac{I_{OCS} \cdot R_{OCS}}{R_{DSON}}$$

where the typical value of  $I_{OCS}$  is  $200\mu A$ .

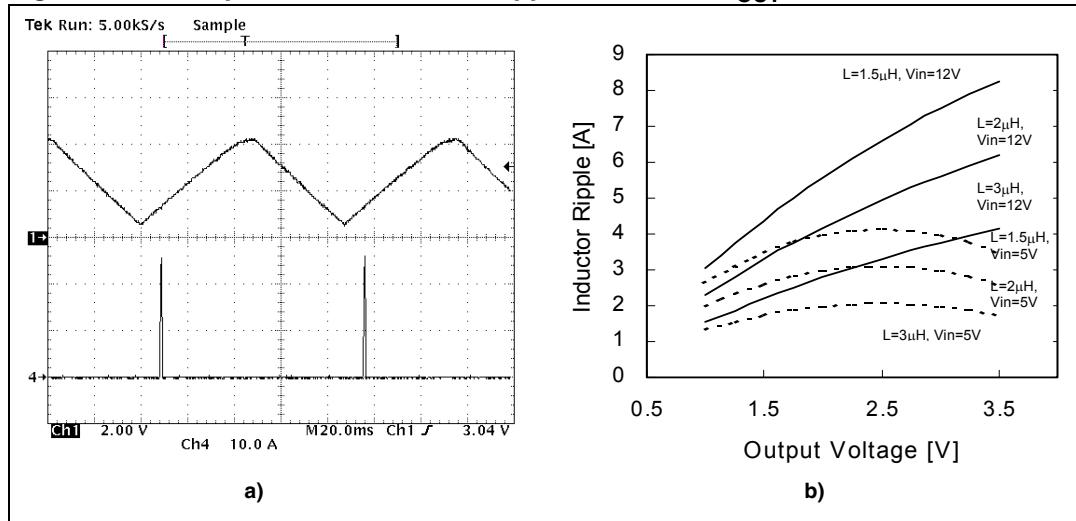
To calculate the  $R_{OCS}$  value it must be considered the maximum  $R_{DSON}$  (also the variation with temperature) and the minimum value of  $I_{OCS}$ . To avoid undesirable trigger of overcurrent protection this relationship must be satisfied:

### Equation 5

$$I_P \geq I_{OUTMAX} + \frac{\Delta I}{2} = I_{PEAK}$$

where  $\Delta I$  is the inductance ripple current and  $I_{OUTMAX}$  is the maximum output current.

In case of output short circuit the soft start capacitor is discharged with constant current ( $10\mu A$  typ.) and when the SS pin reaches 0.5V the soft start phase is restarted. During the soft start the over-current protection is always active and if such kind of event occurs, the device turns off both mosfets, and the SS capacitor is discharged again after reaching the upper threshold of about 4V. The system is now working in HICCUP mode, as shown in [Figure 7 on page 16](#) a. After removing the cause of the over-current, the device restart working normally without power supplies turn off and on.

Figure 7. Hiccup mode and Inductor ripple current vs.  $V_{OUT}$ 

## 5.6 Inductor design

The inductance value is defined by a compromise between the transient response time, the efficiency, the cost and the size. The inductor has to be calculated to sustain the output and the input voltage variation to maintain the ripple current  $\Delta I_L$  between 20% and 30% of the maximum output current. The inductance value can be calculated with this relationship:

Equation 6

$$L = \frac{V_{IN} - V_{OUT}}{f_s \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

Where  $f_{SW}$  is the switching frequency,  $V_{IN}$  is the input voltage and  $V_{OUT}$  is the output voltage. Figure 7 b shows the ripple current vs. the output voltage for different values of the inductor, with  $V_{IN} = 5V$  and  $V_{IN} = 12V$ .

Increasing the value of the inductance reduces the ripple current but, at the same time, reduces the converter response time to a load transient. If the compensation network is well designed, the device is able to open or close the duty cycle up to 100% or down to 0%. The response time is now the time required by the inductor to change its current from initial to final value. Since the inductor has not finished its charging time, the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitance required.

The response time to a load transient is different for the application or the removal of the load: if during the application of the load the inductor is charged by a voltage equal to the difference between the input and the output voltage, during the removal it is discharged only by the output voltage. The following expressions give approximate response time for  $\Delta I$  load transient in case of enough fast compensation network response:

**Equation 7**

$$t_{\text{application}} = \frac{L \cdot \Delta I}{V_{\text{IN}} - V_{\text{OUT}}}$$

**Equation 8**

$$t_{\text{removal}} = \frac{L \cdot \Delta I}{V_{\text{OUT}}}$$

The worst condition depends on the input voltage available and the output voltage selected. Anyway the worst case is the response time after removal of the load with the minimum output voltage programmed and the maximum input voltage available.

## 5.7 Output capacitor

Since the microprocessors require a current variation beyond 10A during load transients, with a slope in the range of tenth A/ $\mu$ sec, the output capacitor is a basic component for the fast response of the power supply. In fact for first few microseconds they supply the current to the load. The controller recognizes immediately the load transient and sets the duty cycle at 100%, but the current slope is limited by the inductor value.

The output voltage has a first drop due to the current variation inside the capacitor (neglecting the effect of the ESL):

**Equation 9**

$$\Delta V_{\text{OUT}} = \Delta I_{\text{OUT}} \cdot \text{ESR}$$

A minimum capacitor value is required to sustain the current during the load transient without discharging it. The voltage drop due to the output capacitor discharge is given by the following equation:

**Equation 10**

$$\Delta V_{\text{OUT}} = \frac{\Delta I_{\text{OUT}}^2 \cdot L}{2 \cdot C_{\text{OUT}} \cdot (V_{\text{INMIN}} \cdot D_{\text{MAX}} - V_{\text{OUT}})}$$

Where  $D_{\text{MAX}}$  is the maximum duty cycle value that is 100%. The lower is the ESR, the lower is the output drop during load transient and the lower is the output voltage static ripple.

## 5.8 Input capacitor

The input capacitor has to sustain the ripple current produced during the on time of the upper MOS, so it must have a low ESR to minimize the losses.

The rms value of this ripple is:

**Equation 11**

$$I_{rms} = I_{OUT} \sqrt{D \cdot (1 - D)}$$

Where D is the duty cycle. The equation reaches its maximum value with D = 0.5.

The losses in worst case are:

**Equation 12**

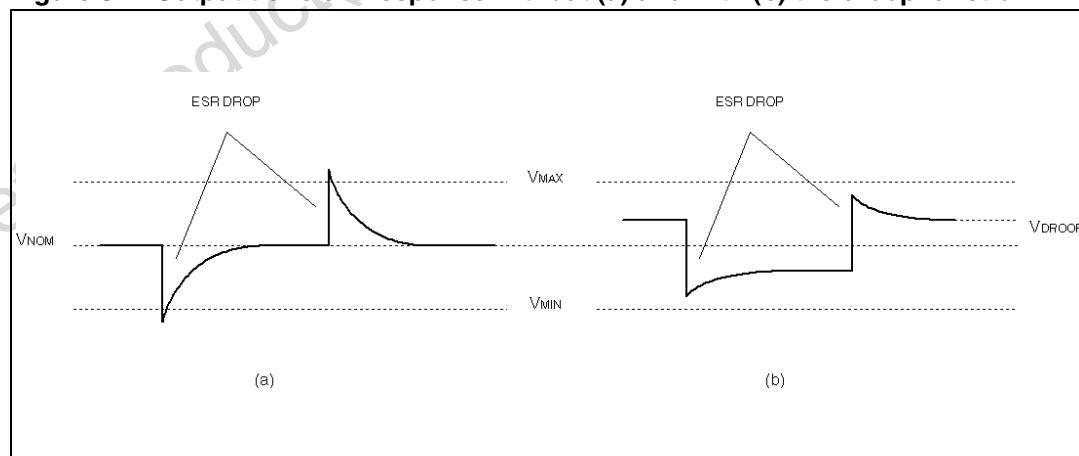
$$P = ESR \cdot I_{rms}^2$$

## 5.9 Compensation network design

The control loop is a voltage mode ([Figure 9 on page 19](#)) that uses a droop function to satisfy the requirements for a VRM module, reducing the size and the cost of the output capacitor.

This method "recovers" part of the drop due to the output capacitor ESR in the load transient, introducing a dependence of the output voltage on the load current: at light load the output voltage will be higher than the nominal level, while at high load the output voltage will be lower than the nominal value.

**Figure 8. Output transient response without (a) and with (b) the droop function**



As shown in [Figure 8 on page 18](#), the ESR drop is present in any case, but using the droop function the total deviation of the output voltage is minimized. In practice the droop function introduces a static error ( $V_{DROOP}$  in [Figure 8 on page 18](#)) proportional to the output current. Since a sense resistor is not present, the output DC current is measured by using the intrinsic resistance of the inductance (a few  $m\Omega$ ). So the low-pass filtered inductor voltage (that is the inductor current) is added to the feedback signal, implementing the droop function in a simple way. Referring to the schematic in [Figure 9](#), the static characteristic of the closed loop system is:

### Equation 13

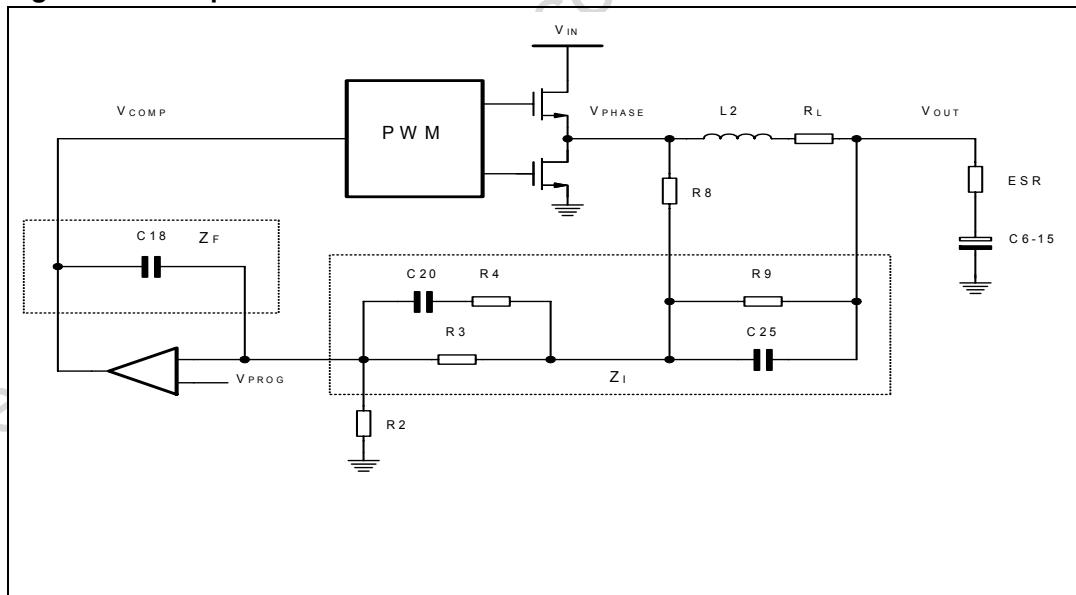
$$V_{OUT} = V_{PROG} + V_{PROG} \cdot \frac{R3 + R8 // R9}{R2} - \frac{R_L \cdot R8 // R9}{R8} \cdot I_{OUT}$$

Where  $V_{PROG}$  is the output voltage of the digital to analog converter (i.e. the set point) and  $R_L$  is the inductance resistance. The second term of the equation allows a positive offset at zero load ( $\Delta V^+$ ); the third term introduces the droop effect ( $\Delta V_{DROOP}$ ). Note that the droop effect is equal the ESR drop if:

### Equation 14

$$\frac{R_L \cdot R8 // R9}{R8} = ESR$$

**Figure 9. Compensation network**



Considering the previous relationships R2, R3, R8 and R9 may be determined in order to obtain the desired droop effect as follow:

- Choose a value for R2 in the range of hundreds of KΩ to obtain realistic values for the other components.
- From the above equations, it results:

**Equation 15**

$$R8 = \frac{\Delta V^+ \cdot R2}{V_{PROG}} \cdot \frac{R_L \cdot I_{MAX}}{\Delta V_{DROOP}}$$

**Equation 16**

$$R9 = R8 \cdot \frac{\Delta V_{DROOP}}{R_L \cdot I_{MAX}} \cdot \frac{1}{1 + \frac{\Delta V_{DROOP}}{R_L \cdot I_{MAX}}}$$

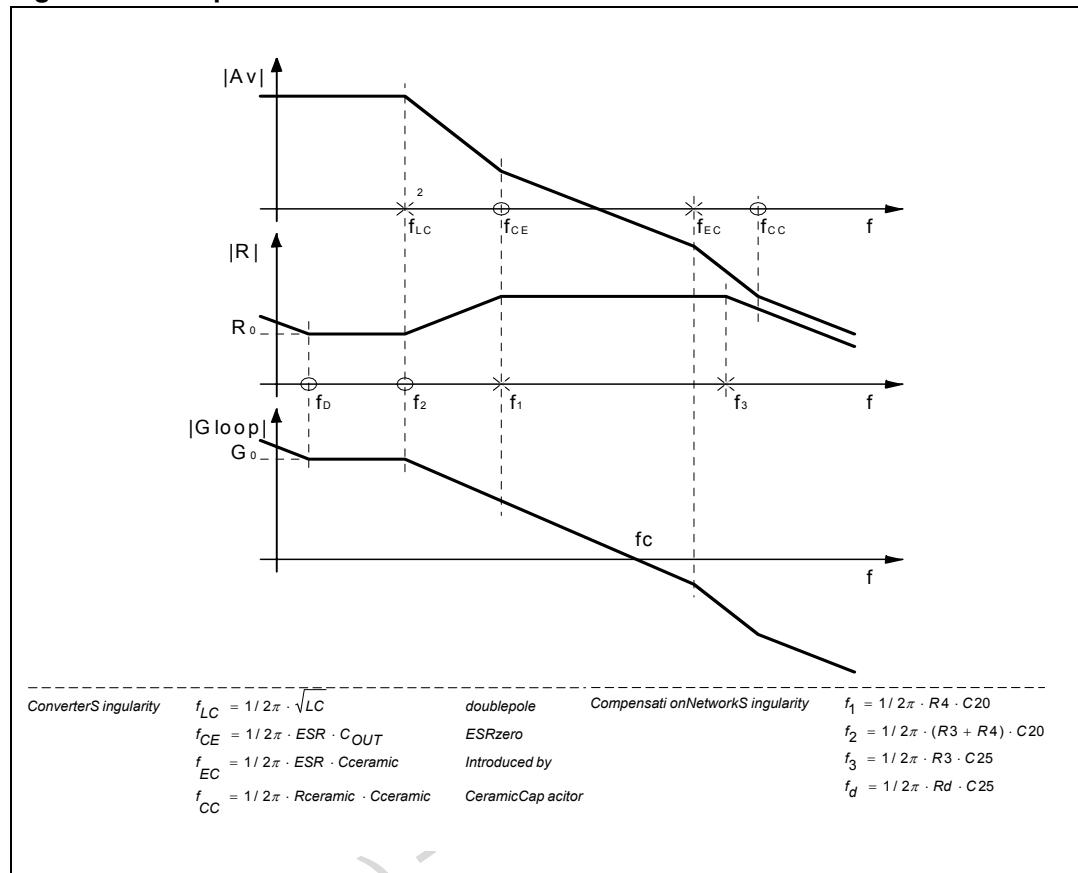
Where  $I_{MAX}$  is the maximum output current.

- The component R3 must be chosen in order to obtain  $R3 \ll R8//R9$  to permit these and successive simplifications.

Therefore, with the droop function the output voltage decreases as the load current increases, so the DC output impedance is equal to a resistance  $R_{OUT}$ . It is easy to verify that the output voltage deviation under load transient is minimum when the output impedance is constant with frequency.

To choose the other components of the compensation network, the transfer function of the voltage loop is considered. To simplify the analysis is supposed that  $R3 \ll Rd$ , where  $Rd = (R8//R9)$ .

**Figure 10. Compensation network definition**



The transfer function may be evaluated neglecting the connection of  $R8$  to PHASE because, as will see later, this connection is important only at low frequencies. So  $R4$  is considered connected to  $VOUT$ . Under this assumption, the voltage loop has the following transfer function:

**Equation 17**

$$G_{loop}(s) = Av(s) \cdot R(s) = Av(s) \cdot \frac{Zf(s)}{Zi(s)} \quad \text{where} \quad Av(s) = \frac{V_{in}}{\Delta V_{osc}} \cdot \frac{Z_C(s)}{Z_C(s) + Z_L(s)}$$

Where  $Z_C(s)$  and  $Z_L(s)$  are the output capacitor and inductor impedance respectively. The expression of  $Z_i(s)$  may be simplified as follow:

**Equation 18**

$$\frac{R_d \cdot \frac{1}{s} \cdot C_{25}}{R_d + \frac{1}{s} \cdot C_{25}} + \frac{\left( R_4 + \frac{1}{s} \cdot C_{20} \right) \cdot R_3}{\left( R_4 + \frac{1}{s} \cdot C_{20} \right) + R_3} = \frac{R_d \left( 1 + s \cdot (\tau_1 + \tau_d) + s^2 \cdot \frac{R_3}{R_d} \cdot \tau_1 \cdot \tau_d \right)}{(1 + s \cdot \tau_2) \cdot (1 + s \cdot \tau_d)} = R_d \frac{\left( 1 + s \frac{R_3}{R_d} \cdot \tau_d \right) \cdot (1 + s \cdot \tau_2) \cdot (1 + s \cdot \tau_1)}{(1 + s \cdot \tau_2) \cdot (1 + s \cdot \tau_d)}$$

Where:  $\tau_1 = R_4 \times C_{20}$ ,  $\tau_2 = (R_4+R_3) \times C_{20}$  and  $\tau_d = R_d \times C_{25}$ .

The regulator transfer function became now:

**Equation 19**

$$R(s) \approx \frac{(1 + s \cdot \tau_2) \cdot (1 + s \cdot \tau_d)}{s \cdot C_{18} \cdot R_d \cdot \left( 1 + s \frac{R_3}{R_d} \cdot \tau_d \right) \cdot (1 + s \cdot \tau_1)}$$

*Figure 10 on page 21* shows a method to select the regulator components (please note that the frequencies  $f_{EC}$  and  $f_{CC}$  corresponds to the singularities introduced by additional ceramic capacitors in parallel to the output main electrolytic capacitor).

- To obtain a flat frequency response of the output impedance, the droop time constant  $\tau_d$  has to be equal to the inductor time constant (see the note at the end of the section):

**Equation 20**

$$\tau_d = R_d \cdot C_{25} = \frac{L}{R_L} = \tau_L \Rightarrow C_{25} = \frac{L}{(R_L \cdot R_d)}$$

- To obtain a constant -20dB/dec Gloop(s) shape the singularity  $f_1$  and  $f_2$  are placed in proximity of  $f_{CE}$  and  $f_{LC}$  respectively. This implies that:

**Equation 21**

$$\frac{f_2}{f_1} = \frac{f_{LC}}{f_{CE}} \Rightarrow R_4 = R_3 \cdot \left( \frac{f_{LC}}{f_{CE}} - 1 \right)$$

$$f_1 = f_{CE} \Rightarrow C_{20} = \frac{1}{2} \cdot \pi \cdot R_4 \cdot f_{CE}$$

- To obtain a Gloop bandwidth of  $f_C$ , results:

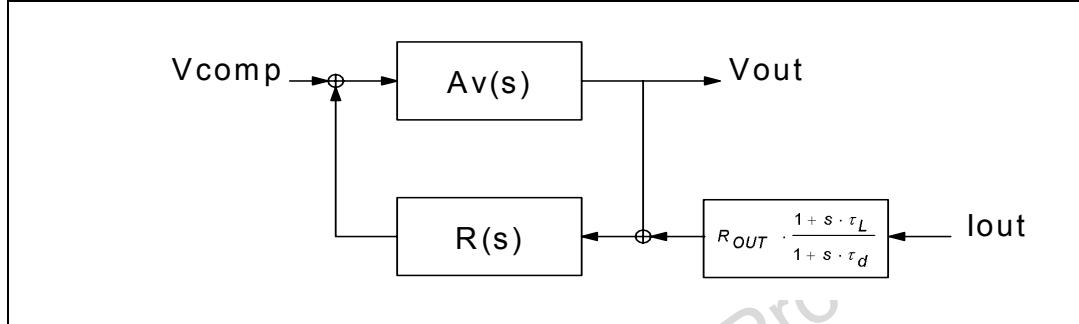
**Equation 22**

$$f_{LC} = 1 \cdot f_C \Rightarrow G_0 = A_0 \cdot R_0 = \frac{V_{IN}}{\Delta V_{osc}} \cdot \frac{C_{20} // C_{25}}{C_{18}} = \frac{f_C}{f_{LC}} \Rightarrow C_{18} = \frac{V_{IN}}{\Delta V_{osc}} \cdot \frac{C_{20} \cdot C_{25}}{C_{20} + C_{25}}$$

**Note:** To understand the reason of the previous assumption, the scheme in [Figure 11 on page 23](#) must be considered.

In this scheme, the inductor current has been substituted by the load current, because in the frequencies range of interest for the Droop function these current are substantially the same and it was supposed that the droop network don't represent a charge for the inductor.

**Figure 11. Voltage regulation with droop function block scheme**



It results:

**Equation 23**

$$Z_{OUT} = \frac{V_o}{I_{LOAD}} = R_d \cdot \frac{1 + s\tau_L}{1 + s\tau_d} \cdot \frac{G_{LOOP}}{1 + G_{LOOP}} = R_{OUT} \cdot \frac{1 + s\tau_L}{1 + s\tau_d}$$

Because in the interested range  $|G_{LOOP}| \gg 1$ .

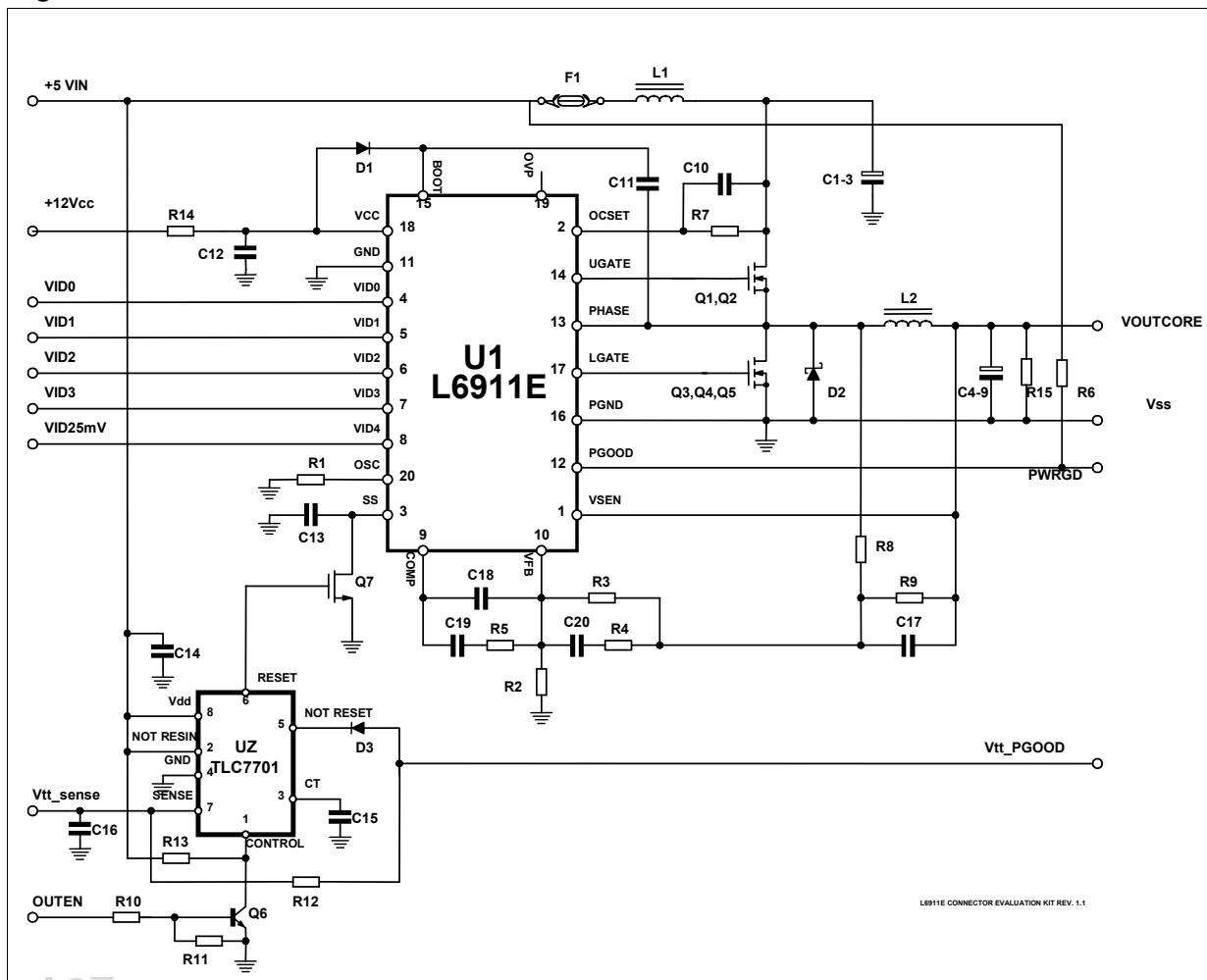
To obtain a flat shape, the relationship considered will naturally follow.

## 6 VRM demo board description

*Figure 12* shows the schematic circuit of the VRM evaluation board. The design has been developed for a VRM 8.5 Flexible Motherboard applicaton delivering up to 28.5A.

An additional circuit sense a Vtt bus (1.2V typ.) and generate a 2.5mS (typ.) delayed Vtt\_PWRGD signal when this rail is over 1.1V. The assertion of the Vtt\_PWRGD signal enables the device together with the ENOUT input.

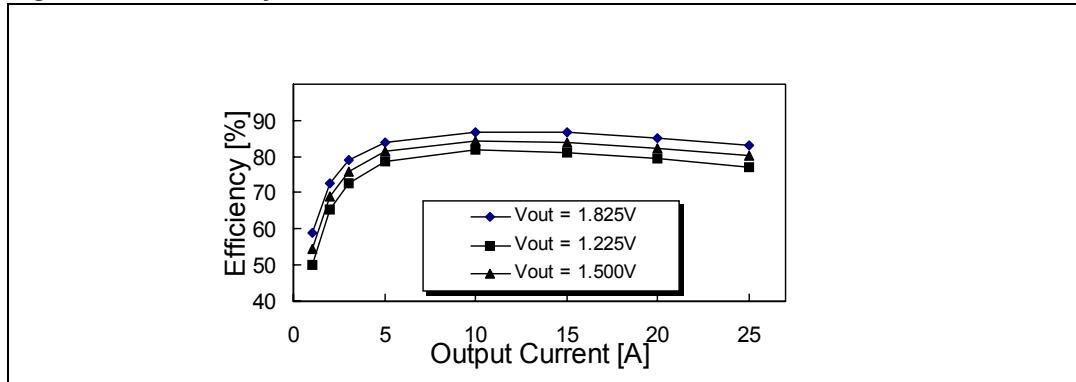
**Figure 12. Schematic circuit**



## 6.1 Efficiency

The measured efficiency versus load current at different output voltages is shown in [Figure 13](#). In the application two Mosfets STS12NF30L (30V, 8.5mΩ typ with  $V_{GS} = 12V$ ) connected in parallel are used for the High Side, while three of them are used for the Low Side.

**Figure 13. Efficiency vs. load current**



## 6.2 Inductor design

Since the maximum output current is 28.5A, to have a 20% ripple (5A) the inductor chosen is  $1.5\mu H$ .

## 6.3 Output capacitor

In the demo six OSCON capacitors, model 6SP680M, are used, with a maximum ESR equal to  $12m\Omega$  each. Therefore the resultant ESR is of  $2m\Omega$ . For load transient of 28.5A in the worst case the voltage drop is of:

**Equation 24**

$$\Delta V_{out} = 28.5 * 0.002 = 57mV$$

The voltage drop due to the capacitor discharge during load transient, considering that the maximum duty cycle is equal to 100% results in 46.5mV with 1.85V of programmed output.

## 6.4 Input capacitor

For  $I_{OUT} = 28.5A$  and with  $D = 0.5$ (worst case for input current ripple),  $I_{rms}$  is equal to  $17.8A$ . Three OSCON electrolytic capacitors 6SP680M, with a maximum ESR equal to  $12m\Omega$ , are chosen to sustain the ripple. So the losses in worst case are:

### Equation 25

$$P = ESR \cdot I_{rms}^2 = (1.25(670)m)W$$

## 6.5 Over-current protection

Substituting the demo board parameters in the relationship reported in the relative section, ( $I_{OCSMIN} = 170\mu A$ ;  $I_P = 33A$ ;  $R_{DSONMAX} = 3m\Omega$ ) it results that  $R_{OCS} = 1k\Omega$ .

## 7 Connector pin orientation

**Table 7. Connector pin orientation**

| Pin #                 | Row A                 | Pin # | Row B                |
|-----------------------|-----------------------|-------|----------------------|
| 1                     | 5Vin                  | 50    | 5Vin                 |
| 2                     | 5Vin                  | 49    | 5Vin                 |
| 3                     | 5Vin                  | 48    | 5Vin                 |
| 4                     | 5Vin                  | 47    | 5Vin                 |
| 5                     | 12Vin                 | 46    | 12Vin                |
| 6                     | 12Vin                 | 45    | 12Vin                |
| 7                     | Reserved              | 44    | No Contact           |
| 8                     | VID0                  | 43    | VID1                 |
| 9                     | VID2                  | 42    | VID3                 |
| 10                    | VID4 (25mV)           | 41    | PWRGD                |
| 11                    | OUTEN                 | 40    | Ishare               |
| 12                    | V <sub>TT_PWRGD</sub> | 39    | V <sub>TT</sub>      |
| 13                    | Vss                   | 38    | Vss                  |
| 14                    | V <sub>CC_CORE</sub>  | 37    | Vss                  |
| 15                    | V <sub>CC_CORE</sub>  | 36    | V <sub>CC_CORE</sub> |
| 16                    | Vss                   | 35    | Vss                  |
| 17                    | V <sub>CC_CORE</sub>  | 34    | V <sub>CC_CORE</sub> |
| <b>Mechanical Key</b> |                       |       |                      |
| 18                    | Vss                   | 33    | Vss                  |
| 19                    | V <sub>CC_CORE</sub>  | 32    | V <sub>CC_CORE</sub> |
| 20                    | Vss                   | 31    | Vss                  |
| 21                    | V <sub>CC_CORE</sub>  | 30    | V <sub>CC_CORE</sub> |
| 22                    | Vss                   | 29    | Vss                  |
| 23                    | V <sub>CC_CORE</sub>  | 28    | V <sub>CC_CORE</sub> |
| 24                    | Vss                   | 27    | Vss                  |
| 25                    | V <sub>CC_CORE</sub>  | 26    | V <sub>CC_CORE</sub> |

## 8 PCB and components layout

Figure 14. PCB and components layouts

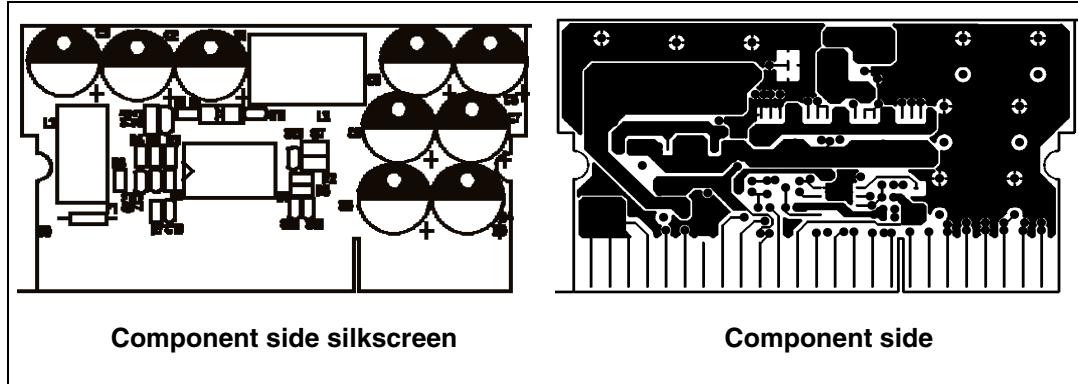


Figure 15. PCB and components layouts

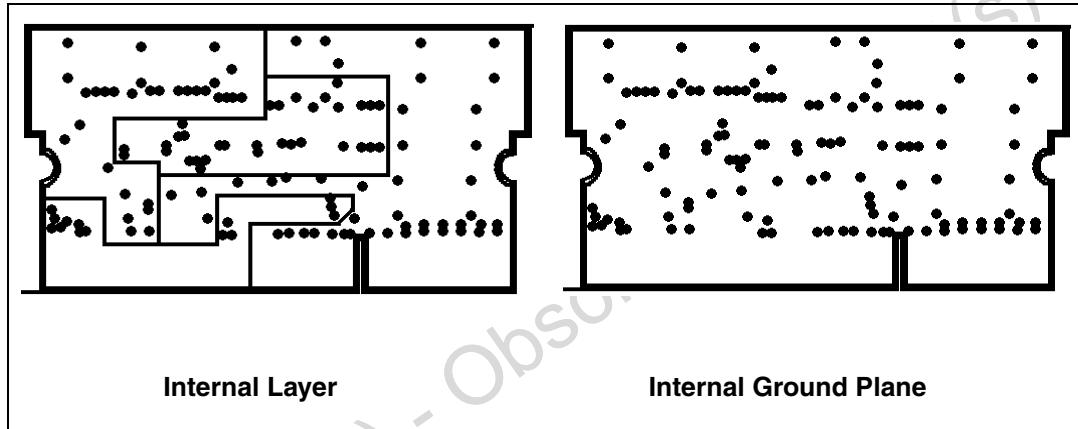
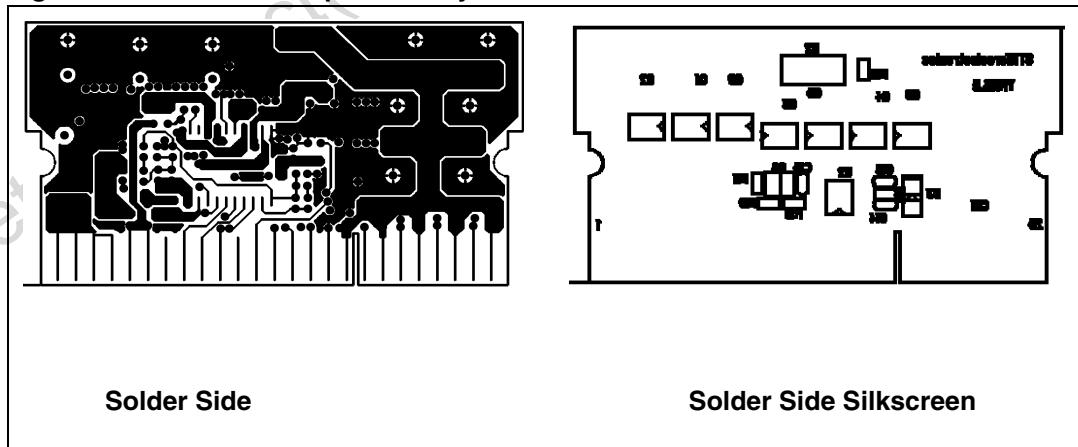


Figure 16. PCB and components layouts



**Table 8. Part list**

| <b>Resistors</b>   |                                |                                 |                                  |
|--------------------|--------------------------------|---------------------------------|----------------------------------|
| R1                 | Not Mounted                    |                                 | SMD 0805                         |
| R2                 | 470K                           | 1%                              | SMD 0805                         |
| R3                 | 1K                             |                                 | SMD 0805                         |
| R4                 | 82                             |                                 | SMD 0805                         |
| R5                 | Not Mounted                    |                                 | SMD 0805                         |
| R6                 | 20K                            |                                 | SMD 0805                         |
| R7                 | 680                            |                                 | SMD 0805                         |
| R8                 | 13K                            |                                 | SMD 0805                         |
| R9                 | 100K                           |                                 | SMD 0805                         |
| R10                | 6.8K                           | 1%                              | SMD 0805                         |
| R11                | 10K                            | 1%                              | SMD 0805                         |
| R12                | 1K                             |                                 | SMD 0805                         |
| R13                | 10K                            |                                 | SMD 0805                         |
| R14                | 8.2Ω                           |                                 | SMD 0805                         |
| R15                | 1K                             |                                 | SMD 0805                         |
| <b>Capacitors</b>  |                                |                                 |                                  |
| C1-C3              | 680µF- 6.3V                    | OSCON 6SP680M                   | Radial 10x10.5                   |
| C4-C9              | 820 µF – 4V or<br>680µF – 6.3V | OSCON 4SP820M<br>OSCON 6SP680M  | Radial 10x10.5<br>Radial 10x10.5 |
| C10                | 1nF                            |                                 | SMD 0805                         |
| C11,C13-C16        | 100nF                          |                                 | SMD 0805                         |
| C12                | 1µF                            |                                 | SMD 0805                         |
| C17                | 47nF                           |                                 | SMD 0805                         |
| C18                | 3.3nF                          |                                 | SMD 0805                         |
| C19                | Not Mounted                    |                                 | SMD 0805                         |
| C20                | 100nF                          |                                 | SMD 0805                         |
| <b>Magnetics</b>   |                                |                                 |                                  |
| L1                 | 1.5µH                          | T44-52 Core, 7T - 18AWG         |                                  |
| L2                 | 1.8µH                          | T50-52B Core, 8T – 16AWG        |                                  |
| <b>Transistors</b> |                                |                                 |                                  |
| Q1-Q5              | STS12NF30L or<br>FDS6670       | STMicroelectronics<br>Fairchild | SO8<br>SO8                       |
| Q6                 | Signal NPN BJT                 |                                 | SOT23                            |
| Q7                 | Signal MOSFET                  |                                 | SOT23                            |

**Table 8. Part list (continued)**

| <b>Diodes</b> |             |                    |       |
|---------------|-------------|--------------------|-------|
| D1            | 1N4148      |                    | SOT23 |
| D2            | STPS3L25U   | STMicroelectronics | SMB   |
| D3            |             |                    |       |
| <b>Ics</b>    |             |                    |       |
| U1            | L6911E      | STMicroelectronics | SO20  |
| U2            | TLC7701QD   | Texas Instruments  | SO8   |
| <b>Fuse</b>   |             |                    |       |
| F1            | 251015A-15A | Littlefuse         | AXIAL |

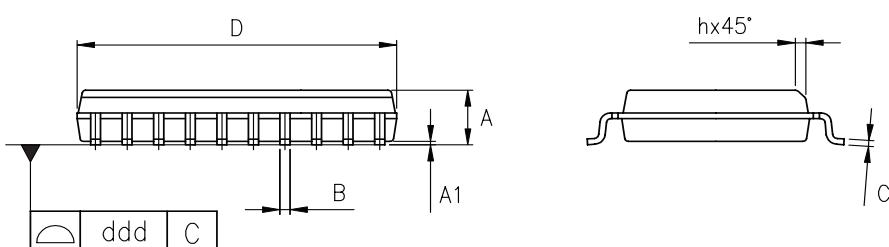
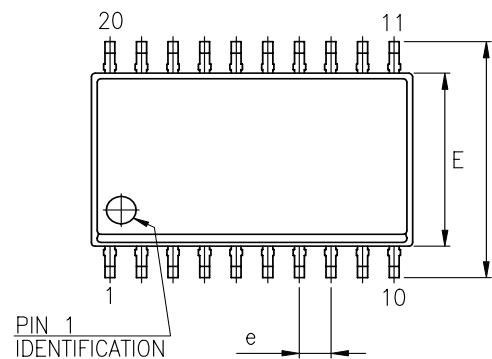
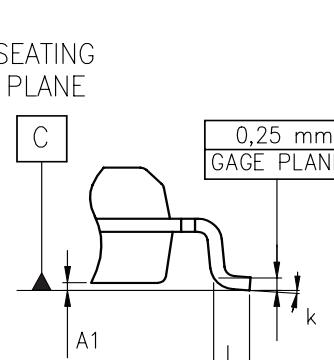
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## 9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

Obsolete Product(s) - Obsolete Product(s)

Figure 17. SO20 Mechanical data &amp; package dimensions

| DIM.  | mm                   |      |       | inch  |       |       |  | OUTLINE AND<br>MECHANICAL DATA |
|---|----------------------|------|-------|-------|-------|-------|--|--------------------------------|
|   | MIN.                 | Typ. | MAX.  | MIN.  | Typ.  | MAX.  |  |                                |
| A   | 2.35                 |      | 2.65  | 0.093 |       | 0.104 |  |                                |
| A1  | 0.10                 |      | 0.30  | 0.004 |       | 0.012 |  |                                |
| B   | 0.33                 |      | 0.51  | 0.013 |       | 0.200 |  |                                |
| C   | 0.23                 |      | 0.32  | 0.009 |       | 0.013 |  |                                |
| D <sup>(1)</sup>  | 12.60                |      | 13.00 | 0.496 |       | 0.512 |  |                                |
| E   | 7.40                 |      | 7.60  | 0.291 |       | 0.299 |  |                                |
| e   |                      | 1.27 |       |       | 0.050 |       |  |                                |
| H   | 10.0                 |      | 10.65 | 0.394 |       | 0.419 |  |                                |
| h   | 0.25                 |      | 0.75  | 0.010 |       | 0.030 |  |                                |
| L   | 0.40                 |      | 1.27  | 0.016 |       | 0.050 |  |                                |
| k   | 0° (min.), 8° (max.) |      |       |       |       |       |  |                                |
| ddd   |                      |      | 0.10  |       |       | 0.004 |  |                                |
| (1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.   |                      |      |       |       |       |       |  |                                |
| <b>SO20</b>   |                      |      |       |       |       |       |  |                                |
|    |                      |      |       |       |       |       |  |                                |
| 0016022 D   |                      |      |       |       |       |       |  |                                |

Obsolete

## 10 Revision history

**Table 9. Revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 15-Nov-2001 | 2        | Preliminary version  |
| 10-Apr-2007 | 3        | Document has been reformatted, updated <a href="#">Table 3</a> . |

Obsolete Product(s) - Obsolete Product(s)

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