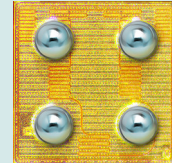


EPC2036 – Enhancement Mode Power Transistor

 $V_{DS}, 100\text{ V}$
 $R_{DS(on)}, 73\text{ m}\Omega$
 $I_D, 1.7\text{ A}$


Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 60 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 150°C)	120	
I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 340^\circ\text{C/W}$)	1.7	A
	Pulsed (25°C , $T_{PULSE} = 300\text{ }\mu\text{s}$)	18	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	



EPC2036 eGaN® FETs are supplied only in passivated die form with solder bumps
Die Size: 0.9 mm x 0.9 mm

Applications

- High Speed DC-DC conversion
- Wireless Power Transfer
- High Frequency Hard-Switching and Soft-Switching Circuits
- LiDAR/Pulsed Power Applications
- Class-D Audio

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

www.epc-co.com/epc/Products/eGaNfETs/EPC2036.aspx

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$, $I_D = 300\text{ }\mu\text{A}$	100			V
I_{DSS}	Drain Source Leakage	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$	20	250		μA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$	0.1	0.9		mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$	20	250		μA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 0.6\text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}$, $I_D = 1\text{ A}$	62	73		m Ω
V_{SD}	Source-Drain Forward Voltage	$I_S = 0.5\text{ A}$, $V_{GS} = 0\text{ V}$	1.9			V

All measurements were done with substrate shorted to source.

Thermal Characteristics			
		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.5	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction to Board	65	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	100	$^\circ\text{C/W}$

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Dynamic Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _{ISS}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V		75	90	pF
C _{OSS}	Output Capacitance			50	75	
C _{RSS}	Reverse Transfer Capacitance			0.7	1.1	
R _G	Gate Resistance			0.6		Ω
Q _G	Total Gate Charge	V _{DS} = 50 V, V _{GS} = 5 V, I _D = 1 A		700	910	pC
Q _{GS}	Gate-to-Source Charge	V _{DS} = 50 V, I _D = 1 A		170		
Q _{GD}	Gate-to-Drain Charge			140	240	
Q _{G(TH)}	Gate Charge at Threshold			120		
Q _{OSS}	Output Charge	V _{DS} = 50 V, V _{GS} = 0 V		3900	5900	
Q _{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate shorted to source.

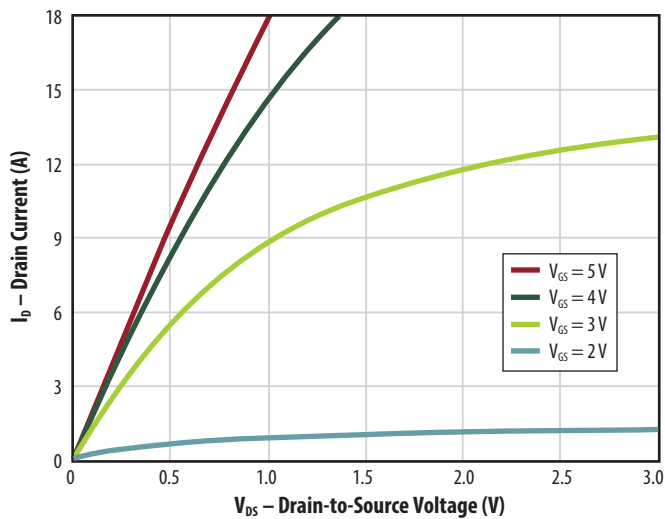
Figure 1: Typical Output Characteristics at 25°C 

Figure 2: Transfer Characteristics

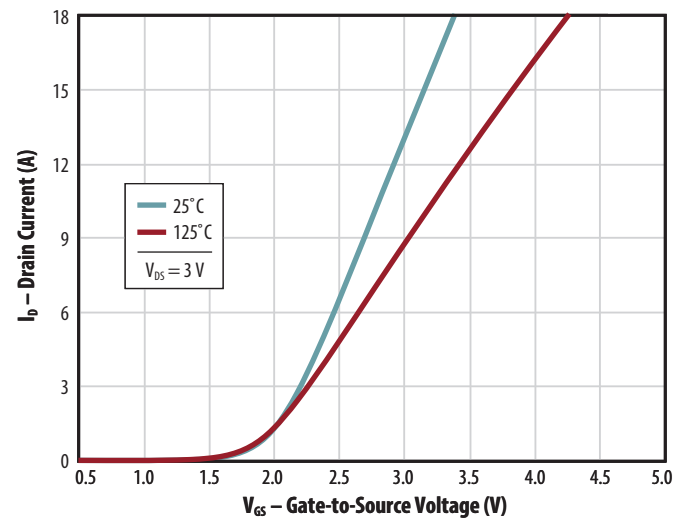
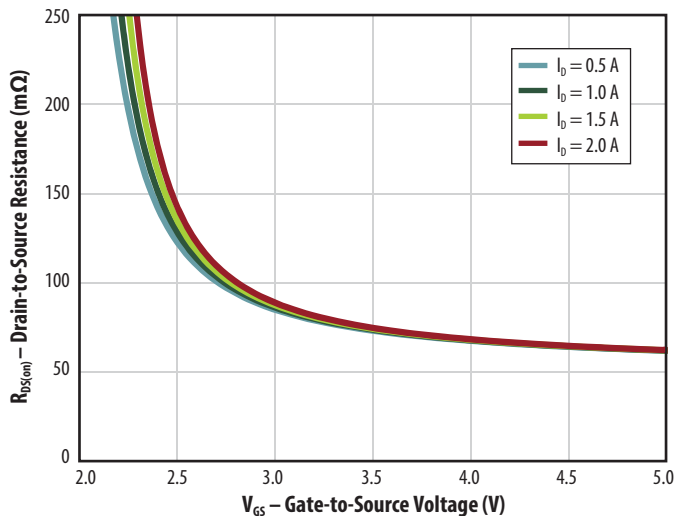
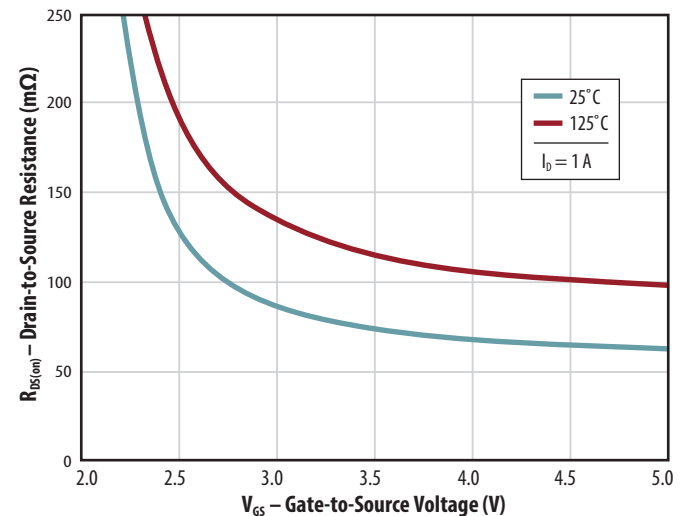
Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

Figure 5a: Capacitance (Linear Scale)

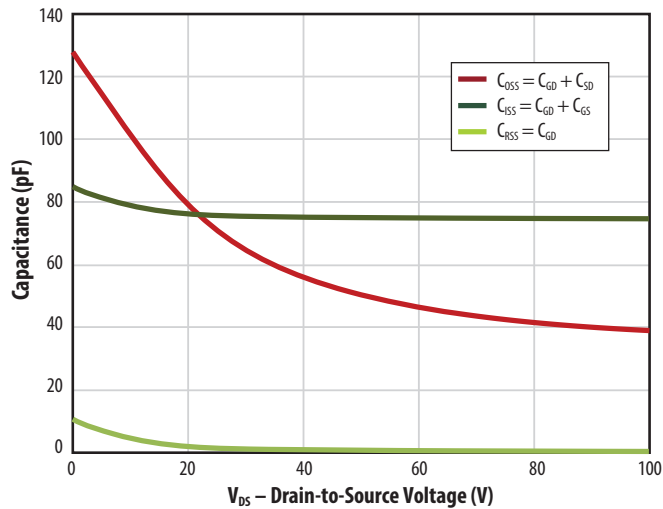


Figure 5b: Capacitance (Log Scale)

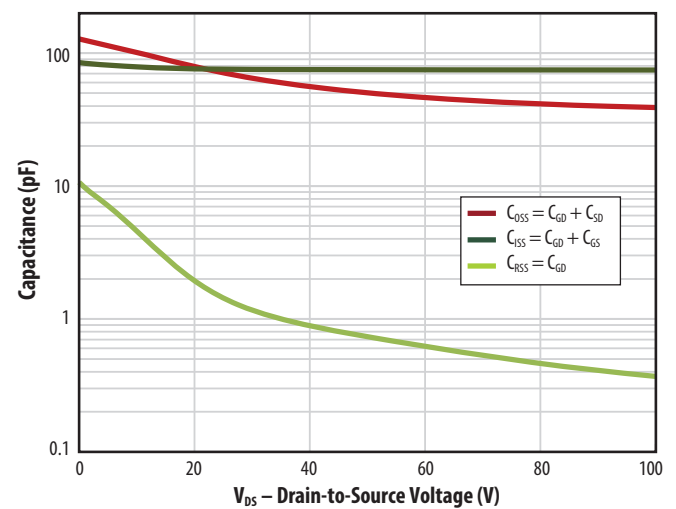


Figure 6: Gate Charge

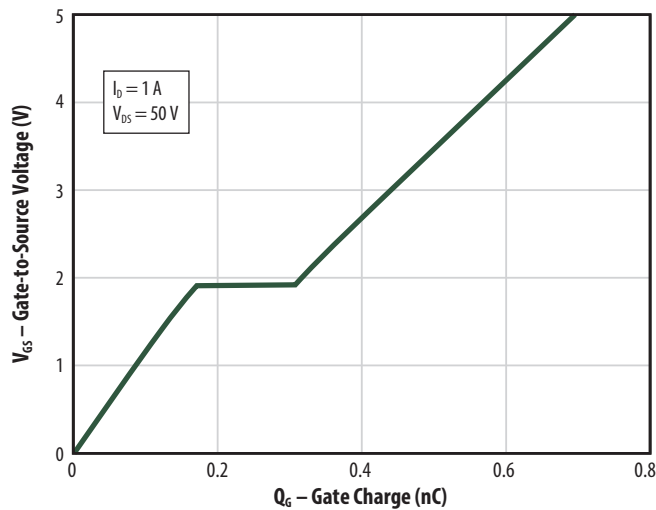


Figure 7: Reverse Drain-Source Characteristics

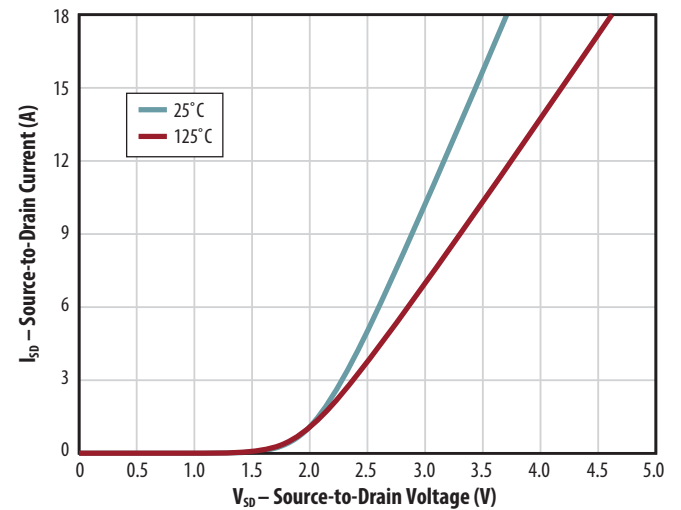


Figure 8: Normalized On Resistance vs. Temperature

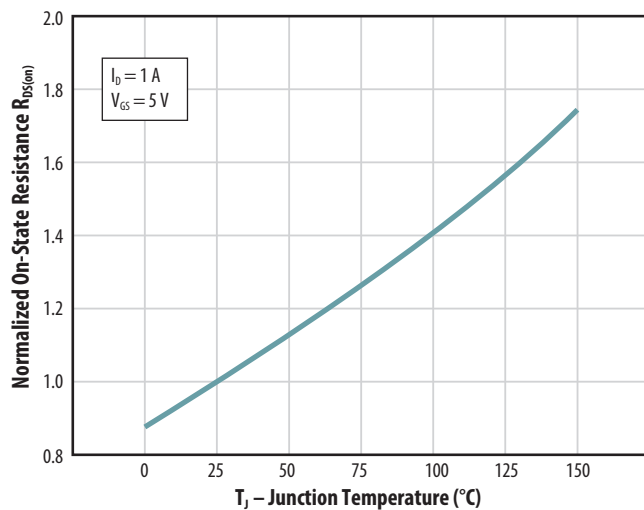
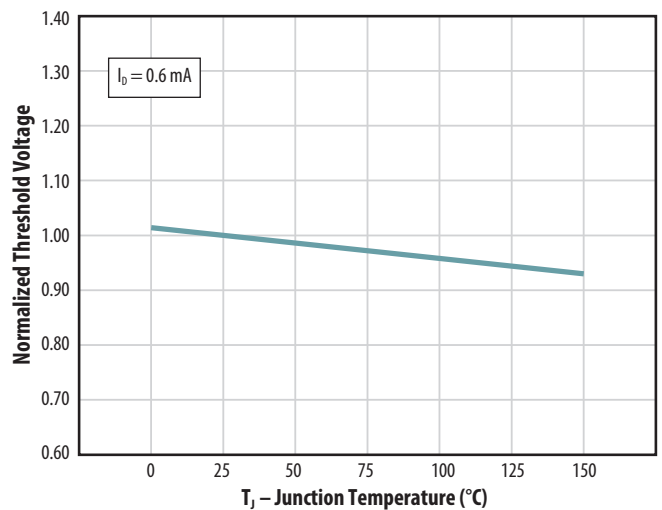


Figure 9: Normalized Threshold Voltage vs. Temperature



All measurements were done with substrate shorted to source.

Figure 10: Gate Leakage Current

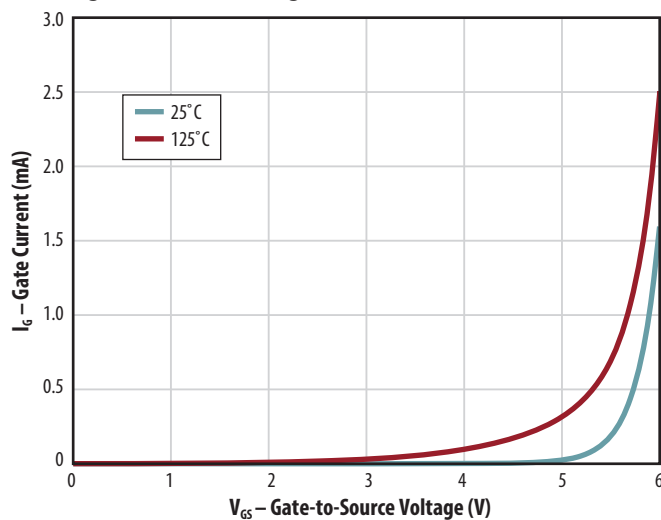


Figure 11: Transient Thermal Response Curves

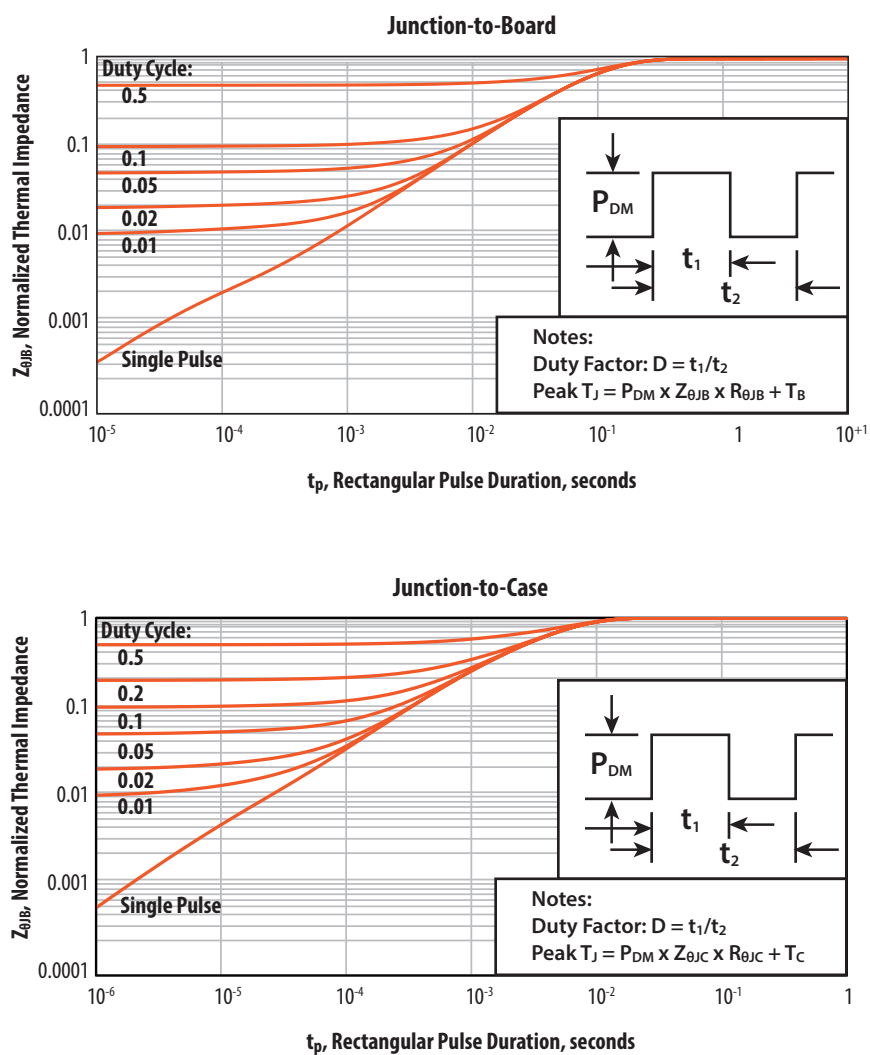
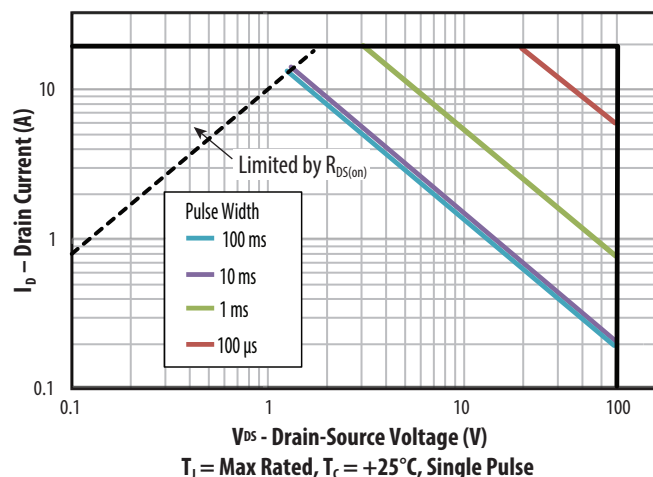
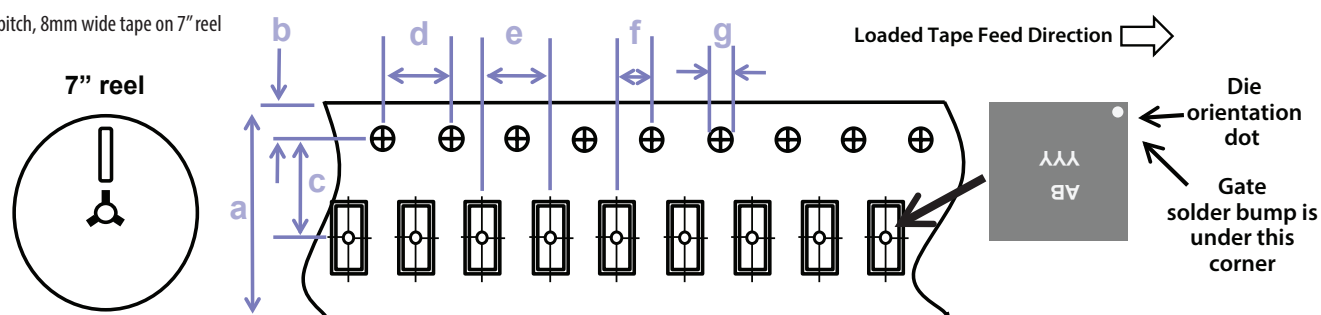


Figure 12: Safe Operating Area



TAPE AND REEL CONFIGURATION

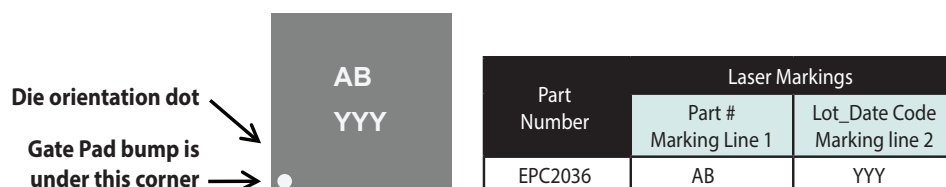
4mm pitch, 8mm wide tape on 7" reel



Dimension (mm)	EPC2036 (note 1)		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

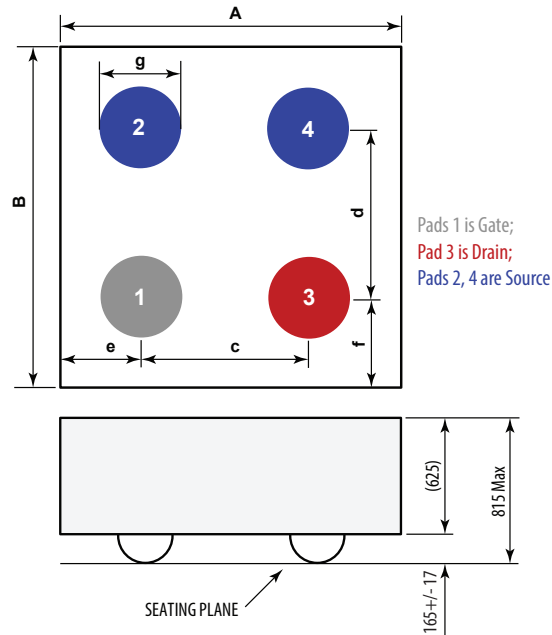
Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE MARKINGS



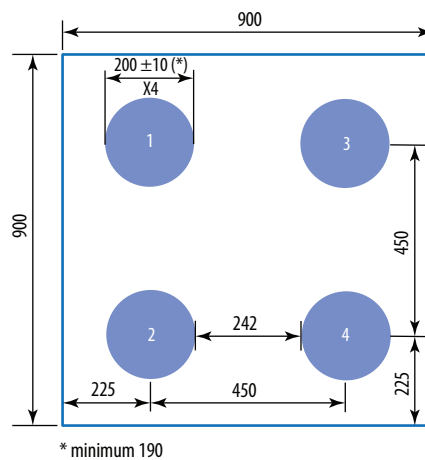
DIE OUTLINE

Solder Bump View



DIM	MIN	Nominal	MAX
A	870	900	930
B	870	900	930
c	450	450	450
d	450	450	450
e	210	225	240
f	210	225	240
g	187	208	229

Side View

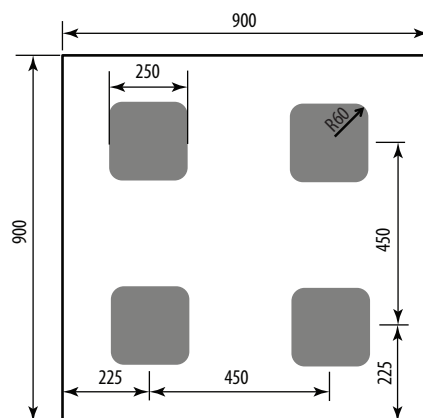
**RECOMMENDED
LAND PATTERN**(measurements in μm)

The land pattern is solder mask defined
Solder mask is $10\mu\text{m}$ smaller per side than bump

Pads 1 is Gate;

Pad 3 is Drain;

Pads 2, 4 are Source

**RECOMMENDED
STENCIL DRAWING**(measurements in μm)

Recommended stencil should be 4mil ($100\mu\text{m}$) thick, must
be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5%
metals content.

Additional assembly resources available at
<http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398; 8,785,974; 8,890,168; 8,969,918; 8,853,749; 8,823,012

Information subject to
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