

**SN54LVTH541, SN74LVTH541  
3.3-V ABT OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

SCBS682G – MARCH 1997 – REVISED OCTOBER 2003

- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )**
- **Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ C$**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **$I_{off}$  and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

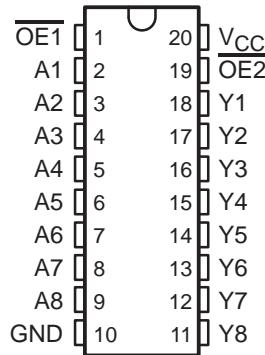
#### description/ordering information

These octal buffers/drivers are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

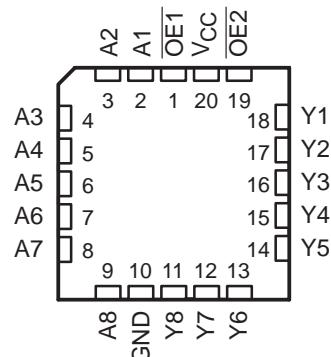
The 'LVTH541 devices are ideal for driving bus lines or buffer-memory address registers. These devices feature inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all outputs are in the high-impedance state.

**SN54LVTH541 . . . J OR W PACKAGE  
SN74LVTH541 . . . DB, DW, NS, OR PW PACKAGE  
(TOP VIEW)**



**SN54LVTH541 . . . FK PACKAGE  
(TOP VIEW)**



$T_A$	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^\circ C$ to $85^\circ C$	SOIC – DW	Tube	SN74LVTH541DW	LVTH541
		Tape and reel	SN74LVTH541DWR	
	SOP – NS	Tape and reel	SN74LVTH541NSR	LVTH541
	SSOP – DB	Tape and reel	SN74LVTH541DBR	LXH541
	TSSOP – PW	Tube	SN74LVTH541PW	LXH541
		Tape and reel	SN74LVTH541PWR	
$-55^\circ C$ to $125^\circ C$	CDIP – J	Tube	SNJ54LVTH541J	SNJ54LVTH541J
	CFP – W	Tube	SNJ54LVTH541W	SNJ54LVTH541W
	LCCC – FK	Tube	SNJ54LVTH541FK	SNJ54LVTH541FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**description/ordering information (continued)**

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

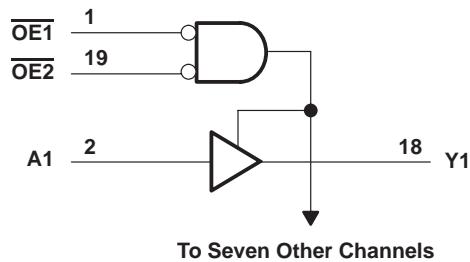
When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JEDEC 51-7.

#### **recommended operating conditions (see Note 4)**

		SN54LVTH541		SN74LVTH541		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2.7	3.6	2.7	3.6	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage		5.5		5.5	V
I <sub>OH</sub>	High-level output current		-24		-32	mA
I <sub>OL</sub>	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate	200		200		μs/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54LVTH541			SN74LVTH541			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 2.7 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ , $I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$			$V_{CC} - 0.2$			V
	$V_{CC} = 2.7 \text{ V}$ , $I_{OH} = -8 \text{ mA}$	2.4			2.4			
	$V_{CC} = 3 \text{ V}$	$I_{OH} = -24 \text{ mA}$	2					
		$I_{OH} = -32 \text{ mA}$			2			
$V_{OL}$	$V_{CC} = 2.7 \text{ V}$	$I_{OL} = 100 \mu\text{A}$		0.2		0.2		V
		$I_{OL} = 24 \text{ mA}$		0.5		0.5		
	$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$		0.4		0.4		
		$I_{OL} = 32 \text{ mA}$		0.5		0.5		
		$I_{OL} = 48 \text{ mA}$		0.55				
		$I_{OL} = 64 \text{ mA}$				0.55		
$I_I$	$V_{CC} = 0 \text{ or } 3.6 \text{ V}$ , $V_I = 5.5 \text{ V}$			10		10		$\mu\text{A}$
	Control inputs	$V_{CC} = 3.6 \text{ V}$ , $V_I = V_{CC} \text{ or GND}$		$\pm 1$		$\pm 1$		
		$V_{CC} = 3.6 \text{ V}$	$V_I = V_{CC}$	1		1		
	Data inputs		$V_I = 0$	-5		-5		
$I_{off}$	$V_{CC} = 0$ , $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$					$\pm 100$		$\mu\text{A}$
$I_I(\text{hold})$	Data inputs	$V_{CC} = 3 \text{ V}$	$V_I = 0.8 \text{ V}$	75		75		$\mu\text{A}$
			$V_I = 2 \text{ V}$	-75		-75		
		$V_{CC} = 3.6 \text{ V}^\ddagger$	$V_I = 0 \text{ to } 3.6 \text{ V}$			$\pm 500$		
$I_{OZH}$	$V_{CC} = 3.6 \text{ V}$ , $V_O = 3 \text{ V}$			5		5		$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 3.6 \text{ V}$ , $V_O = 0.5 \text{ V}$			-5		-5		$\mu\text{A}$
$I_{OZPU}$	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$ , $V_O = 0.5 \text{ V to } 3 \text{ V}$ , OE = don't care			$\pm 100^*$		$\pm 100$		$\mu\text{A}$
$I_{OZPD}$	$V_{CC} = 1.5 \text{ V to } 0$ , $V_O = 0.5 \text{ V to } 3 \text{ V}$ , OE = don't care			$\pm 100^*$		$\pm 100$		$\mu\text{A}$
$I_{CC}$	$V_{CC} = 3.6 \text{ V}$ , $I_O = 0$ , $V_I = V_{CC} \text{ or GND}$	Outputs high		0.19		0.19		$\text{mA}$
		Outputs low		5		5		
		Outputs disabled		0.19		0.19		
$\Delta I_{CC}^\S$	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ , One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or GND			0.2		0.2		$\text{mA}$
$C_I$	$V_I = 3 \text{ V or } 0$			3		3		$\text{pF}$
$C_O$	$V_O = 3 \text{ V or } 0$			7		7		$\text{pF}$

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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**switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH541		SN74LVTH541		UNIT			
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$					
			MIN	MAX	MIN	MAX				
$t_{PLH}$	A	Y	1	3.7	4	1.1	2.4	3.5	3.9	ns
$t_{PHL}$			1	3.7	4	1.1	2.4	3.5	3.9	
$t_{PZH}$	$\overline{OE1}$ or $\overline{OE2}$	Y	1.4	5.3	6.3	1.5	3.5	5.2	6.2	ns
$t_{PZL}$			1.4	5.4	6	1.5	3.7	5.3	5.9	
$t_{PHZ}$	$\overline{OE1}$ or $\overline{OE2}$	Y	1.4	5.8	6.1	1.5	3.9	5.6	5.9	ns
$t_{PLZ}$			1.4	5.4	5.7	1.5	3	5	5.3	

† All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

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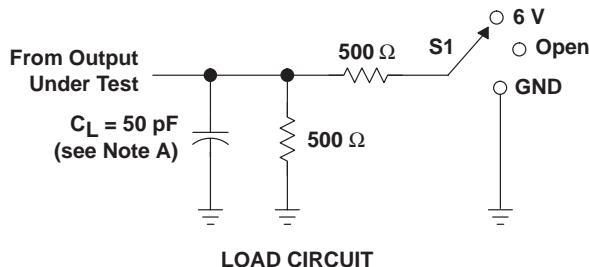


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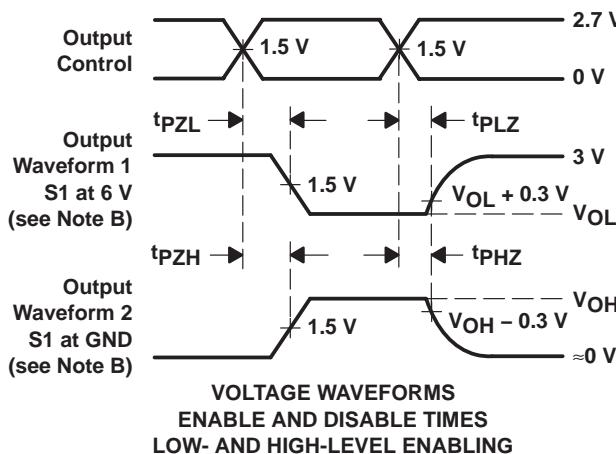
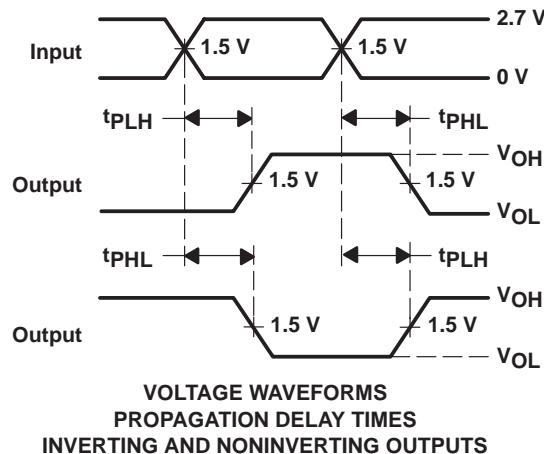
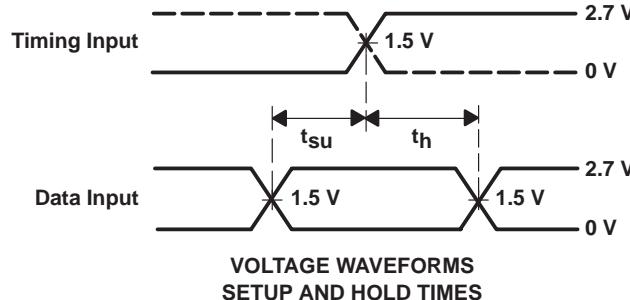
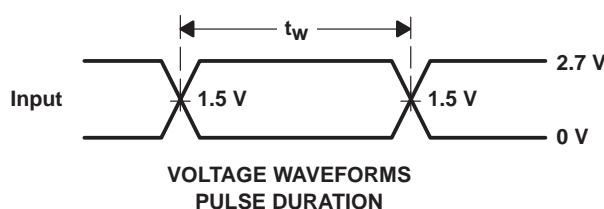
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**PARAMETER MEASUREMENT INFORMATION**



TEST	S1
$t_{PHL}/t_{PLH}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- The outputs are measured one at a time with one transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LVTH541DBR</a>	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH541
SN74LVTH541DBR.B	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH541
<a href="#">SN74LVTH541DW</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH541
SN74LVTH541DW.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH541
<a href="#">SN74LVTH541DWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH541
SN74LVTH541DWR.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH541
<a href="#">SN74LVTH541NSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH541
SN74LVTH541NSR.B	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH541
<a href="#">SN74LVTH541PW</a>	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH541
SN74LVTH541PW.B	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH541
<a href="#">SN74LVTH541PWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH541
SN74LVTH541PWR.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH541
<a href="#">SN74LVTH541PWRG4</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH541
SN74LVTH541PWRG4.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH541

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

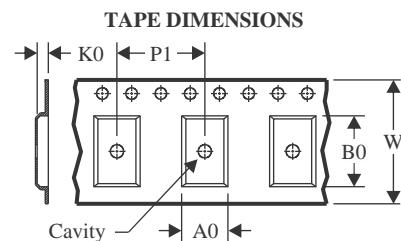
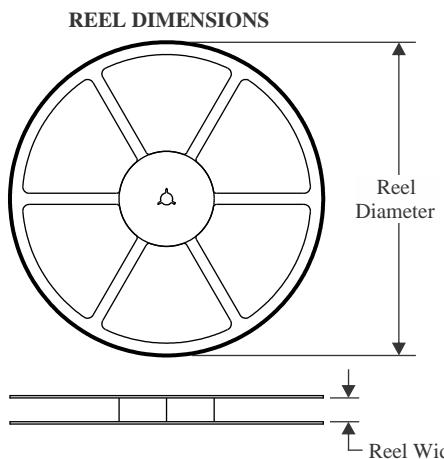
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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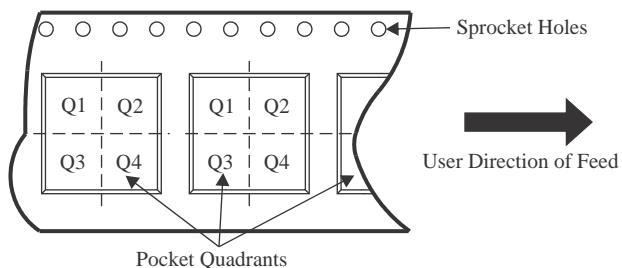
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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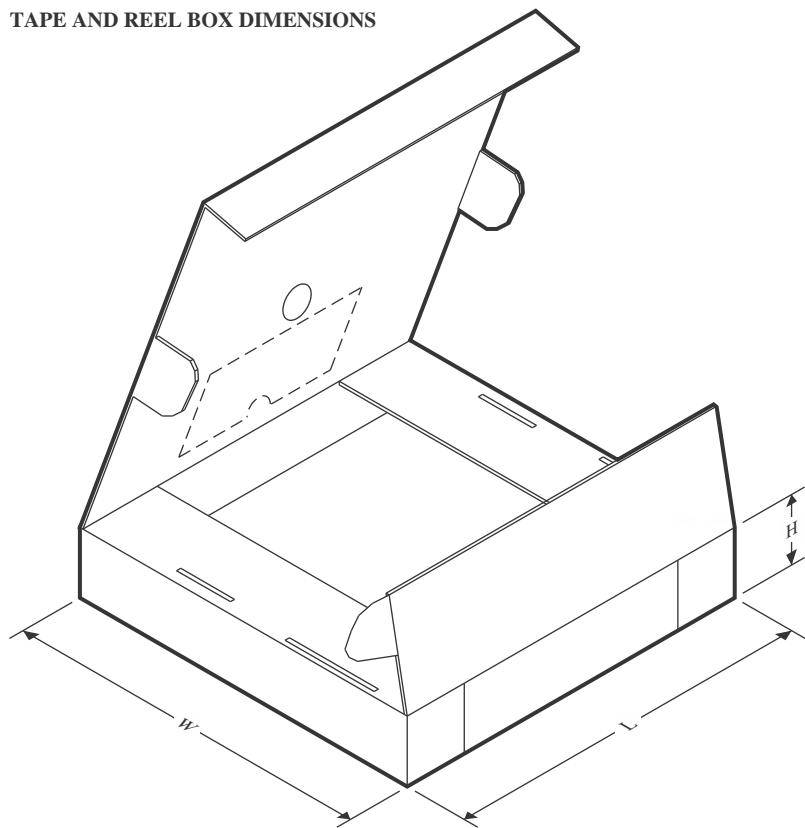
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


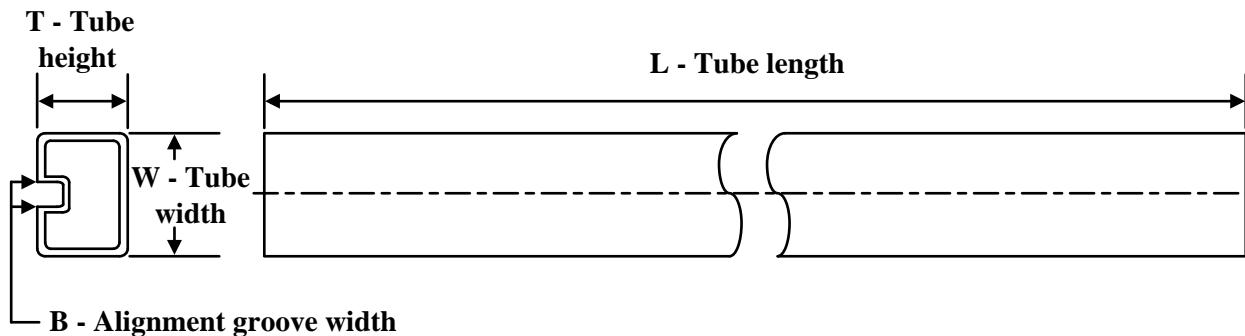
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH541DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVTH541DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVTH541NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVTH541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVTH541PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH541DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LVTH541DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LVTH541NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LVTH541PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVTH541PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
SN74LVTH541DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVTH541DW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVTH541PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVTH541PW.B	PW	TSSOP	20	70	530	10.2	3600	3.5

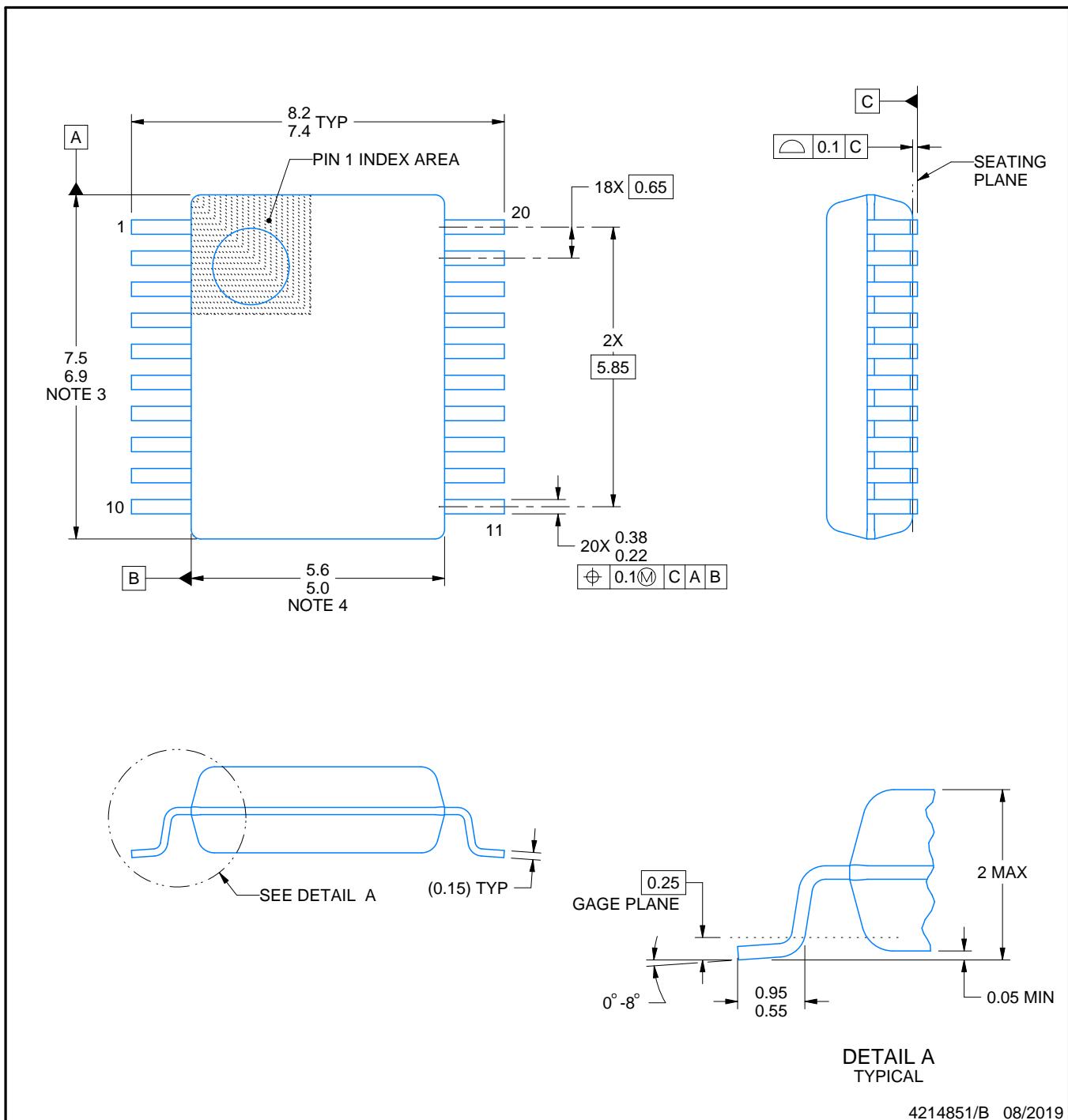
# PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

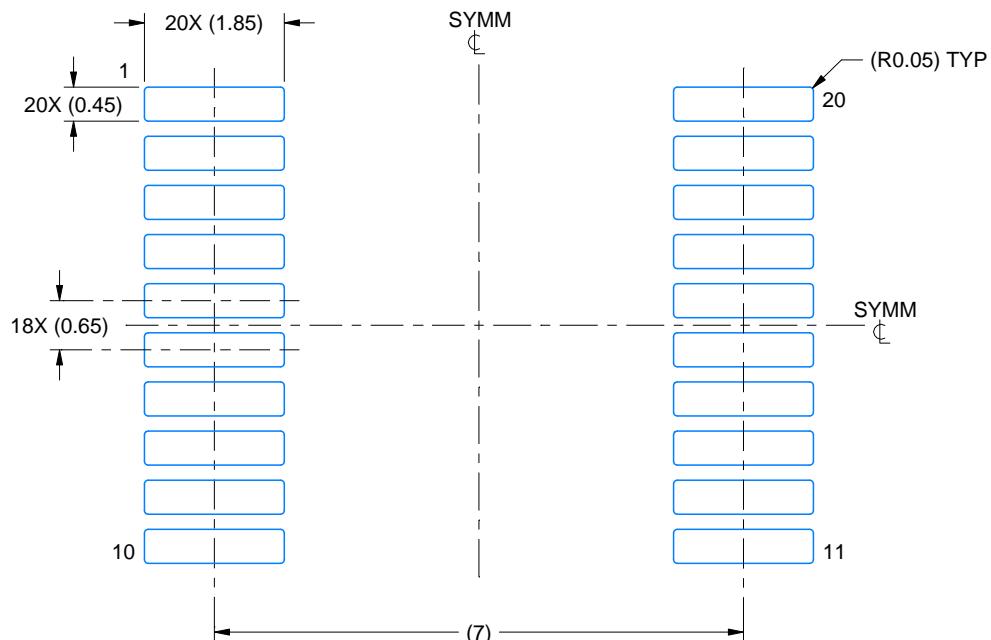
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

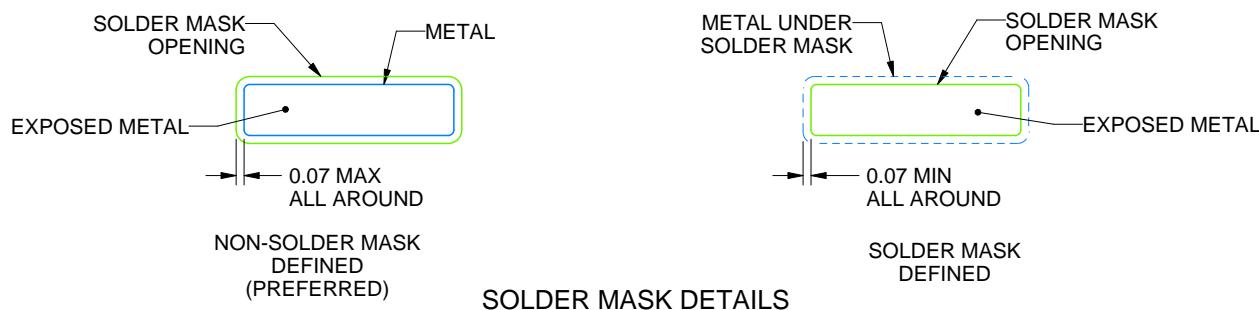
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

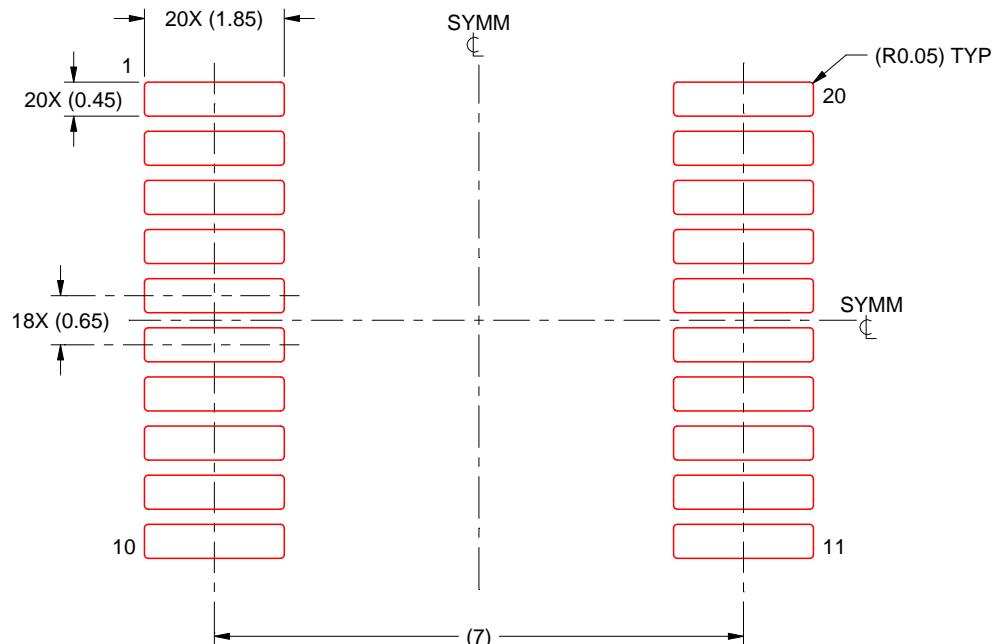
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**DB0020A**

## SSOP - 2 mm max height

## SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X**

4214851/B 08/2019

#### NOTES: (continued)

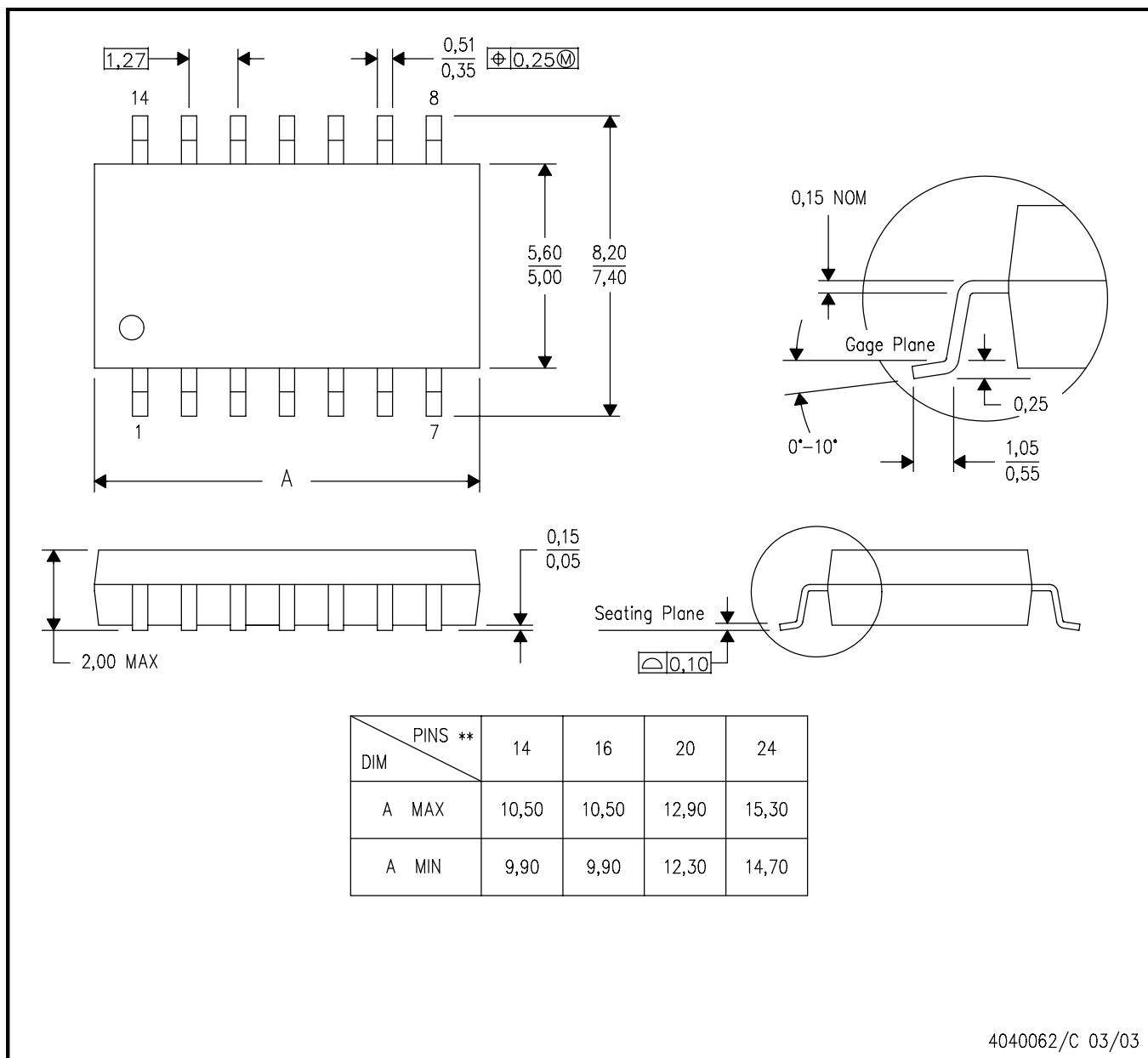
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

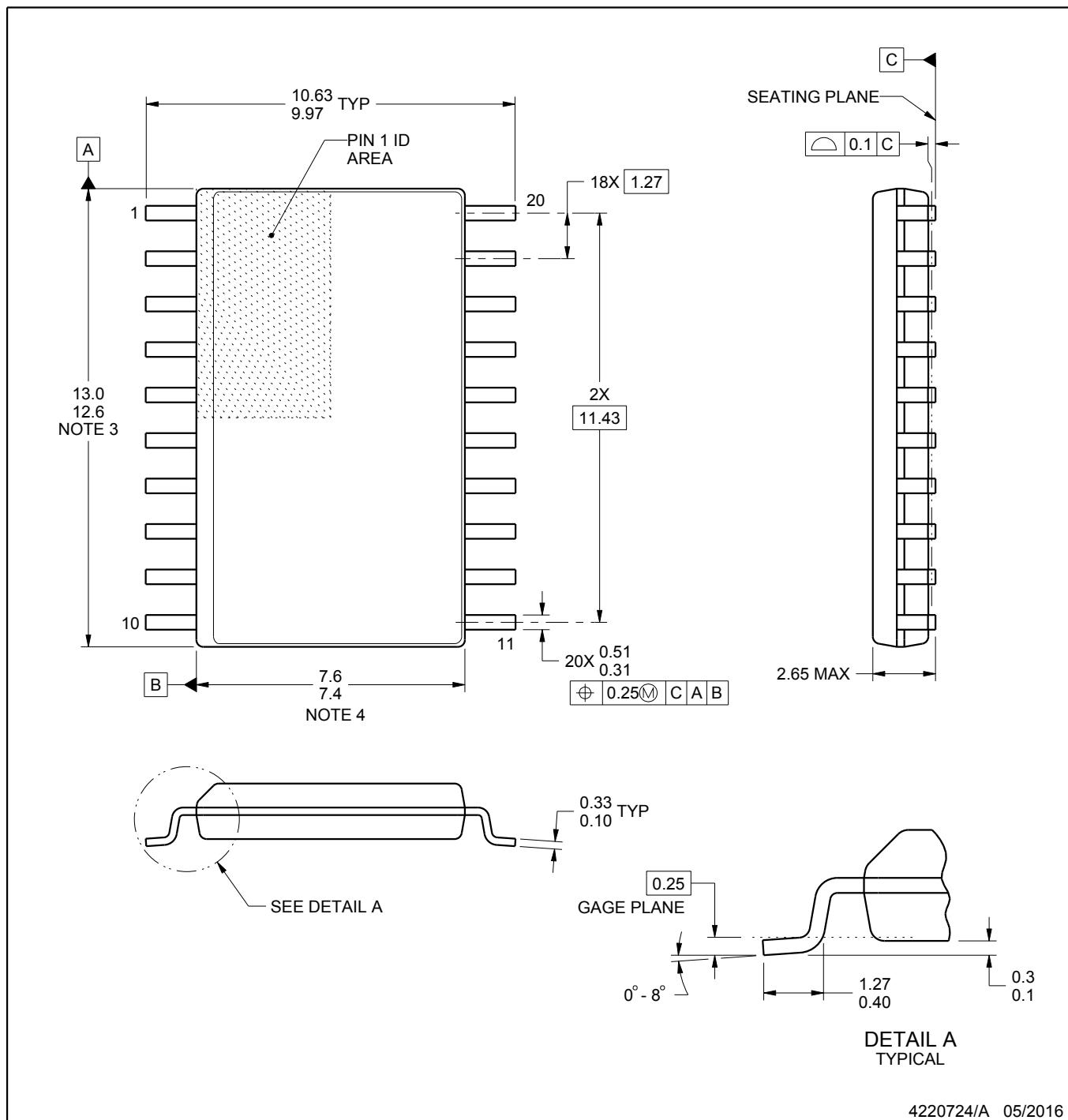


## PACKAGE OUTLINE

**DW0020A**

## **SOIC - 2.65 mm max height**

SOIG



## NOTES:

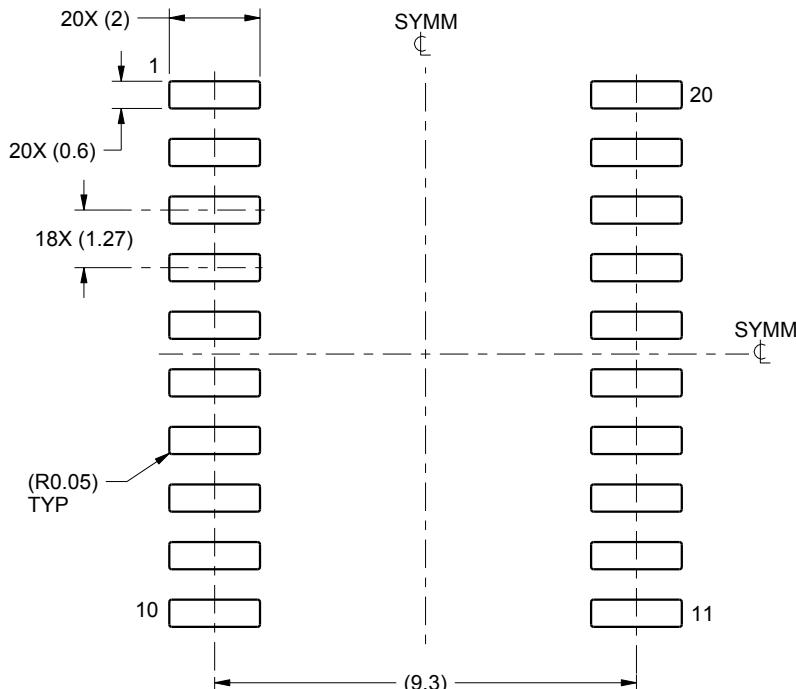
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

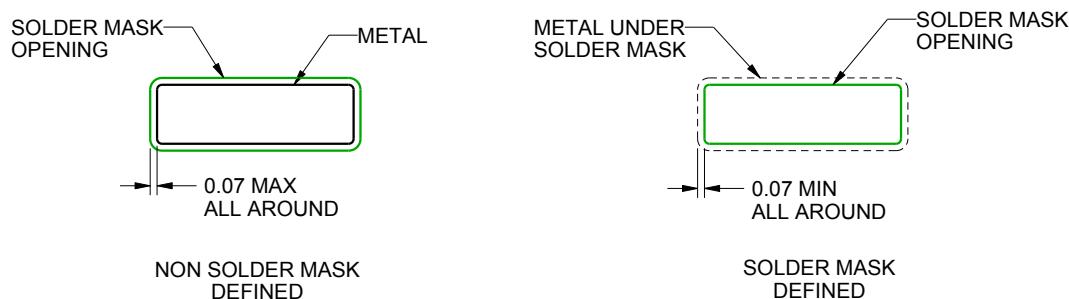
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

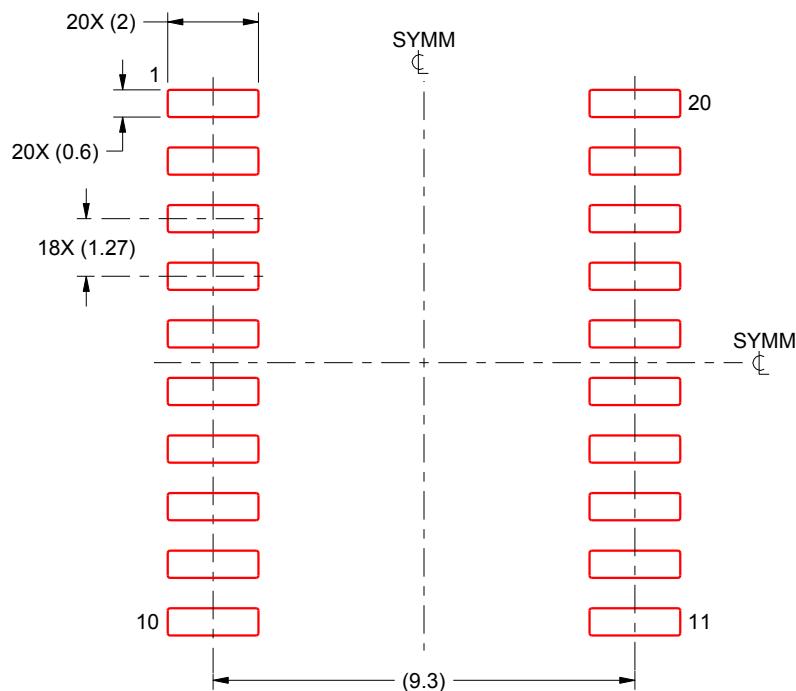
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

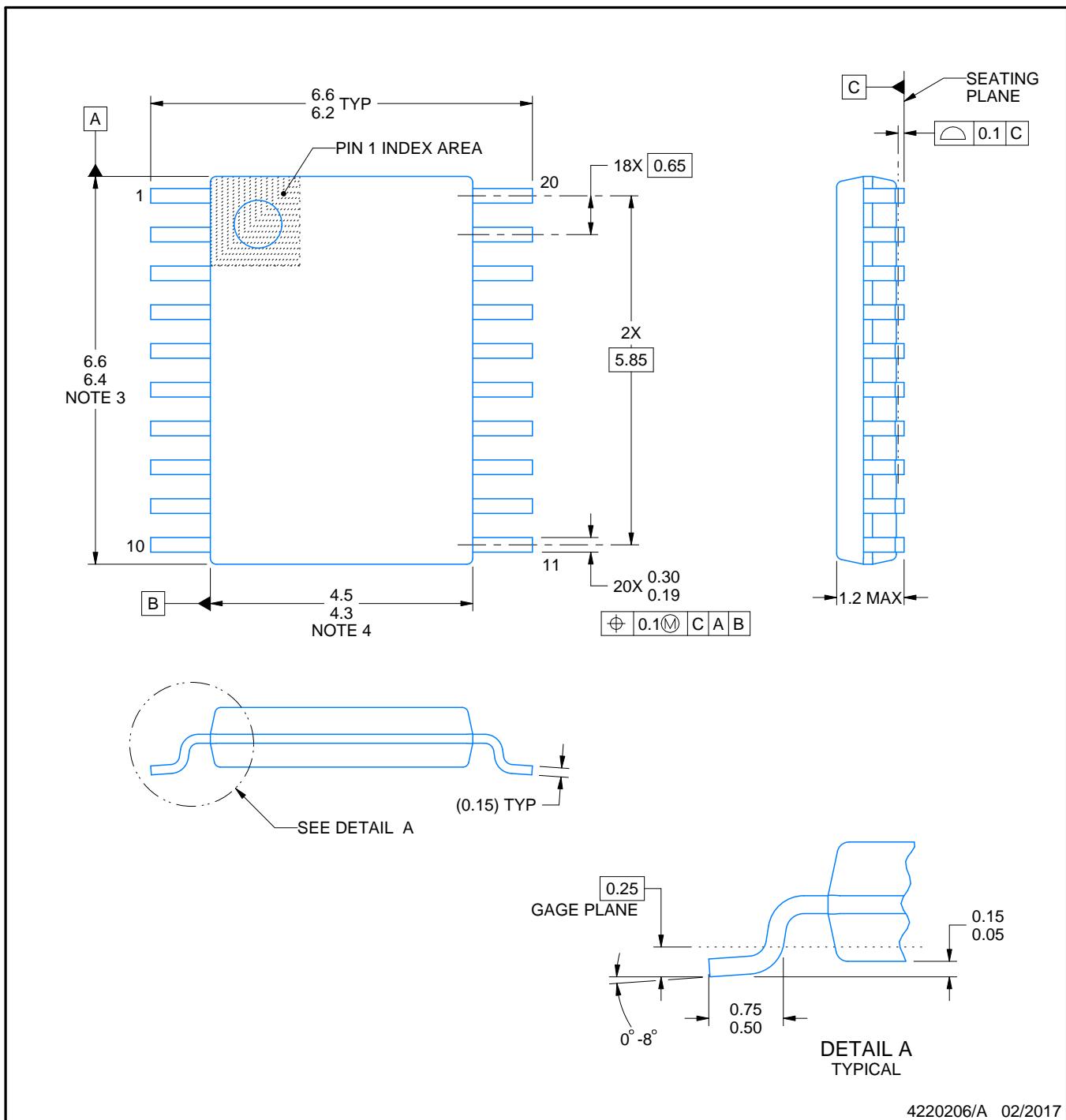
## PACKAGE OUTLINE

**PW0020A**



## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



## NOTES:

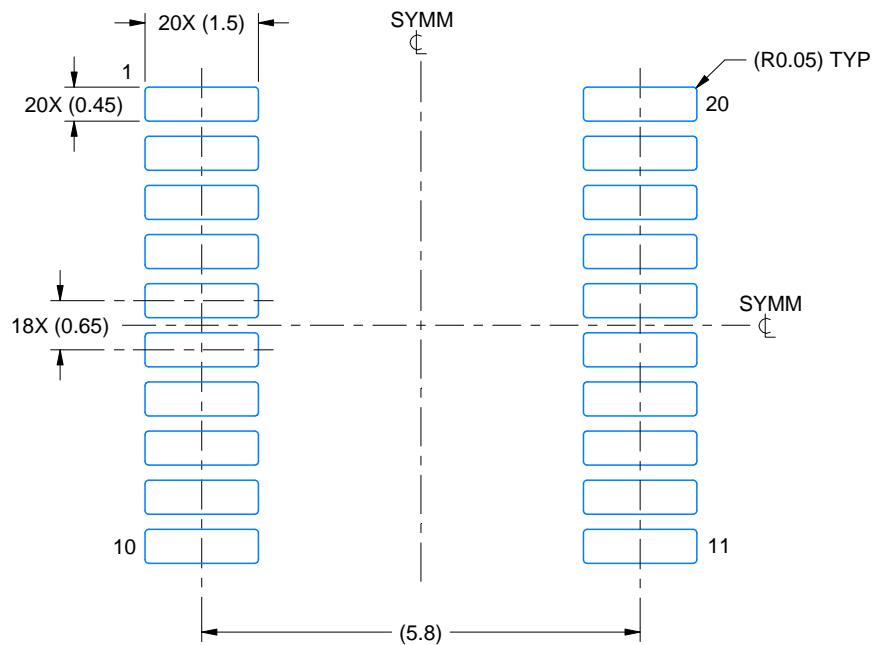
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

## EXAMPLE BOARD LAYOUT

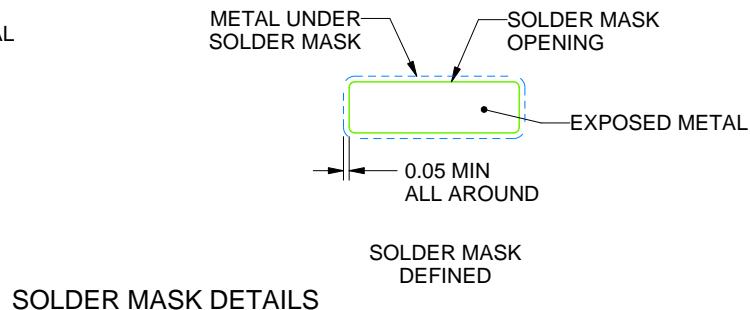
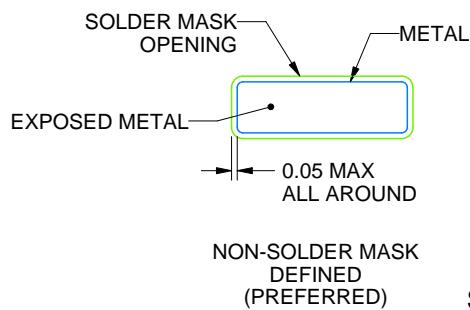
**PW0020A**

## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

#### NOTES: (continued)

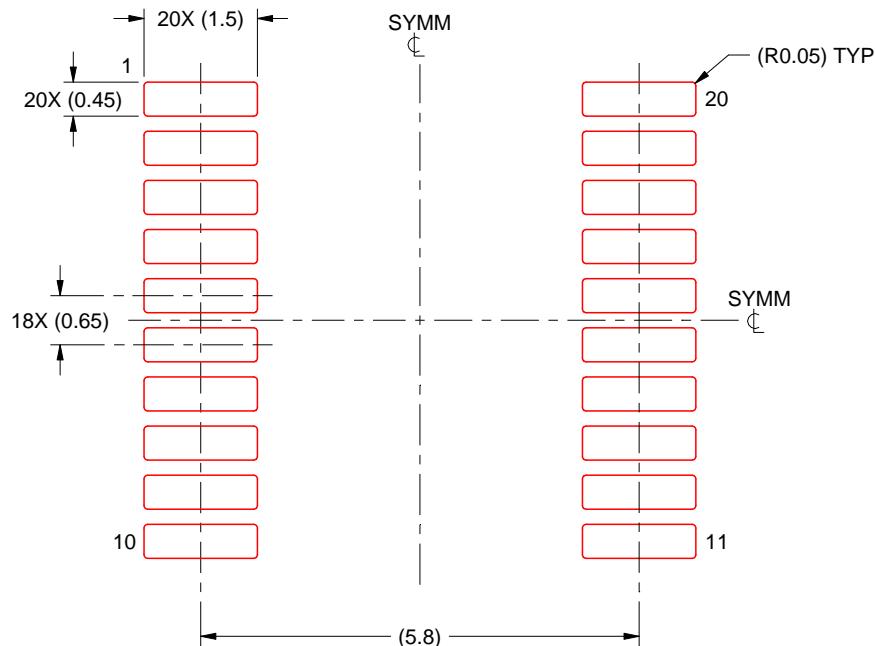
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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