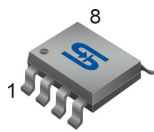


SOP-8



Pin Definition:

- | | |
|-----------|----------|
| 1. Source | 8. Drain |
| 2. Source | 7. Drain |
| 3. Source | 6. Drain |
| 4. Gate | 5. Drain |

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (m Ω)	I_D (A)
-30	5.2 @ $V_{GS} = -10V$	-17
	9.5 @ $V_{GS} = -4.5V$	

Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

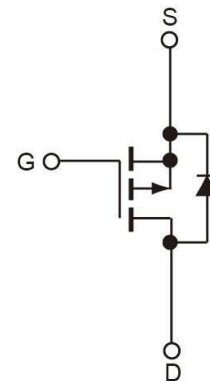
- DC-DC Converter
- Battery Power System

Ordering Information

Part No.	Package	Packing
TSM4459CS RLG	SOP-8	2.5Kpcs / 13" Reel

Note: "G" denote for Halogen Free Product

Block Diagram



P-Channel MOSFET

Absolute Maximum Rating ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	-68	A
Maximum Power Dissipation ^{Note a.}	P_D	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Ambient Thermal Resistance ^{Note a.}	$R\theta_{JA}$	50	$^\circ\text{C/W}$

Notes:

a. The Device Surface Mounted on 1inch² FR4 Board with 2oz copper.

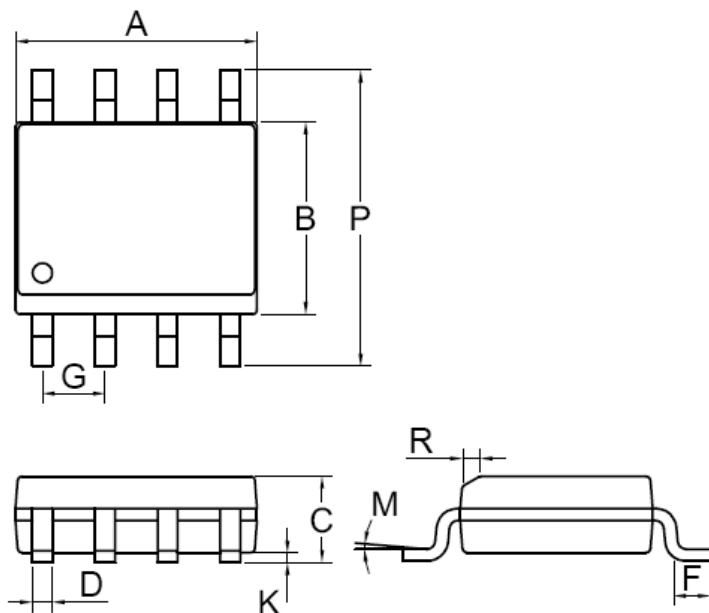
Electrical Specifications ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV_{DSS}	-30	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-1	--	-3	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = -30V, V_{GS} = 0V$	I_{DSS}	--	--	-1.0	μA
Drain-Source On-State Resistance ^a	$V_{GS} = -10V, I_D = -9A$	$R_{DS(ON)}$	--	4	5.2	m Ω
	$V_{GS} = -4.5V, I_D = -9A$		--	7	9.5	
Diode Forward Voltage	$I_S = -18A, V_{GS} = 0V$	V_{SD}	--	0.8	--	V
Dynamic						
Total Gate Charge	$V_{DS} = -24V, I_D = -17A,$ $V_{GS} = -4.5V$	Q_g	--	78.4	--	nC
Gate-Source Charge		Q_{gs}	--	25.1	--	
Gate-Drain Charge		Q_{gd}	--	38.7	--	
Gate Resistance	$f = 1.0MHz$	R_g	--	2.88	--	Ω
Input Capacitance	$V_{DS} = -15V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	6205	--	pF
Output Capacitance		C_{oss}	--	963	--	
Reverse Transfer Capacitance		C_{rss}	--	330	--	
Switching						
Turn-On Delay Time	$V_{DD} = -15V, R_L = 15\Omega,$ $V_{GEN} = -10V,$ $R_G = 4.7\Omega$	$t_{d(on)}$	--	75.2	--	nS
Turn-On Rise Time		t_r	--	33.8	--	
Turn-Off Delay Time		$t_{d(off)}$	--	275	--	
Turn-Off Fall Time		t_f	--	92.1	--	

Notes:

a. pulse test: $PW \leq 300\mu\text{S}$, duty cycle $\leq 2\%$

SOP-8 Mechanical Drawing



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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