

NTLJD3115P

MOSFET – Power, Dual, P-Channel, WDFN 2X2 mm -20 V, -4.1 A

Features

- WDFN Package Provides Exposed Drain Pad for Excellent Thermal Conduction
- 2x2 mm Footprint Same as SC-88
- Lowest $R_{DS(on)}$ Solution in 2x2 mm Package
- 1.8 V $R_{DS(on)}$ Rating for Operation at Low Voltage Gate Drive Logic Level
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- Bidirectional Current Flow with Common Source Configuration
- This is a Pb-Free Device

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment
- Li-Ion Battery Charging and Protection Circuits
- High Side Load Switch

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	−20	V
Gate-to-Source Voltage			V _{GS}	±8.0	V
Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	−3.3	A
		T _A = 85°C		−2.4	
	t ≤ 5 s	T _A = 25°C		−4.1	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.5	W
	t ≤ 5 s			2.3	
Continuous Drain Current (Note 2)	Steady State	T _A = 25°C	I _D	−2.3	A
		T _A = 85°C		−1.6	
Power Dissipation (Note 2)	Steady State	T _A = 25°C	P _D	0.71	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	−20	A
Operating Junction and Storage Temperature			T _J , T _{STG}	−55 to 150	°C
Source Current (Body Diode) (Note 2)			I _S	−1.9	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

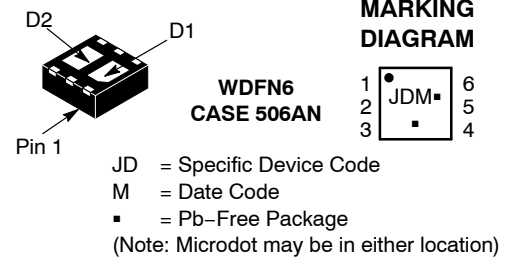
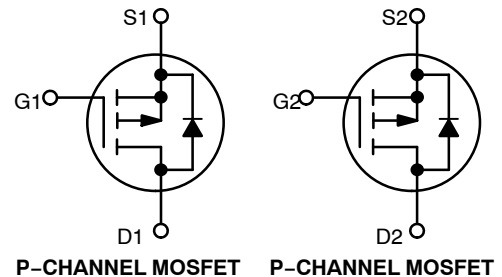
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm², 2 oz Cu.



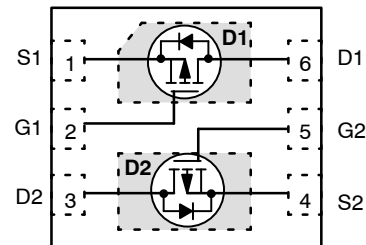
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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX (Note 1)
-20 V	100 m Ω @ -4.5 V	-4.1 A
	135 m Ω @ -2.5 V	
	200 m Ω @ -1.8 V	



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NTLJD3115PT1G	WDFN6 (Pb-Free)	3000/Tape & Reel
NTLJD3115PTAG	WDFN6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
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SINGLE OPERATION (SELF-HEATED)

Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	83	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	177	
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	54	

DUAL OPERATION (EQUALLY HEATED)

Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	58	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	133	
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	40	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).

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MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = -250 μA, Ref to 25°C		9.95		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V	T _J = 25°C		-1.0	μA
			T _J = 85°C		-10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8.0 V			±100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250 μA	-0.4	-0.7	-1.0	V
Negative Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J			2.44		mV/°C
Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -2.0 A		75	100	mΩ
		V _{GS} = -2.5 V, I _D = -2.0 A		101	135	
		V _{GS} = -1.8 V, I _D = -1.6 A		150	200	
Forward Transconductance	g _{FS}	V _{DS} = -5.0 V, I _D = -2.0 A		6.0		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = -10 V		531		pF
Output Capacitance	C _{OSS}			91		
Reverse Transfer Capacitance	C _{RSS}			56		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -2.0 A		5.5	6.2	nC
Threshold Gate Charge	Q _{G(TH)}			0.7		
Gate-to-Source Charge	Q _{GS}			1.0		
Gate-to-Drain Charge	Q _{GD}			1.4		
Gate Resistance	R _G			8.8		Ω

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = -4.5 V, V _{DD} = -5.0 V, I _D = -1.0 A, R _G = 6.0 Ω		6.0		ns
Rise Time	t _r			11		
Turn-Off Delay Time	t _{d(OFF)}			21		
Fall Time	t _f			8.0		
Turn-On Delay Time	t _{d(ON)}	V _{GS} = -4.5 V, V _{DD} = -10 V, I _D = -2.0 A, R _G = 2.0 Ω		6.0		ns
Rise Time	t _r			12		
Turn-Off Delay Time	t _{d(OFF)}			19		
Fall Time	t _f			6.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Recovery Voltage	V _{SD}	V _{GS} = 0 V, I _S = -1.0 A	T _J = 25°C	-0.75	-1.0	V
			T _J = 125°C	-0.64		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _{SD} /dI _t = 100 A/μs, I _S = -1.0 A		12.6		ns
Charge Time	t _a			7.0		
Discharge Time	t _b			5.6		
Reverse Recovery Time	Q _{RR}			5.0		nC

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

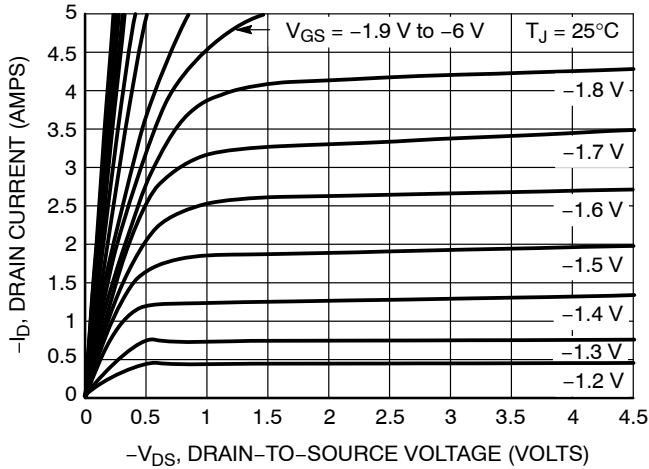


Figure 1. On-Region Characteristics

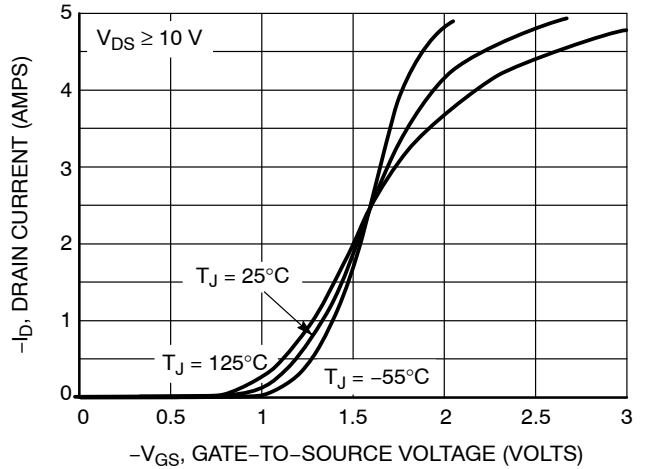


Figure 2. Transfer Characteristics

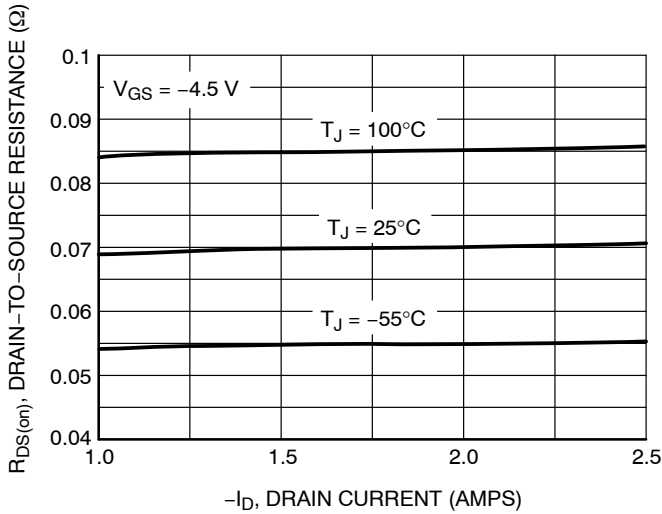


Figure 3. On-Resistance versus Drain Current

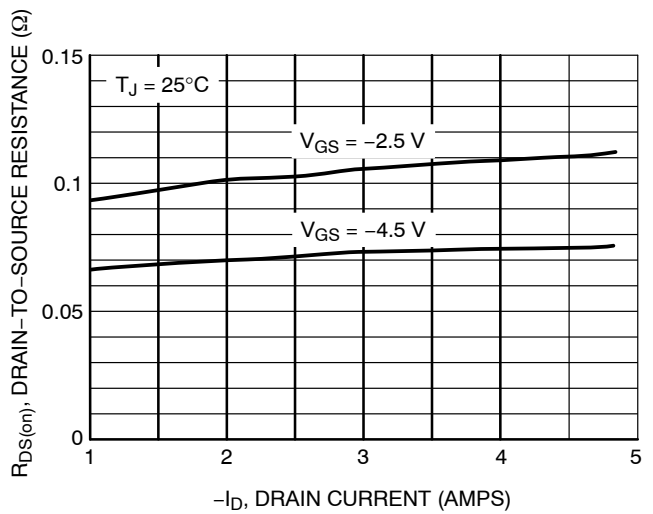


Figure 4. On-Resistance versus Drain Current and Gate Voltage

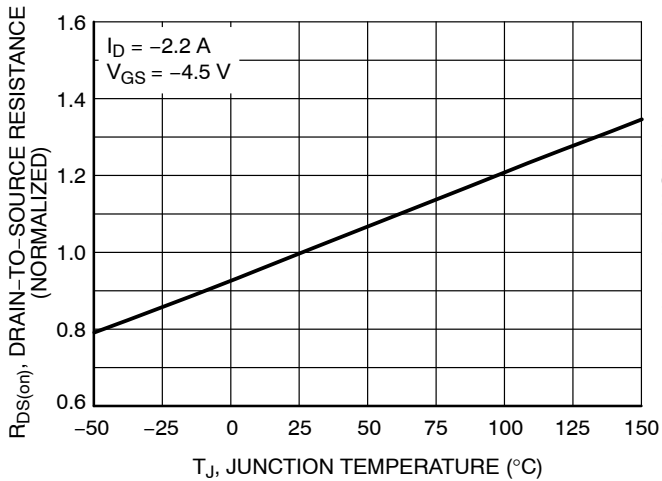


Figure 5. On-Resistance Variation with Temperature

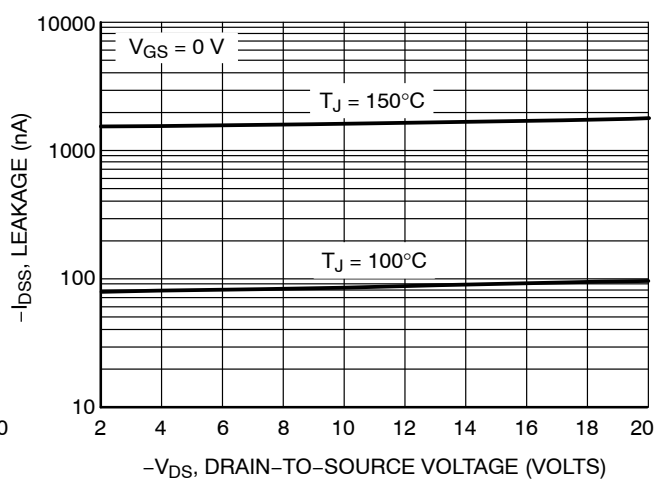


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

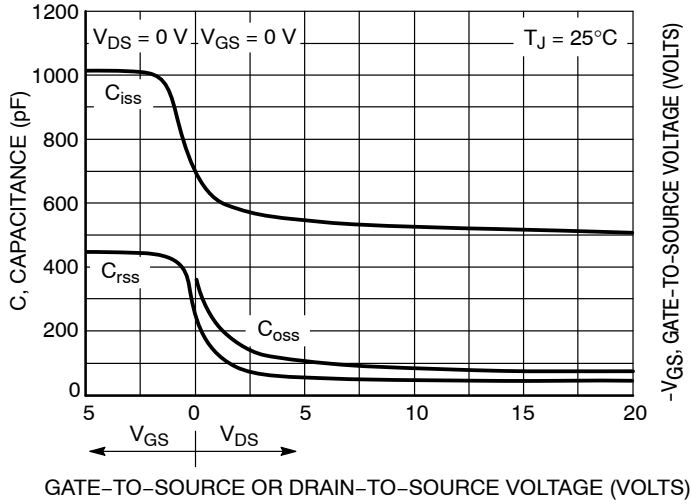


Figure 7. Capacitance Variation

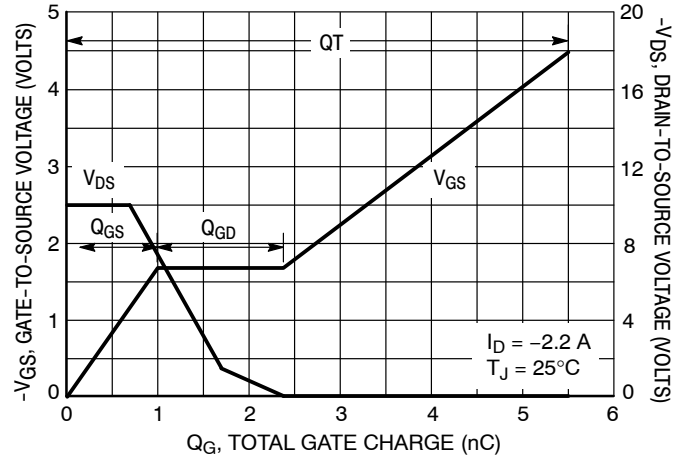


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

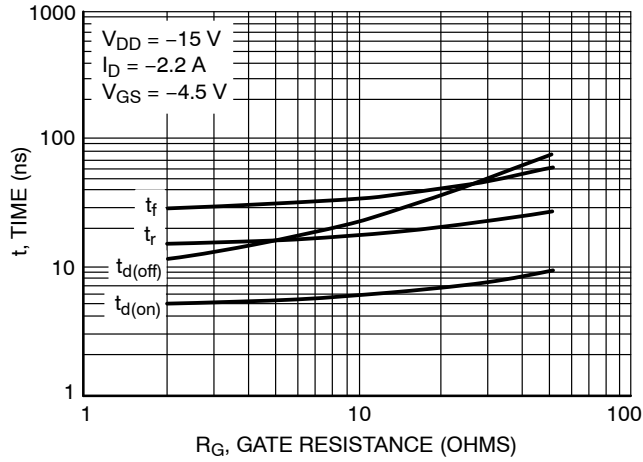


Figure 9. Resistive Switching Time Variation versus Gate Resistance

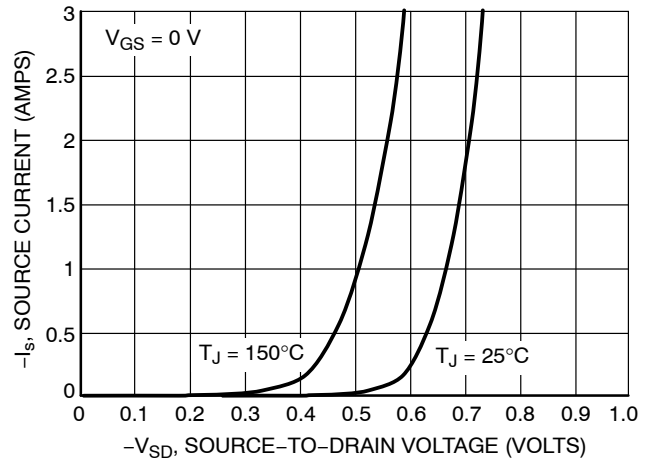


Figure 10. Diode Forward Voltage versus Current

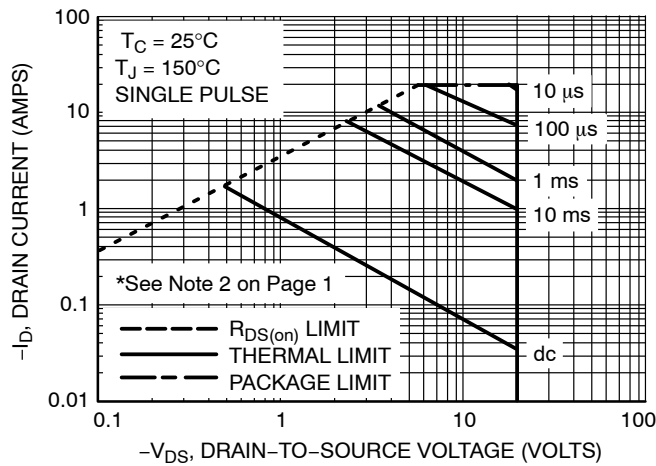


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

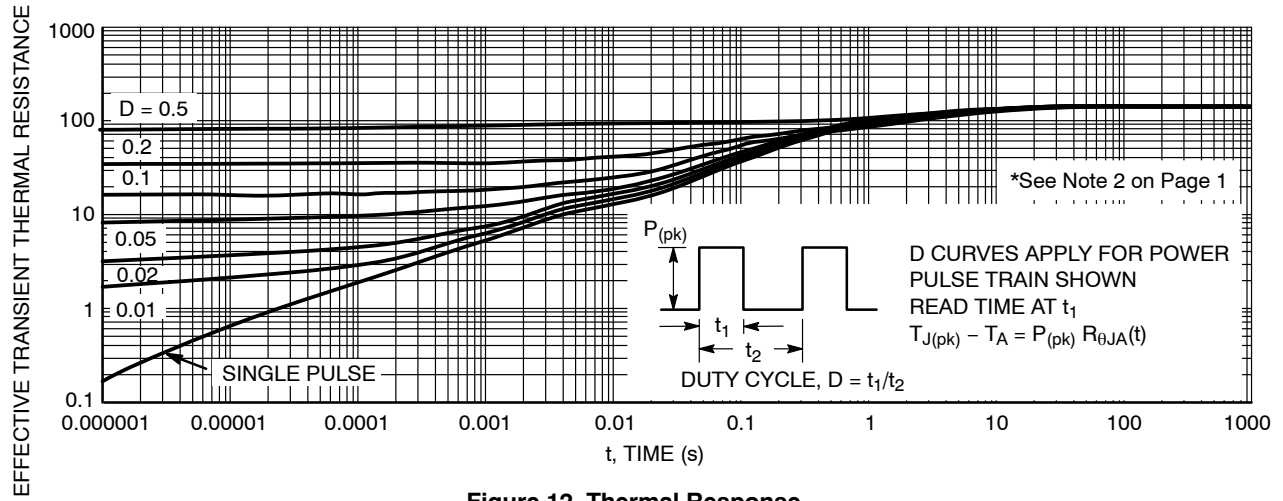
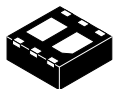
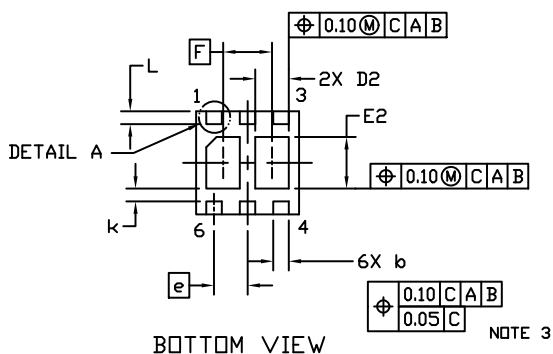
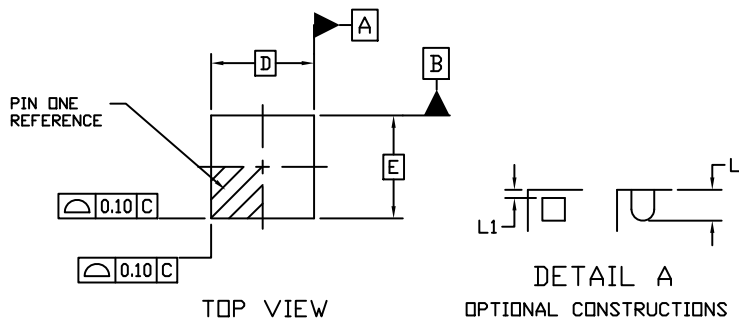


Figure 12. Thermal Response



WDFN6 2x2, 0.65P
CASE 506AN
ISSUE H

DATE 25 JAN 2022



GENERIC
MARKING DIAGRAM*



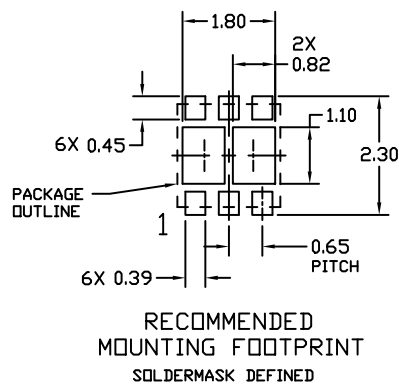
XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN.	MAX.
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.95 BSC	
k	0.25 REF	
L	0.20	0.30
L1	---	0.10



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