

# CD4011A, CD4012A, CD4023A Types

## CMOS NAND Gates

Quad 2 Input — CD4011A  
Dual 4 Input — CD4012A  
Triple 3 Input — CD4023A

The TI-CD4011A, CD4012A, and CD4023A NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of CMOS gates.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

### Features:

- Quiescent current specified to 15  $\mu$ A
- Maximum input leakage of 1  $\mu$ A at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| Characteristic                                             | Min. | Max. | Units |
|------------------------------------------------------------|------|------|-------|
| Supply Voltage Range (over full package temperature range) | 3    | 12   | V     |

### MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE ( $T_{stg}$ ) ..... -65 to +150°C  
OPERATING-TEMPERATURE RANGE ( $T_A$ ):  
PACKAGE TYPES D, F, K, H ..... -55 to +125°C  
PACKAGE TYPE E ..... -40 to +85°C  
DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )  
(Voltages referenced to  $V_{SS}$  Terminal) ..... -0.5 to +15 V  
POWER DISSIPATION PER PACKAGE ( $P_D$ ):  
FOR  $T_A = -40$  to +60°C (PACKAGE TYPE E) ..... 500 mW  
FOR  $T_A = +60$  to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW  
FOR  $T_A = -55$  to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW  
FOR  $T_A = +100$  to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW  
DEVICE DISSIPATION PER OUTPUT TRANSISTOR  
FOR  $T_A =$  FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW  
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to  $V_{DD} + 0.5$  V  
LEAD TEMPERATURE (DURING SOLDERING):  
At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79 mm) from case for 10 s max ..... +265°C

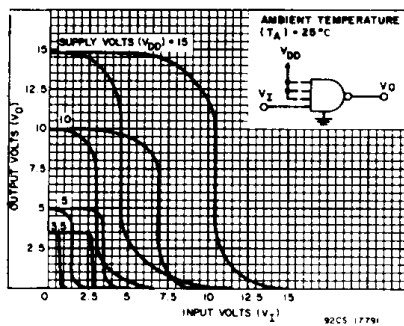


Fig. 2 — Minimum & maximum voltage transfer characteristics.

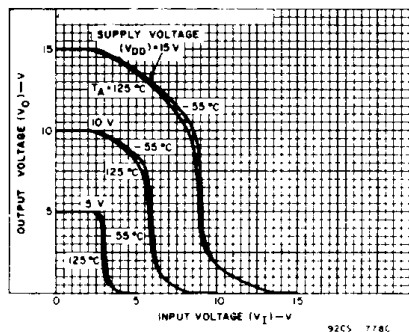


Fig. 3 — Typical voltage transfer characteristics as a function of temperature.

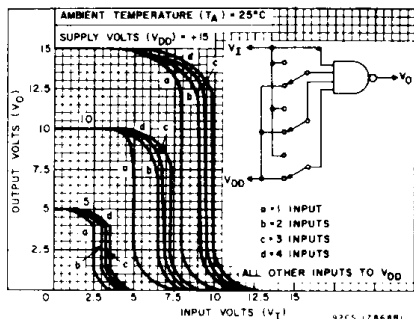


Fig. 4 — Typical multiple input switching transfer characteristics for CD4012A.

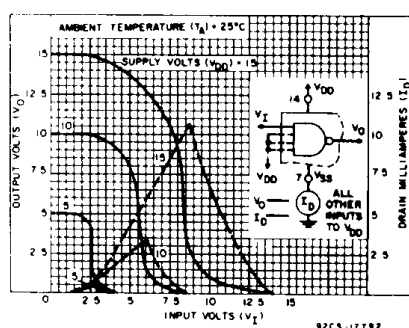


Fig. 5 — Typical current & voltage transfer characteristics.

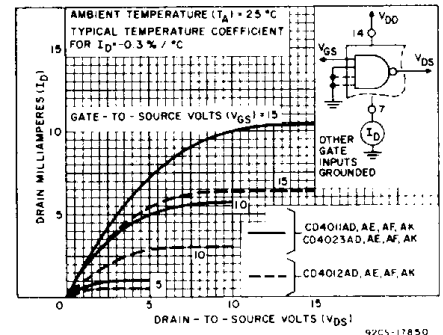
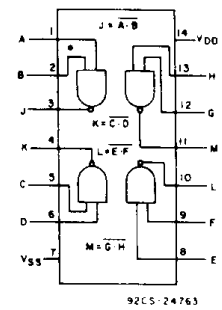
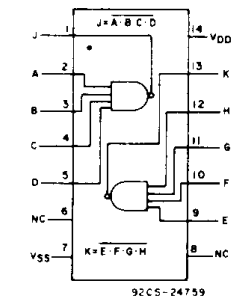


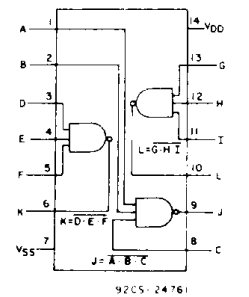
Fig. 6 — Typical n-channel drain characteristics.



CD4011A

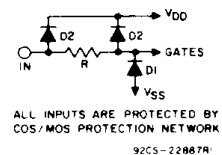


CD4012A



CD4023AH

Fig. 1 — Functional diagrams.



92CS-22887R

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## STATIC ELECTRICAL CHARACTERISTICS

| Characteristic                                                          | Conditions            |                        |                        | Limits at Indicated Temperatures (°C) |       |       |        |           |       |       |        | Units |
|-------------------------------------------------------------------------|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|--------|-----------|-------|-------|--------|-------|
|                                                                         |                       |                        |                        | D,F,K,H Packages                      |       |       |        | E Package |       |       |        |       |
|                                                                         | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>DD</sub><br>(V) | -55                                   | +25   |       | +125   | -40       | +25   |       | +85    |       |
|                                                                         |                       |                        |                        | Typ.                                  | Limit |       |        | Typ.      | Limit |       |        |       |
| Quiescent Device<br>Current, I <sub>L</sub> Max.                        | —                     | —                      | 5                      | 0.05                                  | 0.001 | 0.05  | 3      | 0.5       | 0.005 | 0.5   | 15     | μA    |
|                                                                         | —                     | —                      | 10                     | 0.1                                   | 0.001 | 0.1   | 6      | 5         | 0.005 | 5     | 30     |       |
|                                                                         | —                     | —                      | 15                     | 2                                     | 0.02  | 2     | 40     | 50        | 0.5   | 50    | 500    |       |
| Output Voltage:<br>Low-Level<br>V <sub>OL</sub>                         | —                     | 0,5                    | 5                      | 0 Typ.; 0.05 Max.                     |       |       |        |           |       |       |        | V     |
|                                                                         | —                     | 0,10                   | 10                     | 0 Typ.; 0.05 Max.                     |       |       |        |           |       |       |        |       |
| High Level,<br>V <sub>OH</sub>                                          | —                     | 0,5                    | 5                      | 4.95 Min.; 5 Typ.                     |       |       |        |           |       |       |        | V     |
|                                                                         | —                     | 0,10                   | 10                     | 9.95 Min.; 10 Typ.                    |       |       |        |           |       |       |        |       |
| Noise Immunity:<br>Inputs Low,<br>V <sub>NL</sub>                       | 3.6                   | —                      | 5                      | 1.5 Min.; 2.25 Typ.                   |       |       |        |           |       |       |        | V     |
|                                                                         | 7.2                   | —                      | 10                     | 3 Min.; 4.5 Typ.                      |       |       |        |           |       |       |        |       |
| Inputs High,<br>V <sub>NH</sub>                                         | 1.4                   | —                      | 5                      | 1.5 Min.; 2.25 Typ.;                  |       |       |        |           |       |       |        | V     |
|                                                                         | 2.8                   | —                      | 10                     | 3 Min.; 4.5 Typ.                      |       |       |        |           |       |       |        |       |
| Noise Margin:<br>Inputs Low,<br>V <sub>NML</sub>                        | 4.5                   | —                      | 5                      | 1 Min.                                |       |       |        |           |       |       |        | V     |
|                                                                         | 9                     | —                      | 10                     | 1 Min.                                |       |       |        |           |       |       |        |       |
| Inputs High,<br>V <sub>NMH</sub>                                        | 0.5                   | —                      | 5                      | 1 Min.                                |       |       |        |           |       |       |        | V     |
|                                                                         | 1                     | —                      | 10                     | 1 Min.                                |       |       |        |           |       |       |        |       |
| Output Drive<br>Current:<br>N-Channel<br>(Sink)<br>I <sub>DN</sub> Min. |                       |                        |                        |                                       |       |       |        |           |       |       |        | mA    |
| CD4011A                                                                 | 0.5                   | —                      | 5                      | 0.31                                  | 0.5   | 0.25  | 0.175  | 0.145     | 0.5   | 0.12  | 0.095  |       |
| CD4023A                                                                 | 0.5                   | —                      | 10                     | 0.62                                  | 0.6   | 0.5   | 0.35   | 0.3       | 0.6   | 0.25  | 0.2    |       |
| CD4012A                                                                 | 0.5                   | —                      | 5                      | 0.15                                  | 0.25  | 0.12  | 0.085  | 0.072     | 0.25  | 0.06  | 0.05   |       |
|                                                                         | 0.5                   | —                      | 10                     | 0.31                                  | 0.6   | 0.25  | 0.175  | 0.155     | 0.6   | 0.13  | 0.105  |       |
| P-Channel<br>(Source),<br>I <sub>DP</sub> Min.                          | 4.5                   | —                      | 5                      | -0.31                                 | -0.5  | -0.25 | -0.175 | -0.145    | -0.5  | -0.12 | -0.095 |       |
| All Types                                                               | 9.5                   | —                      | 10                     | -0.75                                 | -1.2  | -0.6  | -0.4   | -0.35     | -1.2  | -0.3  | -0.24  |       |
| Input Leakage<br>Current,<br>I <sub>IL</sub> , I <sub>IH</sub>          | Any<br>Input          |                        | 15                     | ±10 <sup>-5</sup> Typ.; ±1 Max.       |       |       |        |           |       |       |        | μA    |

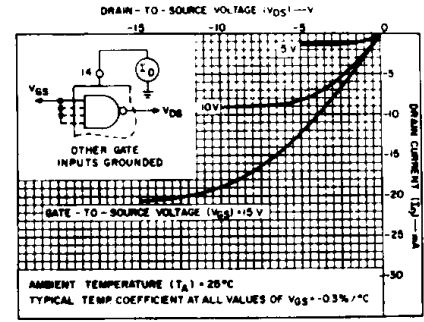


Fig. 7 - Typical p-channel drain characteristics.

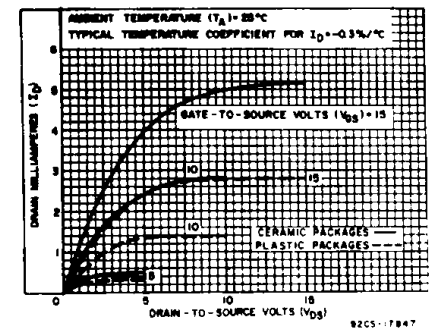


Fig. 8 - Minimum n-channel drain characteristics - CD4011A & CD4023A.

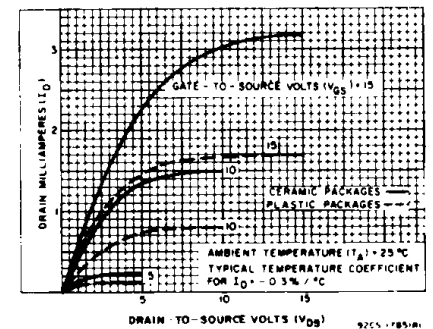


Fig. 9 - Minimum n-channel drain characteristics.

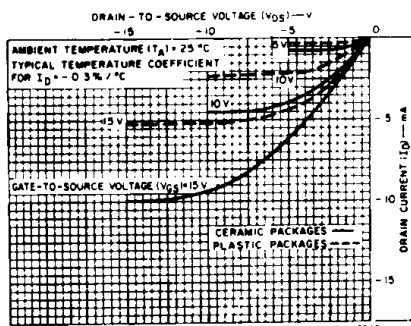


Fig. 10 - Minimum p-channel drain characteristics.

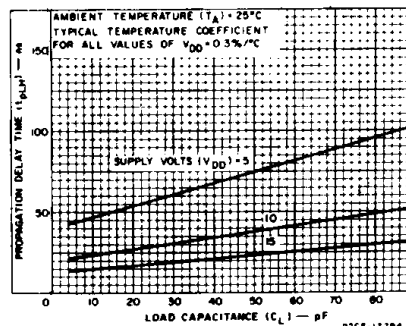


Fig. 11 - Typical low-to-high level propagation delay time vs. C<sub>L</sub>.

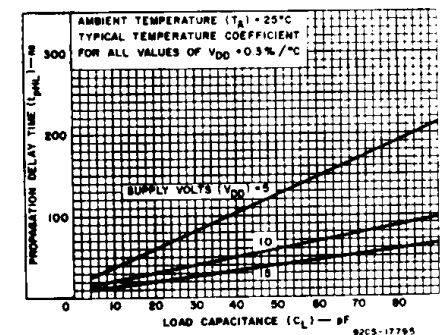


Fig. 12 - Typical high-to-low level propagation delay time vs. C<sub>L</sub> - CD4011A, & CD4023A.

# CD4011A, CD4012A, CD4023A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15\text{ pF}$ , Input  $t_r, t_f = 20\text{ ns}$ ,  
 $R_L = 200\text{ k}\Omega$

| CHARACTERISTICS                                                | TEST<br>CONDITIONS | LIMITS                 |      |      |              |      | UNITS |
|----------------------------------------------------------------|--------------------|------------------------|------|------|--------------|------|-------|
|                                                                |                    | D, F, K, H<br>Packages |      |      | E<br>Package |      |       |
|                                                                |                    | VDD<br>(V)             | Typ. | Max. | Typ.         | Max. |       |
| Propagation Delay Time:<br>Low-to-High Level, t <sub>PLH</sub> |                    | 5                      | 50   | 75   | 50           | 100  | ns    |
|                                                                |                    | 10                     | 25   | 40   | 25           | 50   |       |
| High-to-Low Level, t <sub>PHL</sub><br>CD4011A and CD4023A     |                    | 5                      | 50   | 75   | 50           | 100  | ns    |
|                                                                |                    | 10                     | 25   | 40   | 25           | 50   |       |
| CD4012A                                                        |                    | 5                      | 100  | 150  | 100          | 200  | ns    |
|                                                                |                    | 10                     | 50   | 75   | 50           | 100  |       |
| Transition Time:<br>Low-to-High Level, t <sub>TLH</sub>        |                    | 5                      | 75   | 100  | 75           | 125  | ns    |
|                                                                |                    | 10                     | 40   | 60   | 40           | 75   |       |
| High-to-Low Level, t <sub>THL</sub><br>CD4011A and CD4023A     |                    | 5                      | 75   | 125  | 75           | 150  | ns    |
|                                                                |                    | 10                     | 50   | 75   | 50           | 100  |       |
| CD4012A                                                        |                    | 5                      | 250  | 375  | 250          | 500  | ns    |
|                                                                |                    | 10                     | 125  | 200  | 125          | 250  |       |
| Input Capacitance, C <sub>i</sub>                              | Any Input          | 5                      | —    | 5    | —            |      | pF    |

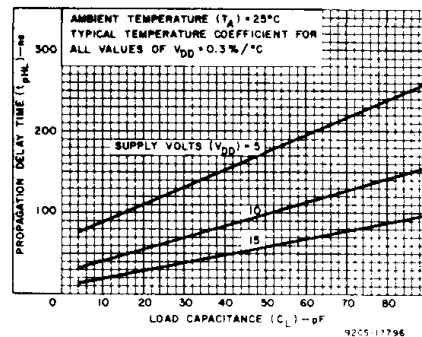


Fig. 13 — Typical high-to-low level propagation delay time vs.  $C_L$  — CD4012A.

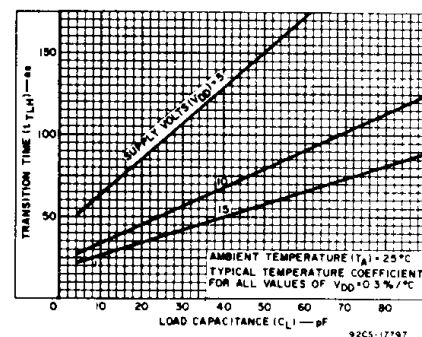


Fig. 14 — Typical low-to-high transition time vs.  $C_L$ .

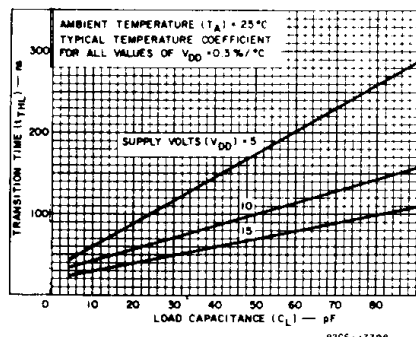


Fig. 15 — Typical high-to-low level transition time vs.  $C_L$  — CD4011A & CD4023A.

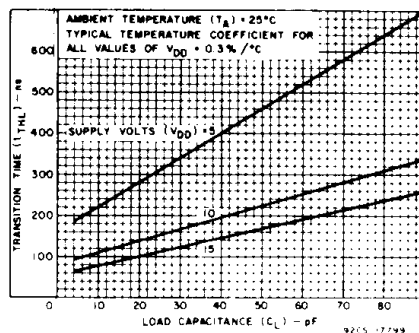


Fig. 16 — Typical high-to-low level transition time vs.  $C_L$  — CD4012A.

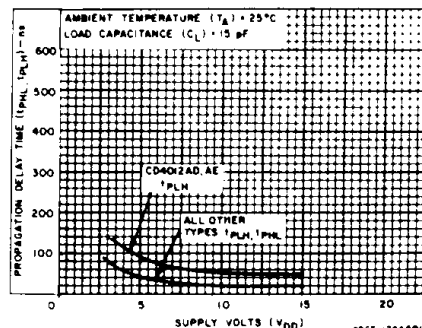


Fig. 17 — Minimum propagation delay time vs.  $V_{DD}$ .

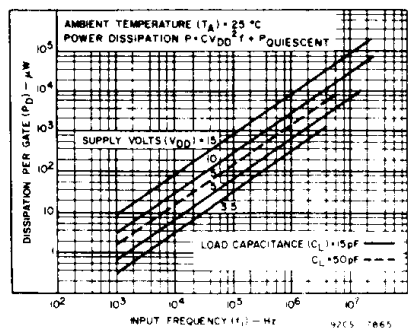


Fig. 18 — Typical dissipation characteristics.

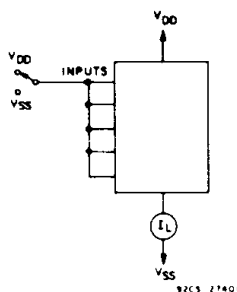


Fig. 19 — Quiescent device current test circuit.

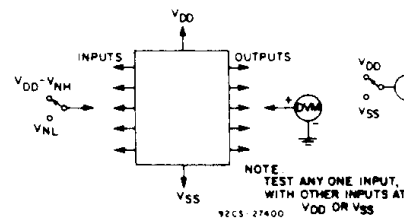


Fig. 20 — Noise immunity test circuit.

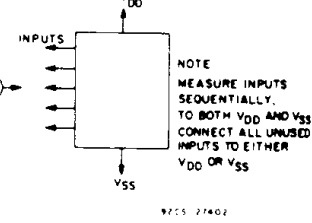


Fig. 21 — Input leakage current test circuit.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD4011AD3        | ACTIVE                | CDIP SB      | JD              | 14   | 1           | TBD                     | POST-PLATE       | N / A for Pkg Type           |
| CD4023AFB        | OBSOLETE              | CDIP         | J               | 14   |             | TBD                     | Call TI          | Call TI                      |
| JM38510/05001BCA | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| JM38510/05003BCA | OBSOLETE              | CDIP         | J               | 14   |             | TBD                     | Call TI          | Call TI                      |
| M/05003BCA       | OBSOLETE              | CDIP         | J               | 14   |             | TBD                     | Call TI          | Call TI                      |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

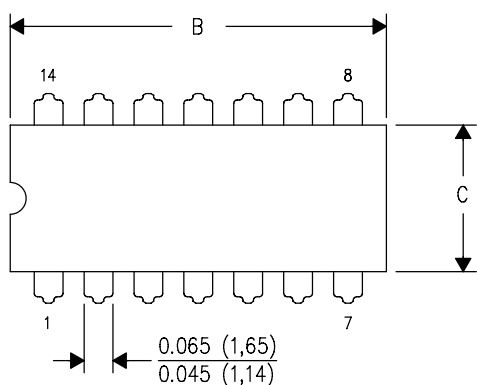
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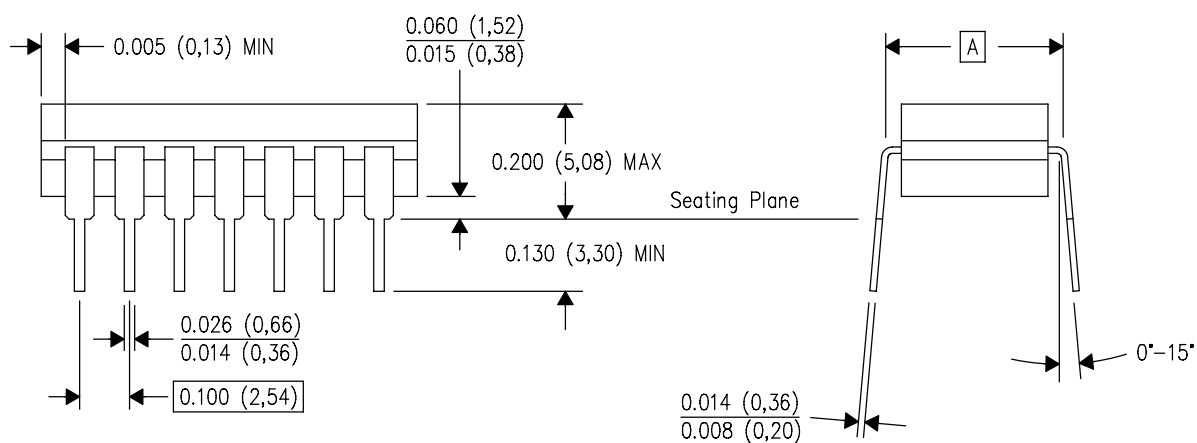
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |

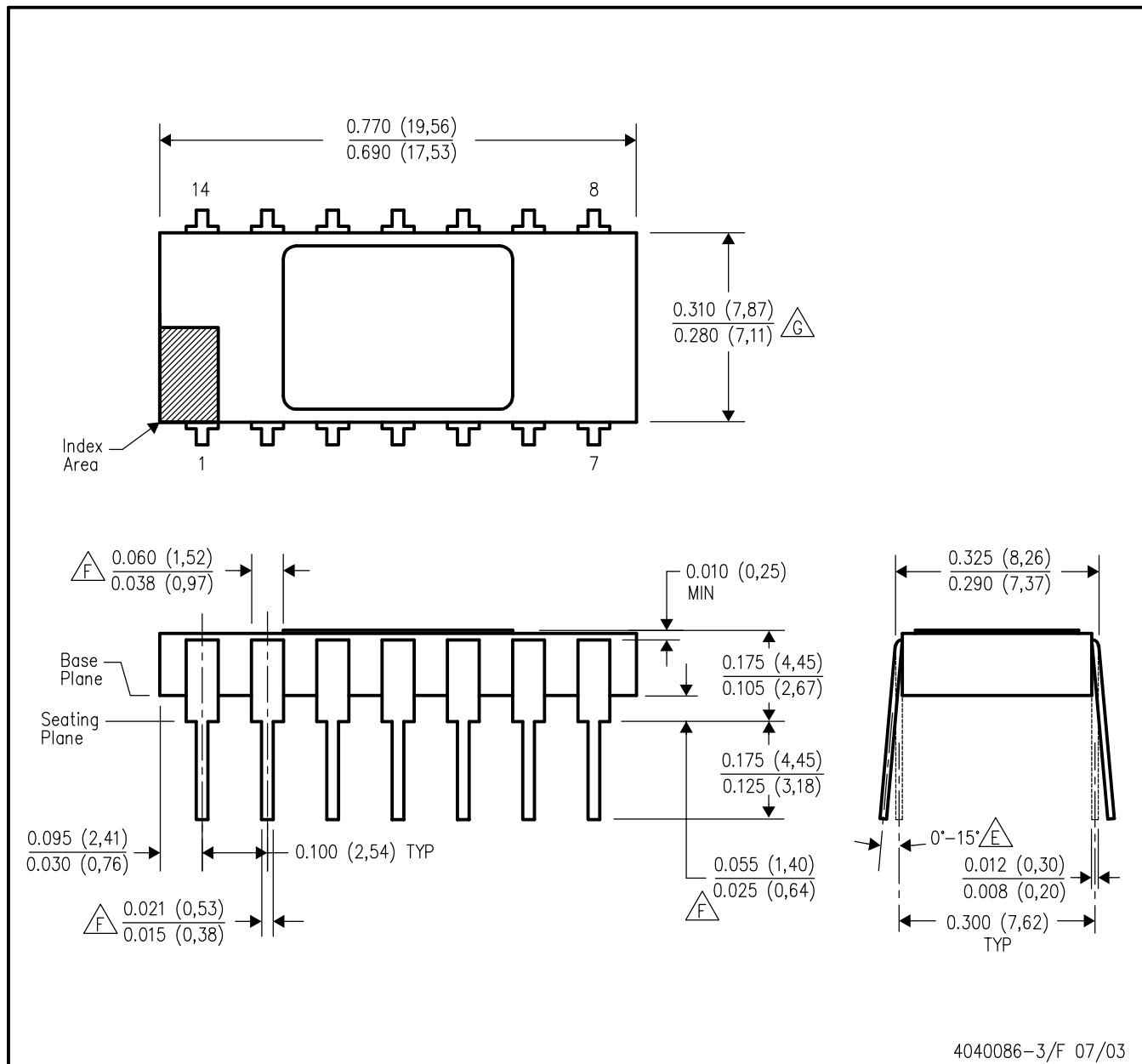


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

JD (R-CDIP-T14)

CERAMIC SIDE-BRAZE DUAL-IN-LINE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Controlling dimension: inch.
  - Leads within 0.005 (0,13) radius of true position (TP) at gage plane with maximum material condition and unit installed.
  - Angle applies to spread leads prior to installation.
  - Outlines on which the seating plane is coincident with the plane (standoff = 0), terminals lead standoffs are not required, and lead shoulder may equal lead width along any part of the lead above the seating/base plane.

- Body width does not include particles of packing materials.
- A visual index feature must be located within the cross-hatched area.

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| DLP® Products               | <a href="http://www.dlp.com">www.dlp.com</a>                       |
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| Microcontrollers            | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a> |
| RFID                        | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>               |
| RF/IF and ZigBee® Solutions | <a href="http://www.ti.com/lprf">www.ti.com/lprf</a>               |

### Applications

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