

DACxx68EVM

The DACxx68 Evaluation Module is an evaluation board containing all the necessary components to evaluate the eight-channel DAC7568, DAC8168, or DAC8568 series of high-performance digital-to-analog converters from Texas Instruments. The EVM is designed so that a single printed-circuit board (PCB) supports the entire family of high-speed, 12- to 16-bit serial DACs. The EVM is provided with Grade C devices which reset to zero and have a full-scale output range of 0 V to 5 V.

The modular EVM form factor allows for direct evaluation of the DAC's performance and operating characteristics. This EVM is compatible with the 5-6K Interface Board ([SLAU104](#)) from Texas Instruments as well as the HPA-MCU Interface Board ([SLAU106](#)).

Contents

1	EVM Overview	2
2	Analog Interface	2
3	Digital Interface	2
4	Power Supplies	3
	4.1 DAC Power	3
	4.2 Stand-Alone Operation	3
5	EVM Operation	3
	5.1 Analog Output	3
	5.2 Reference In/Out	4
	5.3 Digital Control	4
	5.4 SYNC	4
	5.5 LOAD DAC (LDAC)	4
	5.6 CLEAR (CLR)	5
	5.7 Default Jumper Locations	5
6	Bill of Material and EVM Schematic	6
	6.1 Bill of Materials	6
	6.2 EVM Schematic	7
7	Related Documentation from Texas Instruments	8

List of Figures

1	Top Layer Assembly Drawing and Jumper Locations.....	5
---	--	---

List of Tables

1	Digital Control	2
2	J3 Power Input	3
3	EVM Default Jumper Settings.....	5
4	Bill of Materials	6

1 EVM Overview

- Full-featured Evaluation Board for the 12-/14-/16-bit, eight-channel DAC7568, DAC8168, or DAC8568 digital-to-analog converters
- Onboard reference and buffer circuits
- High-speed serial interface
- Modular design for use with a variety of DSP and DACxx68 DAC Controller Interface Boards

2 Analog Interface

For maximum flexibility, the DACxx68EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row header/socket combination at J2. This header/socket provides access to the analog input pins of the ADC. Consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

Pin Number	Signal	Description
J2.2	DAC OUT_G	Voltage output for DAC channel G
J2.4	DAC OUT_E	Voltage output for DAC channel E
J2.6	DAC OUT_C	Voltage output for DAC channel C
J2.8	DAC OUT_A	Voltage output for DAC channel A
J2.10	DAC OUT_B	Voltage output for DAC channel B
J2.12	DAC OUT_D	Voltage output for DAC channel D
J2.14	DAC OUT_F	Voltage output for DAC channel F
J2.16	DAC OUT_H	Voltage output for DAC channel H
J2.18	REF(-)	Unused
J2.20	REF(+)	External reference source input (2.5 V NOM, 2.525 V maximum)
J2.15	VCOM	Common-mode voltage output option
J2.1–J2.19 (odd)	AGND	Analog ground connections (except J2.15)

3 Digital Interface

The DACxx68EVM is designed for easy interfacing to multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row header/socket combination at J2. This header/socket provides access to the digital control and serial data pins of the DACxx68 DAC EVM. Consult Samtec at www.samtec.com or 1-800-SAMTEC-9 for a variety of mating connector options.

Table 1. Digital Control

Pin Number	Signal	Description
J2.1	CNTL	Active-low input to SYNC enables data transfer – jumper configurable (see schematic) via JP5
J2.3	SCLK	Serial clock
J2.5	SCLK(R)	Serial clock return (for DSP host systems)
J2.7	FSX	Frame synchronization for DSP host systems – default SYNC input through JP5 (see schematic)
J2.9	FS(R)	Frame synchronization return (for DSP host systems)
J2.11	DX	Serial data input
J2.13	DR	Unused – Serial data return (for DSP host systems)
J2.15	INT	External source for LOAD DAC (LDAC) strobe via JP6
J2.17	TOUT	Default source for LOAD DAC (LDAC) strobe via JP6
J2.19	GPIO5	Optional source for active low CLEAR (CLR) input

Table 1. Digital Control (continued)

Pin Number	Signal	Description
J2.4	GND	System (EVM) ground
J2.10		
J2.18		

4 Power Supplies

The DACxx68EVM board is built with grade C devices and requires a single +5 V DC for proper operation. This 5-V supply powers the onboard voltage reference (U2) and the common-mode voltage output buffer (U3). When used in combination with one of the DAP Interface boards, J3 provides connection to the common power bus described in document [SLAA185](#). [Table 2](#) shows the pinout of J3.

Table 2. J3 Power Input

Signal	Pin Number		Signal
Unused	1	2	Unused
+5VA	3	4	Unused
GND	5	6	GND
Unused	7	8	Unused
Unused	9	10	Unused

When power is supplied to J3, JP4 allows for one of two different DC voltage sources to be applied to the DAC installed on the EVM. Review the schematic and PCB silkscreen for details.

4.1 DAC Power

JP4 allows the user to select the power supply used by the DAC installed in position U1 on the EVM. When JP4 is in the default factory position (Shunt on pins 1-2), power to the DAC comes from J3 pin 5, which is designated as a +5VDC input. When the shunt on JP4 is moved to pins 2-3, the user may apply an external power source to the DAC via TP1, referenced to TP4.

4.2 Stand-Alone Operation

When used as a stand-alone EVM, the analog power can be applied directly to TP5 referenced to pin TP4. Optimal performance of the EVM requires a clean, well-regulated power source.

CAUTION

The DACs that are compatible with this EVM have a variety of power supply requirements. Check the appropriate data sheets and verify that all power supplies are within the safe operating limits of the converter before applying power to the EVM.

5 EVM Operation

5.1 Analog Output

The analog output from the EVM is applied directly to J2 (top or bottom side) pins 2-16 (even). The DACxx68EVM does not provide any additional filtering or buffering of the output voltage, so that the user may evaluate the converter's low-glitch output performance.

5.2 Reference In/Out

The DAC8568, DAC8168, and DAC7568 provide the ability to use an internal reference or an external reference in the range of 0 V to 2.5 V. The DACxx58 internal reference is powered OFF by default. The following sections describe how to apply an external reference or use the internal reference.

5.2.1 External Reference

provides an external reference via JP3 (shorted pins 1-2 by default) from U2, a precision REF5025 source of 2.5 VDC. When JP3 is shorted on pins 2-3, an external reference may be applied to J2 pin 20 or TP3 reference to TP2.

These external reference sources are applied to pin 8 of the DAC installed on the EVM and are also fed to U3, a unity gain buffer configured OPA379. The output of U3 may be used to provide a 2.5-V, common-mode input to external signal-conditioning circuits via J2 pin 15.

5.2.2 Internal Reference

The internal reference can be powered up and powered down by using a serial command that requires a 32-bit write sequence as defined in the device data sheet (see the *Serial Interface section and Table 1* of document [SBAS430](#)).

CAUTION

Before enabling the internal reference of the DAC installed on the evaluation board, ensure that any shunt jumper applied to JP3 is completely removed.

The internal reference is enabled by setting the feature bits of the DAC control register. The DAC7568/8168/8568 data sheet provides specific details on both the static and flexible operating modes of the internal reference. For more information on using the internal reference source, review the *Internal Reference section* of document [SBAS430](#).

The internal reference source is applied to U3, a unity gain buffer configured OPA379. The output of U3 may be used to provide a 2.5-V, common-mode input to external signal conditioning circuits via J2 pin 15.

5.3 Digital Control

The digital control signals can be applied directly to J1 (top or bottom side). The DACxx68EVM also can be connected directly to a DSP or microcontroller capable of supplying the necessary serial control inputs. Visit the product folder for the EVM or the installed device for a current list of compatible interface and/or accessory boards.

5.4 SYNC

For synchronous DAC update operations, jumper JP5 is provided to allow the source selection of the signal applied to the SYNC input of the DAC installed on the EVM. The factory default condition for the EVM is to place a shunt jumper between pins 1-2 of JP5. This allows the Frame Sync (FS) signal from DSP host systems to be used as the SYNC input to the DAC. This signal originates from J1.7. When the shunt on JP5 is moved to pins 2-3, a GPIO input applied via J1.1 can be used to control the SYNC input to the DAC. JP2 may also be used to hold the LDAC input to the DAC low, allowing synchronous DAC output updates.

5.5 LOAD DAC (LDAC)

For asynchronous updates to the DAC outputs, jumper JP6 is provided to allow the source selection of the signal applied to the LDAC input of the DAC installed on the EVM. The factory default condition for the EVM is to place a shunt jumper between pins 1-2 of JP6. This allows the Timer Output (TOUT) signal from DSP host systems to be used as the LDAC input to the DAC. This signal originates from J1.17.

When the shunt on JP6 is moved to pins 2-3, a user-provided GPIO input may be applied to the LDAC pin via J1.15. This external input acts as an interrupt input to a DSP host processor which can in turn trigger a serial transfer to the DAC. JP2 can be used to hold the LDAC input to the DAC at ground potential if synchronous updates are required.

5.6 CLEAR (CLR)

Jumper JP1 is provided to allow the manual application of a CLR input pulse. The DACxx68EVM user may also apply a CLR input via J1 pin 19. Bringing the CLR pin low clears the content of all DAC registers and all DAC buffers, and replaces the code with the code determined by the clear code register. Jumper JP1 is open by default and uses a 10-k Ω pullup resistor (R1) to maintain logic high on the CLR input pin.

5.7 Default Jumper Locations

Table 3 provides a list of jumpers found on the EVM and their factory default conditions.

Table 3. EVM Default Jumper Settings

Jumper	Shunt Position	Jumper Description
JP1	N/A	Allows CLR to be monitored or controlled via external pulse source. Used with signals applied to J1.19
JP2	OPEN	Allows LDAC to be kept at GND potential when installed; it is recommended to remove any shunt jumper installed on JP6 if JP1 is installed.
JP3	Pins 1-2	Controls reference voltage applied to the installed DAC. When JP3 is moved to pins 2-3, and external reference may be applied to the EVM via J2.20 or to TP3 referenced to TP2
JP4	Pins 1-2	Analog power source control. Default is from J3.3. When shunt is placed on pins 2-3, power to the DAC may be applied to TP1 referenced to TP4.
JP5	Pins 1-2	Controls SYNC source selection – see Section 5.3 for details
JP6	Pins 1-2	Controls LDAC source selection – see Section 5.4 for details

The following diagram provides an overview of the DACxx68 assembly and locations of the various jumpers and connectors.

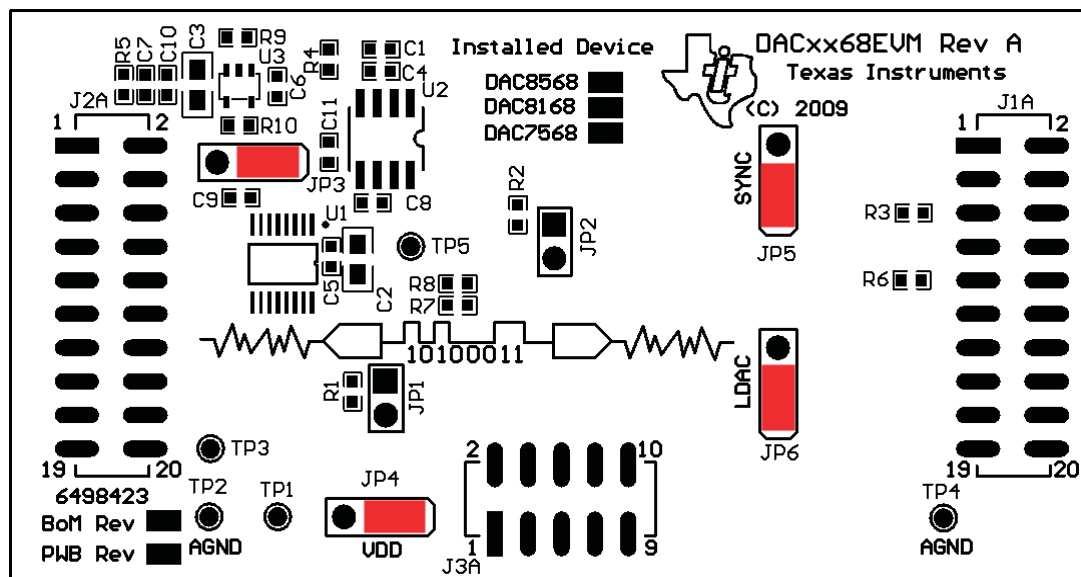


Figure 1. Top Layer Assembly Drawing and Jumper Locations

6 Bill of Material and EVM Schematic

Table 4 contains a complete bill of materials for the DACxx68EVM. The schematic diagram also is provided for reference.

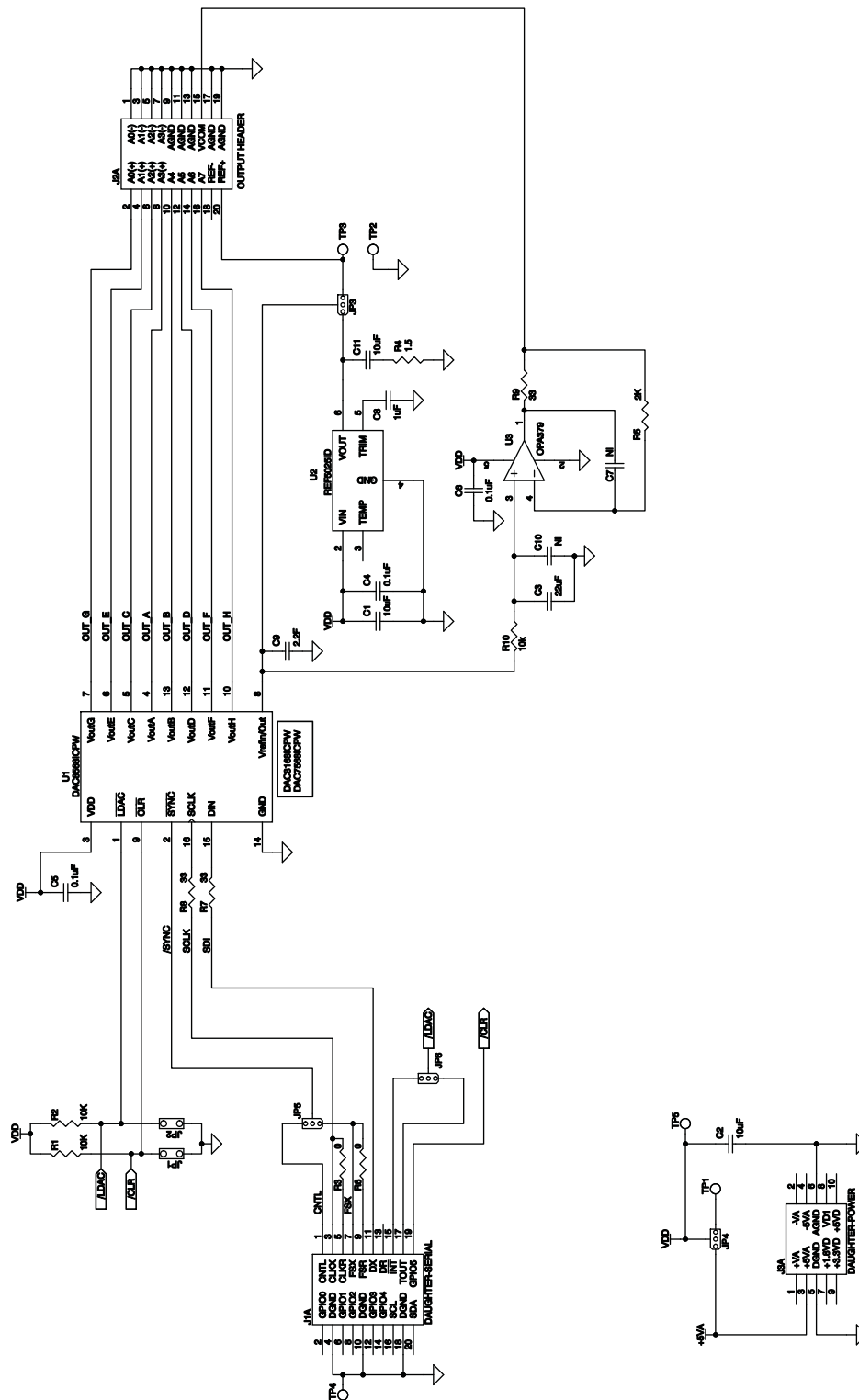
6.1 Bill of Materials

Table 4. Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
C1, C11	CAP CER 10UF 6.3V X5R 20% 0603	TDK	C1608X5R0J106M
C2	CAP CER 10UF 16V X5R 0805	Taiyo Yuden	EMK212BJ106KG-T
C3	CAP CER 22UF 10V X5R 0805	Taiyo Yuden	LMK212BJ226MG-T
C4, C5, C6	CAP CER .10UF 50V X7R 10% 0603	TDK	C1608X7R1H104K
C7, C10	NI		
C8	CAP CER 1.0UF 16V X7R 10% 0603	TDK	C1608X7R1C105K
C9	CAP CER 2.2UF 10V X5R 0603	TDK	C1608X5R1A225K
J1A, J2A (Top Side)	10 Pin, Dual Row, SM Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
J1B, J2B (Bottom Side)	10 Pin, Dual Row, SM Header (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
J3A (Top Side)	5 Pin, Dual Row, SM Header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
J3B (Bottom Side)	5 Pin, Dual Row, SM Header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
JP1, JP2	Header Strip (2 x 1)	Samtec	TSW-102-07-L-S
JP3 - JP6	Header Strip (3 x 1)	Samtec	TSW-103-07-L-S
R1, R2, R10	RES 10.0K OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-0710KL
R3, R6	RES 0 OHM, 1/16W 5% 0603 Chip Resistor	Yageo	RC0603JR-070RL
R4	RES 1.5 OHM 1/10W 5% 0603 SMD	Yageo	RC0603JR-071R5L
R5	RES 2.00K OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-072KL
R7, R8, R9	RES 33.0 OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-0733RL
TP1, TP3, TP5	TEST POINT PC MINI 0.040"D RED	Keystone	5000
TP2, TP4	TEST POINT PC MINI 0.040"D BLACK	Keystone	5001
U1 ⁽¹⁾	Device Under Test	TI	DAC8568/8168/7568ICPW
U2	IC PREC V-REF 2.5V LN 8-SOIC	TI	REF5025AID
U3	IC OPAMP GP R-R 90KHZ SOT23-5	TI	OPA379AIDBVT

⁽¹⁾ The device installed at location U1 is dependent on the EVM ordered. This device is soldered to the board for best performance. U1 may be replaced with any device listed in the EVM Compatible Device Data Sheets table found at the beginning of this document.

6.2 EVM Schematic



7 Related Documentation from Texas Instruments

The following devices data sheet is DACxx68EVM compatible.

- *DAC7568, DAC8168, DAC8568, 12-/14-/16-Bit, Octal-Channel, Ultra-Low Glitch, Voltage Output Digital-to-Analog Converters With 2.5V, 2ppm/°C Internal Reference* data sheet ([SBAS430](#))

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. **THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.**

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0 V to 5 V and the output voltage range of 0 V to 5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30° C. The EVM is designed to operate properly with certain components above 30° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated