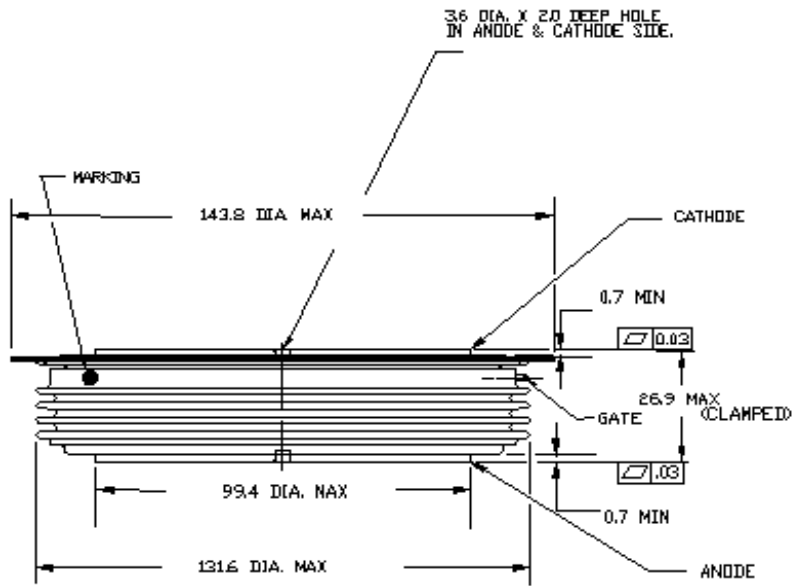




The TDS4 is a medium voltage, high current, thin pack disc SCR employing an amplifying gate structure. This thin package provides greater cooling thus maximizing high current performance. The amplifying gate design allows the SCR to be reliably operated at high di/dt and dv/dt conditions in various phase control applications.

FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I^2t Ratings

APPLICATIONS:

- DC Power Supplies
- Motor Controls
- Plating Rectifiers

ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.
 EXAMPLE: TDS4304002DH is a 3000V 4000A SCR with 300ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating $V_{DRM}-V_{RRM}$	Voltage Code	Current Rating I_{TAVG}	Current Code	Turn-Off T_q	Gate I_{GT}	Leads
TDS4	3000	30	4000	40	0	2	
	2800	28					
	2600	26			600us	300ma	12"
	2400	24			(typ.)	(max)	

Revised: 10/16/2013

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	3000	Volts
Average On-State Current, $T_C=70^{\circ}C$	$I_{T(Avg.)}$	4000	A
RMS On-State Current, $T_C=70^{\circ}C$	$I_{T(RMS)}$	6283	A
Average On-State Current, $T_C=55^{\circ}C$	$I_{T(Avg.)}$	4700	A
RMS On-State Current, $T_C=55^{\circ}C$	$I_{T(RMS)}$	7383	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	I_{TSM}	80,000	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	I_{TSM}	75,424	A
Fuse Coordination I^2t , 60Hz	I^2t	2.67E+07	A ² s
Fuse Coordination I^2t , 50Hz	I^2t	2.84E+07	A ² s
Critical Rate-of-Rise of On-State Current	di/dt	100	A/us
Repetitive			
Critical Rate-of-Rise of On-State Current	di/dt	300	A/us
Non-Repetitive			
Peak Gate Power, 100us	P_{GM}	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	T_J	-40 to+125	$^{\circ}C$
Storage Temperature	$T_{Stg.}$	-50 to+150	$^{\circ}C$
Approximate Weight		6.5	lb
		2.95	Kg
Mounting Force		16,000-20,000	lbs
		71.2 - 89.0	KNewtons

Information presented is based upon limited testing or projected capabilities.
This information is subject to change without notice. The manufacturer makes
no claim as to suitability for use, reliability, capability or future availability of this
product.

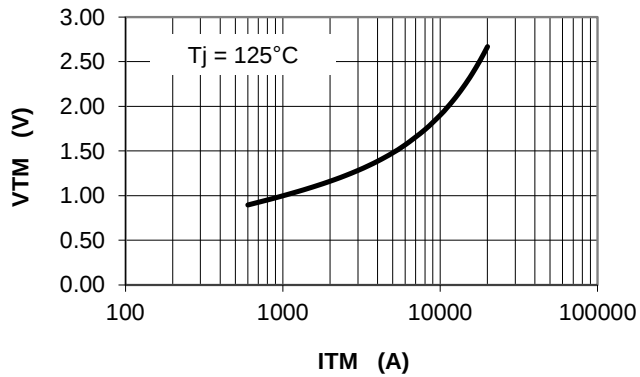
Electrical Characteristics, Tj=25°C unless otherwise specified

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Forward Leakage Current	I_{DRM}	Tj=125°C, V_{DRM} =Rated			250	ma
Repetitive Peak Reverse Leakage Current	I_{RRM}	Tj=125°C, V_{RRM} =Rated			250	ma
Peak On-State Voltage	V_{TM}	Tj=125°C, I_{TM} =4000A			1.38	V
V_{TM} Model, Low Level	V_0	Tj=125°C			0.942	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	15% $I_{TM} - I_{TSM}$			9.79E-02	mΩ
V_{TM} Model, High Level	V_0	Tj=125°C			1.175	V
$V_{TM} = V_0 + r \cdot I_{TM}$	r	$\pi \cdot I_{TM} - I_{TSM}$			7.45E-02	mΩ
V_{TM} Model, 4-Term	A	Tj=125°C			-0.257	
$V_{TM} = A + B \cdot \ln(I_{TM}) +$	B	15% $I_{TM} - I_{TSM}$			0.185	
$C \cdot (I_{TM}) + D \cdot (I_{TM})^{1/2}$	C				7.73E-05	
	D				-3.20E-03	
Turn-On Delay Time	t_d	$V_D = 0.5 \cdot V_{DRM}$ Gate Drive: 40V - 20Ω		3		us
Turn-Off Time	t_q	Tj=125°C $dv/dt = 20V/us$ to 67% V_{DRM}			600	us
$dv/dt_{(Crit)}$	dv/dt	Tj=125°C Exp. Waveform $V_D = 67\%$ Rated	800			V/us
Gate Trigger Current	I_{GT}	Tj=25°C $V_D = 12V$	30	150	300	ma
Gate Trigger Voltage	V_{GT}		0.8	2.0	5.0	V
Peak Reverse Gate Voltage	V_{GRM}				5	V
Reverse Recovery Current	$I_R(Rec)$	Tj=125°C $V_R = 100V$			300	A
Reverse Recovery Charge	QRA				10,500	μCoul

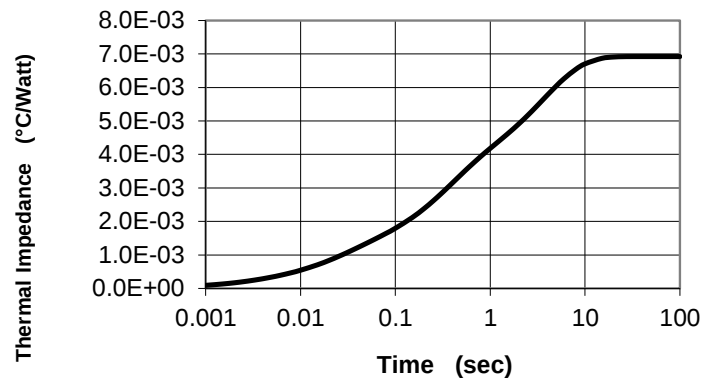
Thermal Characteristics

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Thermal Resistance						
Junction to Case	$R\theta_{jc}$	Double side cooled		0.0065	0.0070	°C/Watt
Case to Sink	$R\theta_{cs}$	Double side cooled		0.001	0.0015	°C/Watt
Thermal Impedance Model	$Z\theta_{jc}$	Double side cooled				
$Z\theta_{jc}(t) = \Sigma(A(N) \cdot (1 - \exp(-t/\text{Tau}(N))))$						
where: N = 1 2 3 4						
$A(N) = 1.43E-04 \quad 9.08E-04 \quad 2.37E-03 \quad 3.50E-03$						
$\text{Tau}(N) = 2.62E-03 \quad 2.31E-02 \quad 3.05E-01 \quad 3.60E+00$						

Maximum On-State Voltage Drop

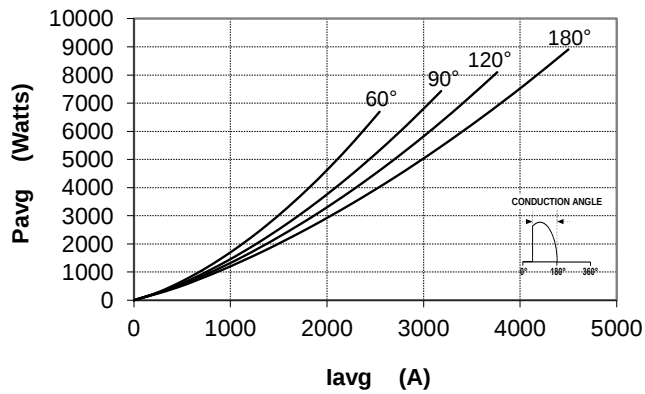


MAXIMUM TRANSIENT THERMAL IMPEDANCE



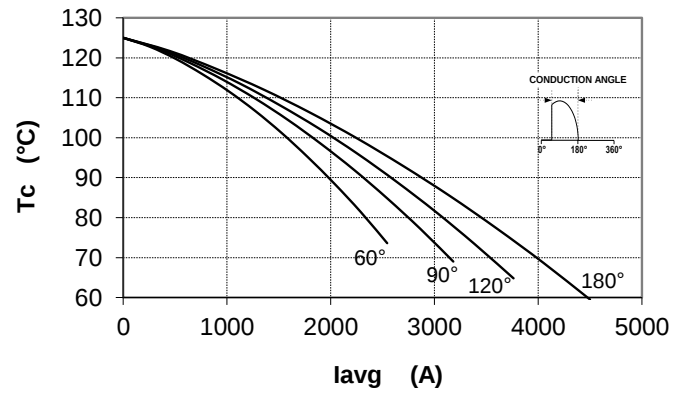
Maximum On-State Power Dissipation

Sinusoidal Waveform



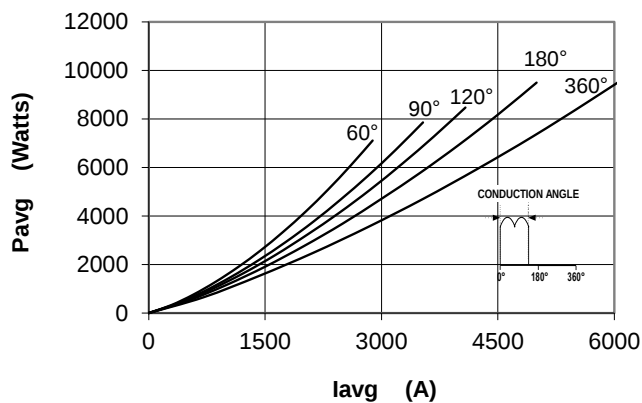
Maximum Allowable Case Temperature

Sinusoidal Waveform



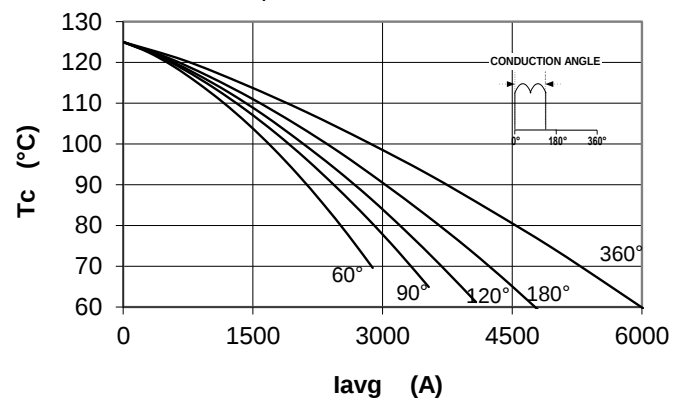
Maximum On-State Power Dissipation

Square Waveform

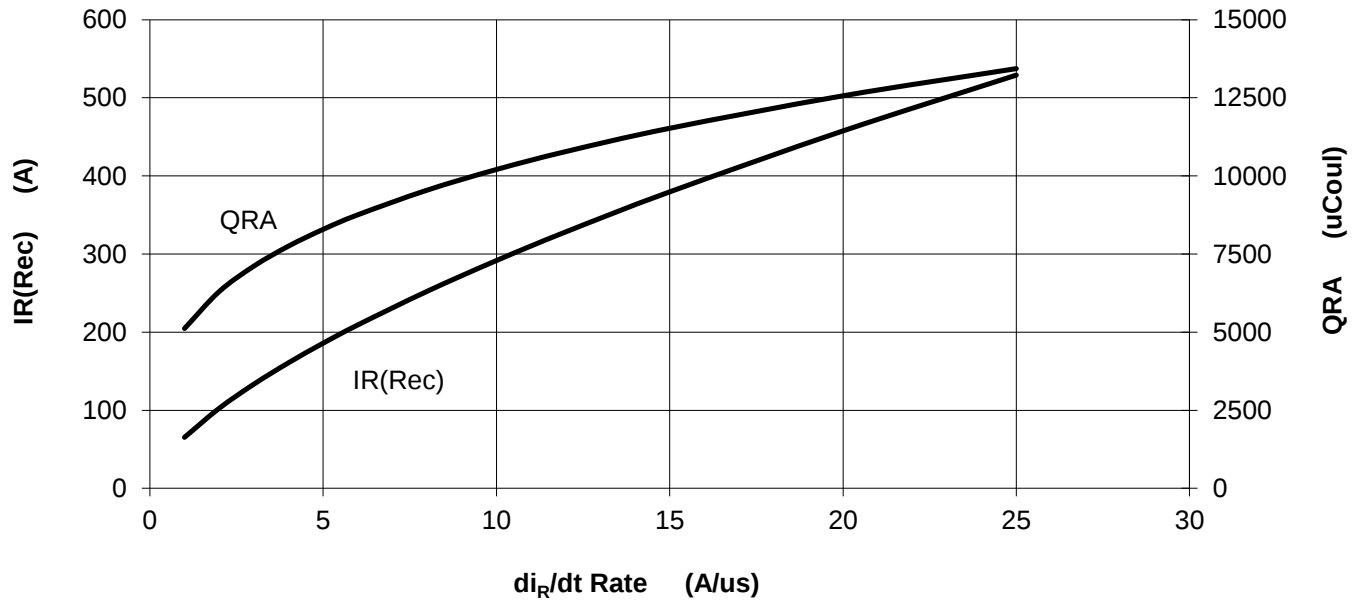


Maximum Allowable Case Temperature

Square Waveform



TDS4304002



MULTI-CYCLE SURGE

TDS434002

VR = 0

