

## Low-power, High-performance $\Delta\Sigma$ Test DAC

### Features

- Digital  $\Delta\Sigma$  Input from CS5376A Digital Filter
- Selectable Differential Analog Outputs
  - Precision output ( $OUT_{\pm}$ ) for electronics tests
  - Buffered output ( $BUF_{\pm}$ ) for sensor tests
- Multiple AC and DC Operational Modes
  - Signal bandwidth: DC to 100 Hz
  - Max AC amplitude: 5  $V_{PP}$  differential
  - Max DC amplitude: + 2.5  $V_{dc}$  differential
- Selectable Attenuation for CS3301A / CS3302A
  - 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64
- Outstanding Performance
  - AC (OUT): -116 dB THD typical, -112 dB max
  - AC (BUF): -108 dB THD typical, -90 dB max
  - DC absolute accuracy: 0.4% typical, 1% max
- Low Power Consumption
  - AC modes / DC modes: 40 mW / 20 mW
  - Sleep mode / Power Down: 1 mW / 10  $\mu$ W
- Extremely Small Footprint
  - 28-pin SSOP package, 8 mm x 10 mm
- Bipolar Power Supply Configuration
  - $VA+ = +2.5$  V;  $VA- = -2.5$  V;  $VD = +3.3$  V

### Description

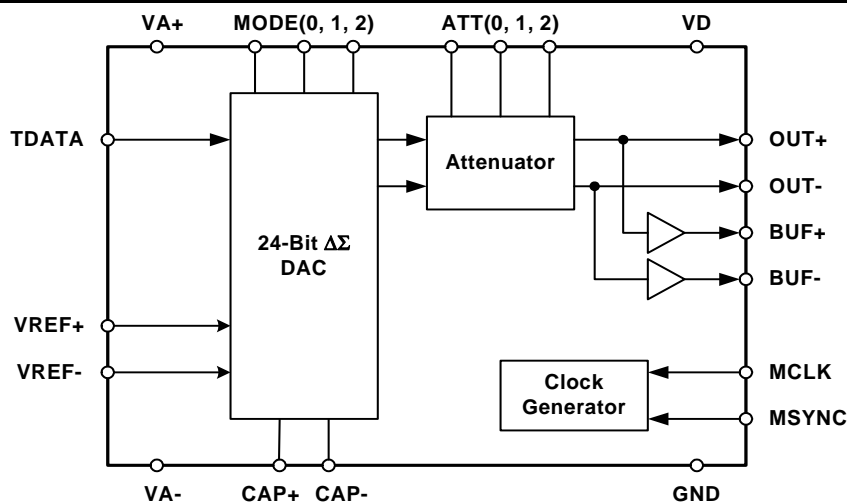
The CS4373A is a high-performance, differential output digital-to-analog converter (DAC) with programmable attenuation and multiple operational modes. AC test modes measure system dynamic performance through THD and CMRR tests while DC test modes are for gain calibration and pulse tests.

The CS4373A is driven by a  $\Delta\Sigma$  digital bit stream from the CS5376A digital filter test bit stream (TBS) generator. It has two sets of differential analog outputs,  $OUT$  and  $BUF$ , to simplify system design as dedicated outputs for testing the electronics channel and for in-circuit sensor tests. Analog output attenuation is selected by simple pin settings and matches the gain of the CS3301A / CS3302A differential amplifiers for full-scale testing at all gain ranges.

The CS4373A test DAC provides self-test and precision calibration capability for high-resolution, low-frequency multi-channel measurement systems designed from CS3301A / CS3302A differential amplifiers, CS5371A / CS5372A  $\Delta\Sigma$  modulators and the CS5376A digital filter.

### ORDERING INFORMATION

See [page 34](#).



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## 1. CHARACTERISTICS AND SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over the [Specified Operating Conditions](#).
- Typical performance characteristics and specifications are measured at nominal supply voltages and  $T_A = 25^\circ\text{C}$ .
- GND = 0 V. Single-ended voltages with respect to GND, differential voltages with respect to opposite half.
- Device is connected as shown in [Figure 6 on page 17](#), unless otherwise noted.

## SPECIFIED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
<b>Bipolar Power Supplies</b>					
Positive Analog $\pm 2\%$	VA+	2.45	2.50	2.55	V
Negative Analog (Note 1) $\pm 2\%$	VA-	-2.45	-2.50	-2.55	V
Positive Digital $\pm 3\%$	VD	3.20	3.30	3.40	V
<b>Voltage Reference Input</b>					
{VREF+} - {VREF-} (Note 2, 3)	VREF	-	2.500	-	V
VREF- (Note 4)	VREF-	-	VA -	-	V
<b>Thermal</b>					
Ambient Operating Temperature Industrial (-IS, -ISZ)	$T_A$	-40	25	85	$^\circ\text{C}$

- Notes:
1. VA- must always be the most-negative input voltage to avoid potential SCR latch-up conditions.
  2. By design, a 2.500 V voltage reference input results in the best signal-to-noise performance.
  3. Full-scale accuracy is directly proportional to the voltage reference absolute accuracy.
  4. VREF inputs must satisfy:  $VA- \leq VREF- < VREF+ \leq VA+$ .

Modes of Operation		
Selection	MODE[2:0]	Mode Description
0	0 0 0	Sleep mode.
1	0 0 1	AC OUT and BUF outputs.
2	0 1 0	AC OUT only, BUF high-z.
3	0 1 1	AC BUF only, OUT high-z.
4	1 0 0	DC common mode output.
5	1 0 1	DC differential output.
6	1 1 0	AC common mode output.
7	1 1 1	Sleep mode.

Attenuation			
Selection	ATT[2:0]	Attenuation	dB
0	0 0 0	1/1	0 dB
1	0 0 1	1/2	-6.02 dB
2	0 1 0	1/4	-12.04 dB
3	0 1 1	1/8	-18.06 dB
4	1 0 0	1/16	-24.08 dB
5	1 0 1	1/32	-30.10 dB
6	1 1 0	1/64	-36.12 dB
7	1 1 1	reserved	reserved

**Table 1. Selections for Operational Mode and Attenuation**

## TEMPERATURE CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature	$T_A$	-40	-	+85	°C
Storage Temperature Range	$T_{STG}$	-65	-	150	°C
Allowable Junction Temperature	$T_{JCT}$	-	-	125	°C
Junction to Ambient Thermal Impedance (4-layer PCB)	$\Theta_{JA}$	-	65	-	°C / W

## ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Parameter
DC Power Supplies	Positive Analog	VA+	-0.5	6.8	V
	Negative Analog	VA-	-6.8	0.5	V
	Digital	VD	-0.5	6.8	V
Analog Supply Differential	(VA+) - (VA-)	VA <sub>DIFF</sub>	-	6.8	V
Digital Supply Differential	(VD) - (VA-)	VD <sub>DIFF</sub>	-	7.6	V
Input Current, Power Supplies	(Note 5)	I <sub>IN</sub>	-	±50	mA
Input Current, Any Pin Except Supplies	(Note 5)	I <sub>IN</sub>	-	±10	mA
Output Current	(Note 5)	I <sub>OUT</sub>	-	±25	mA
Power Dissipation		PDN	-	500	mW
Analog Input Voltages		V <sub>INA</sub>	(VA-) - 0.5	(VA+) + 0.5	V
Digital Input Voltages		V <sub>IND</sub>	-0.5	(VD) + 0.5	V

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

Notes: 5. Transient currents up to ±100 mA will not cause SCR latch-up.

## ANALOG CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
<b>VREF Input</b>					
{VREF+} - {VREF-} (Note 2, 3)	VREF	-	2.500	-	V
VREF- (Note 4)	VREF-	-	VA -	-	V
VREF Input Current, AC modes	VREF <sub>IAC</sub>	-	80	-	μA
VREF Input Current, DC modes	VREF <sub>IDC</sub>	-	40	-	μA
VREF Input Noise (Note 6)	VREF <sub>IN</sub>	-	-	1	μV <sub>rms</sub>
<b>Analog OUT± Output</b>					
Analog External Load at OUT± (Note 7, 8)	Load Resistance	R <sub>LOUT</sub>	50	-	MΩ
	Load Capacitance	C <sub>LOUT</sub>	-	-	pF
Differential Output Impedance	1/1	ZDIF <sub>OUT</sub>	-	1.4	kΩ
	1/2		-	10.1	kΩ
	1/4		-	7.9	kΩ
	1/8		-	5.1	kΩ
	1/16		-	3.3	kΩ
	1/32		-	2.3	kΩ
	1/64		-	1.7	kΩ
Single-ended Output Impedance	1/1	ZSE <sub>OUT</sub>	-	0.7	kΩ
	1/2		-	7.4	kΩ
	1/4		-	9.0	kΩ
	1/8		-	9.4	kΩ
	1/16		-	9.5	kΩ
	1/32		-	9.5	kΩ
	1/64		-	9.4	kΩ
High-Z Impedance (Note 8)	HZ <sub>OUT</sub>	-	3	-	MΩ
Crosstalk to BUF± High-Z Output (Note 8)	XT <sub>OUT</sub>	-	-120	-	dB
<b>Analog BUF± Output</b>					
Analog External Load at BUF± (Note 8)	Load Resistance	R <sub>LBUF</sub>	1	-	kΩ
	Load Capacitance	C <sub>LBUF</sub>	-	-	nF
Differential Output Impedance	1/1 - 1/64	ZDIF <sub>BUF</sub>	-	6	Ω
Single-ended Output Impedance (Note 9) (BUF-) 1/64 (Note 9) (BUF+) 1/64	1/1 - 1/32	ZSE <sub>BUF</sub>	-	3	Ω
			-	3	
			-	50	
High-Z Impedance (Note 8)	HZ <sub>BUF</sub>	-	4.5	-	MΩ
Crosstalk to OUT± High-Z Output (Note 8)	XT <sub>BUF</sub>	-	-120	-	dB

- Notes:
- Maximum integrated noise over the measurement bandwidth for the voltage reference device attached to the VREF± inputs.
  - Load on the precision OUT± outputs is normally from the CS3301A / CS3302A amplifiers, which have 1 GΩ/1 TΩ typical input impedance and 18 pF typical input capacitance.
  - Guaranteed by design and/or characterization.
  - Single-ended output impedance at 1/64 is different for BUF+ and BUF- due to the output attenuator architecture.

## AC DIFFERENTIAL MODES 1, 2, 3

Parameter	Symbol	Min	Typ	Max	Unit
<b>AC Differential Characteristics</b>					
Full-scale Differential AC Output	$V_{ACFS}$	-	5	-	V <sub>pp</sub>
		-	2.5	-	V <sub>pp</sub>
		-	1.25	-	V <sub>pp</sub>
		-	625	-	mV <sub>pp</sub>
		-	312.5	-	mV <sub>pp</sub>
		-	156.25	-	mV <sub>pp</sub>
		-	78.125	-	mV <sub>pp</sub>
Full-scale Bandwidth (Note 8)	$V_{ACBW}$	-	-	100	Hz
Impulse Amplitude (Note 8, 10)	$V_{ACIMP}$	-	-	-20	dBfs
<b>AC Differential Accuracy</b>					
Full-scale Accuracy (Note 3, 11)	$V_{ACABS}$	- 0.5	- 0.2	0.2	%FS
Relative Accuracy (Note 12)	$V_{ACREL}$	- 0.2	± 0.1	0.2	%
		-	± 0.1	-	%
		-	± 0.1	-	%
		-	- 0.1 ± 0.2	-	%
		-	- 0.2 ± 0.3	-	%
		-	- 0.5 ± 0.5	-	%
Full-scale Drift (Note 14)	$V_{ACTC}$	-	25	-	μV/°C
<b>DC Common Mode Characteristics</b>					
Common Mode (Note 13)	$V_{ACCM}$	-	(V <sub>A-</sub> ) + 2.35	-	V
Common Mode Drift (Note 13, 14)	$V_{ACCMTC}$	-	300	-	μV/°C

Notes: 10. Maximum amplitude for operation above 100 Hz. A reduced amplitude for higher frequencies is required to guarantee stability of the low-power delta-sigma architecture.

11. Full-scale accuracy compares the defined full-scale 1/1 amplitude to the measured 1/1 amplitude. Specification is for unloaded outputs. Applying a differential load lowers the output amplitude ratiometric to the differential output impedance.
12. Relative accuracy compares the measured 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 amplitude to the measured 1/1 amplitude.
13. Common mode voltage is defined as [(SIG+) + (SIG-)] / 2.
14. Specification is for the parameter over the specified temperature range and is for the device only. It does not include the effects of external components.

## AC DIFFERENTIAL MODES 1, 2, 3 (CONT.)

Parameter			Symbol	Min	Typ	Max	Unit
<b>Signal to Noise</b>							
Signal to Noise (OUT± Unloaded) (Note 15)	1/1 -> 1x	SNR <sub>OUT</sub>	-	114	-	dB	
	1/2 -> 2x		-	114	-	dB	
	1/4 -> 4x		-	114	-	dB	
	1/8 -> 8x		-	113	-	dB	
	1/16 -> 16x		-	111	-	dB	
	1/32 -> 32x		-	108	-	dB	
	1/64 -> 64x		-	103	-	dB	
Signal to Noise (BUF± Unloaded, 1 kΩ Load) (Note 15, 16)	1/1 -> 1x	SNR <sub>BUF</sub>	-	110	-	dB	
	1/2 -> 2x		-	106	-	dB	
	1/4 -> 4x		-	101	-	dB	
	1/8 -> 8x		-	95	-	dB	
	1/16 -> 16x		-	89	-	dB	
	1/32 -> 32x		-	83	-	dB	
	1/64 -> 64x		-	77	-	dB	
<b>Total Harmonic Distortion</b>							
Total Harmonic Distortion (OUT± Unloaded) (Note 17, 18)	1/1 -> 1x	THD <sub>OUT</sub>	-	- 116	- 112	dB	
	1/2 -> 2x		-	- 115	-	dB	
	1/4 -> 4x		-	- 114	-	dB	
	1/8 -> 8x		-	- 112	-	dB	
	1/16 -> 16x		-	- 111	-	dB	
	1/32 -> 32x		-	- 110	-	dB	
	1/64 -> 64x		-	- 106	-	dB	
Total Harmonic Distortion (BUF± Unloaded) (Note 16, 17, 18)	1/1 -> 1x	THD <sub>BUF</sub>	-	- 108	- 90	dB	
	1/2 -> 2x		-	- 105	-	dB	
	1/4 -> 4x		-	- 100	-	dB	
	1/8 -> 8x		-	- 94	-	dB	
	1/16 -> 16x		-	- 88	-	dB	
	1/32 -> 32x		-	- 82	-	dB	
	1/64 -> 64x		-	- 76	-	dB	
Total Harmonic Distortion (BUF± 1 kΩ Load) (Note 16, 17, 18)	1/1 -> 1x	THD <sub>BUFL</sub>	-	- 102	- 80	dB	
	1/2 -> 2x		-	- 101	-	dB	
	1/4 -> 4x		-	- 97	-	dB	
	1/8 -> 8x		-	- 92	-	dB	
	1/16 -> 16x		-	- 87	-	dB	
	1/32 -> 32x		-	- 82	-	dB	
	1/64 -> 64x		-	- 76	-	dB	

- Notes: 15. Specification measured using CS3301A amplifier at corresponding gain with the CS5371A / CS5372A modulator measuring a 430 Hz bandwidth. Amplified noise dominates for x16, x32, x64 amplifier gains.
16. Buffered outputs (BUF±) include 1/f noise not present on the precision outputs (OUT±).
17. Tested with a 31.25 Hz sine wave at -1 dB amplitude.
18. Specification measured using CS3301A amplifier at corresponding gain using the CS5371A / CS5372A modulator measuring a 430 Hz bandwidth. Amplified noise in the harmonic bins dominates THD measurements for x16, x32, x64 amplifier gains.



## DC COMMON MODE 4

Parameter		Symbol	Min	Typ	Max	Unit
DC Common Mode Characteristics						
Common Mode Output		VDC <sub>CM</sub>	-	(VA-)+2.35	-	V
Common Mode Drift	(Note 14)	VDC <sub>CMTC</sub>	-	300	-	μV/°C
DC Common Mode Accuracy						
Common Mode Match	1/1	VDC <sub>CMM</sub>	- 5	± 1	5	mV
Noise						
Noise (OUT± Unloaded) (Note 15)	1/1 -> 1x	N <sub>OUT</sub>	-	6	-	μV <sub>rms</sub>
	1/2 -> 2x		-	7	-	μV <sub>rms</sub>
	1/4 -> 4x		-	7	-	μV <sub>rms</sub>
	1/8 -> 8x		-	7	-	μV <sub>rms</sub>
	1/16 -> 16x		-	7	-	μV <sub>rms</sub>
	1/32 -> 32x		-	9	-	μV <sub>rms</sub>
	1/64 -> 64x		-	14	-	μV <sub>rms</sub>
Noise (BUF± Unloaded, 1 kΩ Load) (Note 15, 16)	1/1 -> 1x	N <sub>BUF</sub>	-	7	-	μV <sub>rms</sub>
	1/2 -> 2x		-	10	-	μV <sub>rms</sub>
	1/4 -> 4x		-	17	-	μV <sub>rms</sub>
	1/8 -> 8x		-	33	-	μV <sub>rms</sub>
	1/16 -> 16x		-	64	-	μV <sub>rms</sub>
	1/32 -> 32x		-	130	-	μV <sub>rms</sub>
	1/64 -> 64x		-	257	-	μV <sub>rms</sub>

## DC DIFFERENTIAL MODE 5

Parameter		Symbol	Min	Typ	Max	Unit
DC Differential Mode Characteristics						
Full-scale Differential DC Output (Note 19)	1/1	VDC <sub>FS</sub>	-	2.5	-	V
	1/2		-	1.25	-	V
	1/4		-	625	-	mV
	1/8		-	312.5	-	mV
	1/16		-	156.25	-	mV
	1/32		-	78.125	-	mV
	1/64		-	39.0625	-	mV
DC Differential Accuracy						
Full-scale Accuracy (Note 3, 11)	1/1	VDC <sub>ABS</sub>	- 1.0	- 0.4	0.2	%FS
Relative Accuracy (Note 12)	1/2	VDC <sub>REL</sub>	- 0.2	± 0.1	0.2	%
	1/4		-	± 0.1	-	%
	1/8		-	-0.1 ± 0.4	-	%
	1/16		-	-0.2 ± 0.9	-	%
	1/32		-	-0.5 ± 1.7	-	%
	1/64		-	-1.0 ± 3.6	-	%
	Full-scale Drift (Note 14)			VDC <sub>TC</sub>	-	25
DC Common Mode Characteristics						
Common Mode (Note 13)		VDC <sub>CM</sub>	-	(VA-)+2.35	-	V
Common Mode Drift (Note 13, 14)		VDC <sub>CMTC</sub>	-	300	-	μV/°C
Noise						
Noise (OUT± Unloaded) (Note 15, 19)	1/1 -> 1x	N <sub>OUT</sub>	-	9	-	μV <sub>rms</sub>
	1/2 -> 2x		-	9	-	μV <sub>rms</sub>
	1/4 -> 4x		-	9	-	μV <sub>rms</sub>
	1/8 -> 8x		-	9	-	μV <sub>rms</sub>
	1/16 -> 16x		-	10	-	μV <sub>rms</sub>
	1/32 -> 32x		-	11	-	μV <sub>rms</sub>
	1/64 -> 64x		-	15	-	μV <sub>rms</sub>
Noise (BUF± Unloaded, 1 kΩ Load) (Note 15, 16, 19)	1/1 -> 1x	N <sub>BUF</sub>	-	10	-	μV <sub>rms</sub>
	1/2 -> 2x		-	12	-	μV <sub>rms</sub>
	1/4 -> 4x		-	18	-	μV <sub>rms</sub>
	1/8 -> 8x		-	32	-	μV <sub>rms</sub>
	1/16 -> 16x		-	67	-	μV <sub>rms</sub>
	1/32 -> 32x		-	122	-	μV <sub>rms</sub>
	1/64 -> 64x		-	265	-	μV <sub>rms</sub>

Notes: 19. DC differential output is chopper stabilized and includes low-level 32 kHz out-of-band noise which is rejected by the digital filter during acquisition.

## AC COMMON MODE 6

Parameter		Symbol	Min	Typ	Max	Unit
<b>AC Common Mode Characteristics</b>						
Full-scale Common Mode AC Output (Note 20)	1/1	$V_{CM_{FS}}$	-	2.5	-	$V_{pp}$
	1/2		-	1.25	-	$V_{pp}$
	1/4		-	625	-	$mV_{pp}$
	1/8		-	312.5	-	$mV_{pp}$
	1/16		-	156.25	-	$mV_{pp}$
	1/32		-	78.125	-	$mV_{pp}$
Full-scale Bandwidth	(Note 8)	$V_{CM_{BW}}$	-	-	100	Hz
Impulse Amplitude	(Note 8, 10)	$V_{CM_{IMP}}$	-	-	-20	dBfs
<b>AC Common Mode Accuracy</b>						
Common Mode Match (OUT± Unloaded) (Note 17, 20)		$V_{CM_{CMM}}$	-	-115	-105	dB
Common Mode Match (BUF± Unloaded, 1 kΩ Load) (Note 16, 17, 20)		$V_{CM_{CMM}}$	-	-95	-85	dB
Full-scale Accuracy (Note 3, 11)	1/1	$V_{AC_{ABS}}$	-	-0.3	-	%FS
Relative Accuracy (Note 12, 20)	1/2	$V_{AC_{REL}}$	-	-0.1	-	%
	1/4		-	-0.5	-	%
	1/8		-	-1.0	-	%
	1/16		-	-2.0	-	%
	1/32		-	-5.0	-	%
Full-scale Drift	(Note 14)	$V_{CM_{TC}}$	-	25	-	$\mu V/^{\circ}C$
<b>DC Common Mode Characteristics</b>						
Common Mode Mean	(Note 21)	$V_{CM_{CM}}$	-	(VA-)+2.35	-	V
Common Mode Mean Drift	(Note 14, 21)	$V_{CM_{CMTTC}}$	-	300	-	$\mu V/^{\circ}C$

Notes: 20. No AC common mode signal is output at 1/64 attenuation due to the attenuator architecture.

21. Common mode mean is defined as  $[(SIG_{max}) + (SIG_{min})] / 2$ .

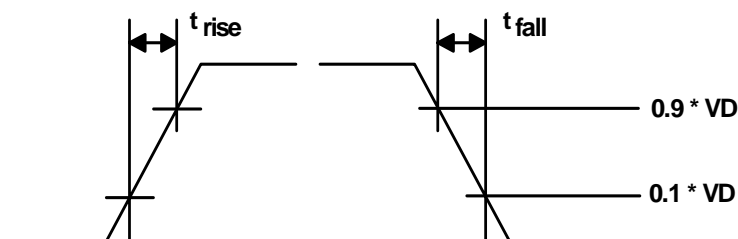
## DIGITAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
<b>Digital Inputs</b>					
High-level Input Drive Voltage (Note 22)	$V_{IH}$	$0.6 \cdot V_D$	-	$V_D$	V
Low-level Input Drive Voltage (Note 22)	$V_{IL}$	0.0	-	0.8	V
Input Leakage Current	$I_{IN}$	-	$\pm 1$	$\pm 10$	$\mu A$
Digital Input Capacitance (Note 8)	$C_{IN}$	-	9	-	pF
Rise Times Except MCLK (Note 8)	$t_{RISE}$	-	-	100	ns
Fall Times Except MCLK (Note 8)	$t_{FALL}$	-	-	100	ns
<b>TDATA Input</b>					
TDATA Input Bit Rate (Note 23)	$f_{tdata}$	-	256	-	kbits/s
TDATA Input One's Density Range (Note 8)	$INR_{OD}$	25	-	75	%
TBSGAIN Full-scale Code (Note 24)	$TBS_{FS}$	-	0x04B8F2	-	
TBSGAIN -20 dB Code (Note 24)	$TBS_{-20dB}$	-	0x0078E5	-	

Notes: 22. Device is intended to be driven with CMOS logic levels.

23. TDATA is generated by the test bit stream generator in the CS5376A digital filter.

24. TBSGAIN register value in the CS5376A digital filter.



**Figure 1. Digital Input Rise and Fall Times**

## DIGITAL CHARACTERISTICS (CONT.)

Parameter	Symbol	Min	Typ	Max	Unit
<b>Master Clock</b>					
MCLK Frequency (Note 25)	$f_{CLK}$	-	2.048	-	MHz
MCLK Period (Note 25)	$t_{mclk}$	-	488	-	ns
MCLK Duty Cycle (Note 8)	$MCLK_{DC}$	40	-	60	%
MCLK Rise Time (Note 8)	$t_{RISE}$	-	-	50	ns
MCLK Fall Time (Note 8)	$t_{FALL}$	-	-	50	ns
MCLK Jitter (In-band or aliased in-band) (Note 8)	$MCLK_{IBJ}$	-	-	300	ps
MCLK Jitter (Out-of-band) (Note 8)	$MCLK_{OBJ}$	-	-	1	ns
<b>Master Sync</b>					
MSYNC Setup Time to MCLK rising (Note 8, 26)	$t_{mss}$	20	122	-	ns
MSYNC Period (Note 8, 26)	$t_{msync}$	40	976	-	ns
MSYNC Hold Time after MCLK falling (Note 8, 26)	$t_{msh}$	20	122	-	ns
MSYNC Instant to TDATA Start (Note 8, 27)	$t_{tdata}$	-	1220	-	ns

- Notes: 25. MCLK is generated by the CS5376A digital filter. If MCLK is disabled, the device automatically enters a power-down state.
26. MSYNC is generated by the CS5376A digital filter and is latched on MCLK rising edge, synchronization instant ( $t_0$ ) on next MCLK rising edge.
27. TDATA can be delayed from 0 to 63 full bit periods by the CS5376A test bit stream generator. The timing diagram shows no TBSDATA delay.

## DIGITAL CHARACTERISTICS (CONT.)

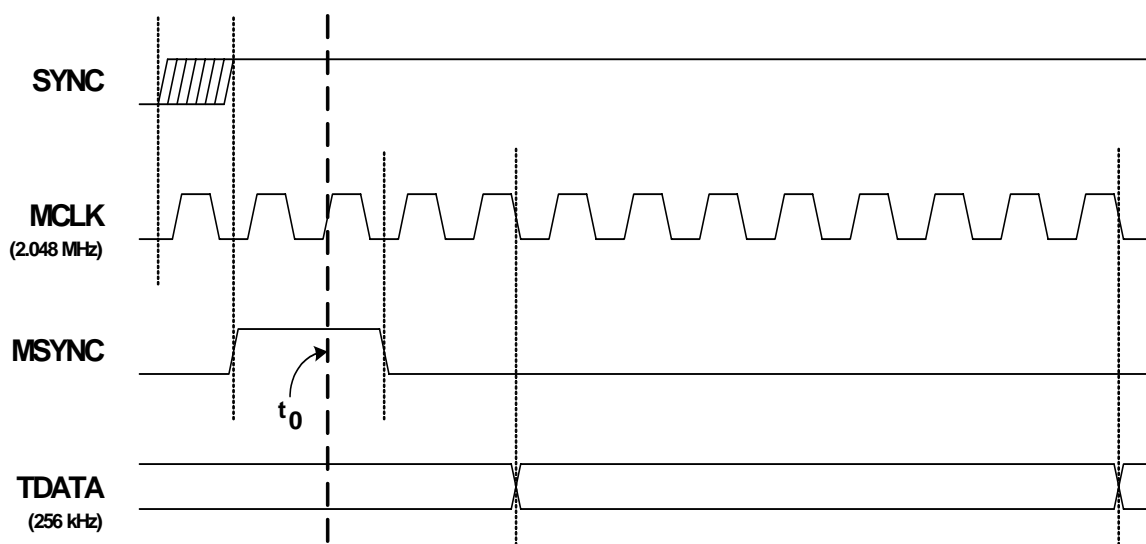


Figure 2. System Timing Diagram

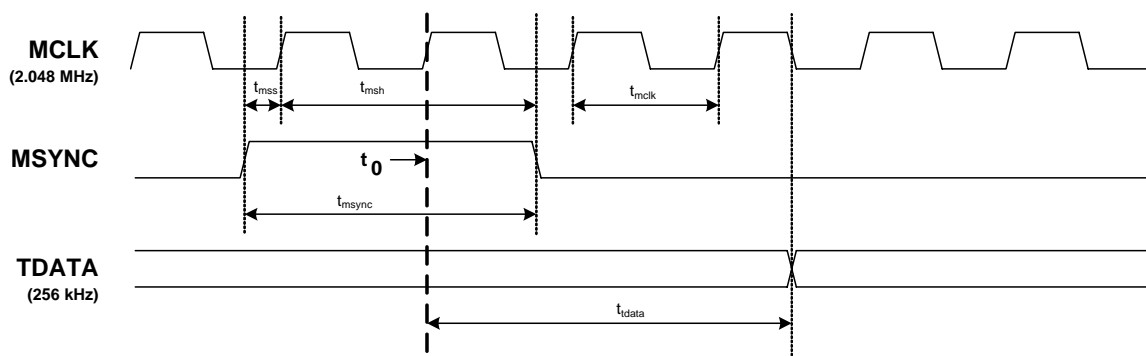


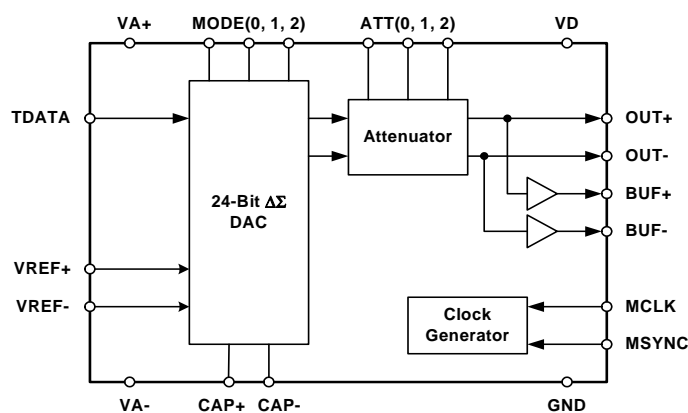
Figure 3. MCLK / MSYNC Timing Detail

## POWER SUPPLY CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
<b>AC Mode Supply Current (MODE = 1, 2, 3, 6)</b>					
Analog Power Supply Current (Note 28)	$I_A$	-	8	10	mA
Digital Power Supply Current (Note 28)	$I_D$	-	20	-	$\mu$ A
<b>DC Mode Supply Current (MODE = 4)</b>					
Analog Power Supply Current (Note 28)	$I_A$	-	2.7	-	mA
Digital Power Supply Current (Note 28)	$I_D$	-	20	-	$\mu$ A
<b>DC Mode Supply Current (MODE = 5)</b>					
Analog Power Supply Current (Note 28)	$I_A$	-	4.2	-	mA
Digital Power Supply Current (Note 28)	$I_D$	-	20	-	$\mu$ A
<b>Sleep Mode Supply Current (MODE = 0, 7)</b>					
Analog Power Supply Current (Note 28)	$I_A$	-	200	-	$\mu$ A
Digital Power Supply Current (Note 28)	$I_D$	-	260	-	$\mu$ A
<b>Power Down Supply Current (MCLK = 0)</b>					
Analog Power Supply Current (Note 28)	$I_A$	-	1	-	$\mu$ A
Digital Power Supply Current (Note 28)	$I_D$	-	20	-	$\mu$ A
Time to Enter Power Down (MCLK disabled) (Note 8)	$PD_{TC}$	-	40	-	$\mu$ S
<b>Power Supply Rejection</b>					
Power Supply Rejection Ratio (Note 29)	PSRR	-	90	-	dB

Notes: 28. All outputs unloaded. Digital inputs forced to VD or DGND respectively.

29. Power supply rejection is characterized by applying a 100 mVp-p 50-Hz sine wave to each supply.



**Figure 4. CS4373A Block Diagram**

## 2. GENERAL DESCRIPTION

The CS4373A is a differential output digital-to-analog converter with multiple operational modes and programmable output attenuation. It provides self-test and precision calibration capability for high-resolution, low-frequency measurement systems designed from CS3301A / CS3302A differential amplifiers, CS5371A / CS5372A  $\Delta\Sigma$  modulators, and the CS5376A digital filter.

### 2.1 Digital Inputs

The CS4373A is driven by a  $\Delta\Sigma$  digital bit stream from the CS5376A digital filter test bit stream (TBS) generator. The digital filter also provides clock and sync signals as well as GPIO control signals to set the operational mode and attenuation.

### 2.2 Analog Outputs

Two sets of differential analog outputs, *OUT* and *BUF*, simplify system design as dedicated outputs for testing the electronics channel and for in-circuit sensor tests. Output attenuator settings are binary weighted (1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64) and match the CS3301A / CS3302A amplifier input levels for full-scale testing at all gain ranges.

For maximum performance, the precision outputs (*OUT* $\pm$ ) must drive only high-impedance loads such as the CS3301A / CS3302A amplifier inputs. The buffered outputs (*BUF* $\pm$ ) can drive lower-impedance loads, down to 1 k $\Omega$ , but with reduced performance compared to the precision outputs.

### 2.3 Multiple Operational Modes

The CS4373A operates in either AC or DC test modes. AC test modes (MODE 1, 2, 3, 6) are used to measure system THD and CMRR performance. DC test modes (MODE 4, 5) are for gain calibration and pulse tests.

### 2.4 Low Power

The CS4373A is optimized for low-power operation and has a restricted operational bandwidth in the AC modes. For stable operation, full-scale AC test signals must not contain frequencies above 100 Hz. AC test signals above 100 Hz (TBS impulse mode, for example) must have a -20 dB reduced amplitude to ensure stability of the CS4373A low-power  $\Delta\Sigma$  architecture.



### 3. SYSTEM DIAGRAMS

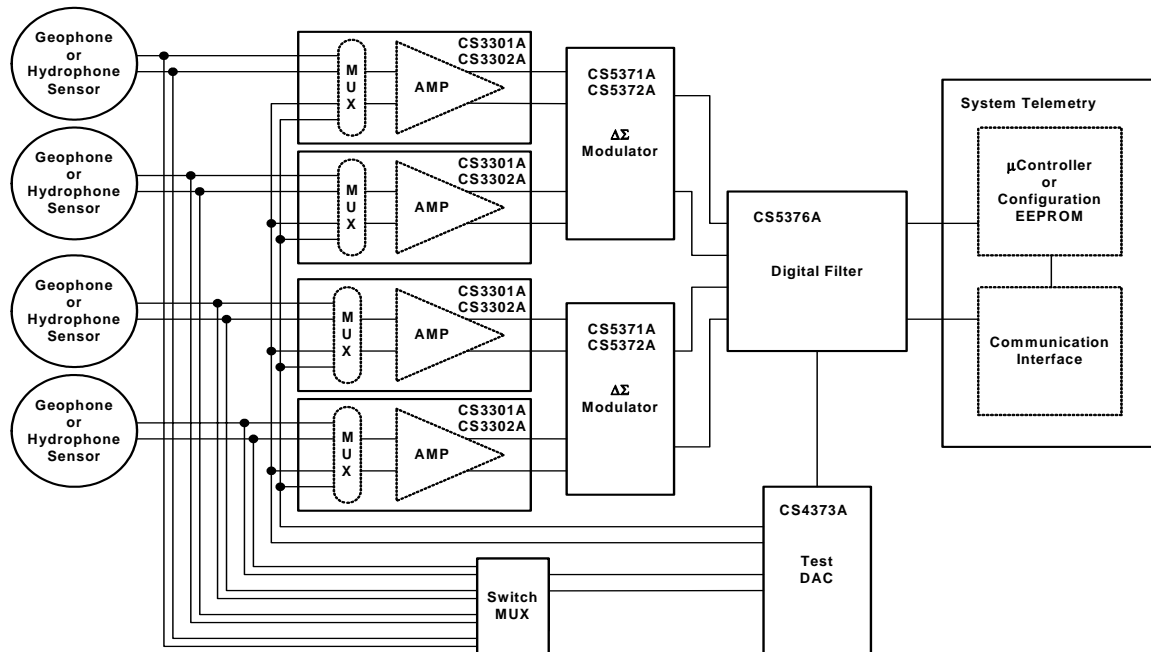


Figure 5. System Diagram

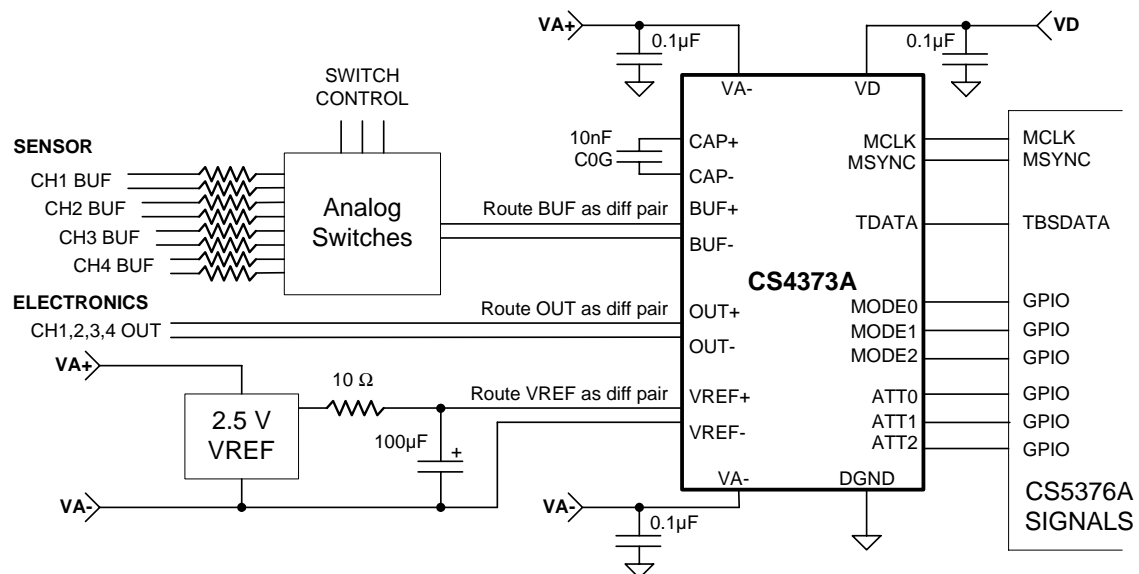
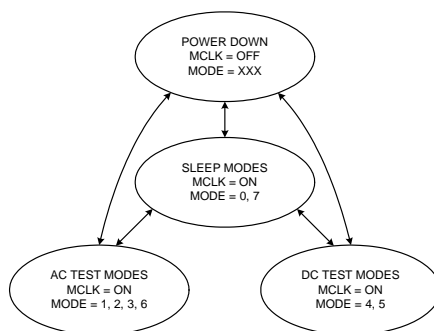


Figure 6. Connection Diagram



**Figure 7. Power Mode Diagram**

## 4. POWER MODES

The CS4373A has four power modes. AC test modes and DC test modes are operational modes, while the power down and sleep modes are non-operational, standby modes.

### 4.1 Power Down

If MCLK is stopped, an internal loss-of-clock detection circuit automatically places the CS4373A into power down. Power down is independent of the MODE and ATT pin settings, and is automatically invoked after approximately 40  $\mu$ s without an incoming MCLK edge.

In power down the AC and DC test circuitry is inactive and the analog outputs are high impedance. When used with the CS5376A digital filter, the CS4373A is powered down immediately after reset since MCLK is disabled by default.

### 4.2 Sleep Modes

With MCLK enabled, selecting either of the sleep modes (MODE 0, 7) places the CS4373A into a micropower sleep state. Following completion of the AC and DC system self-tests, the CS4373A is typically set into

sleep mode for normal data acquisition. In sleep mode the AC and DC test circuitry is inactive and the analog outputs are high impedance.

### 4.3 AC Test Modes

With MCLK and TDATA active, selecting an AC test mode (MODE 1, 2, 3, 6) causes the CS4373A to output AC waveforms on the enabled analog outputs. AC test modes use the low-power  $\Delta\Sigma$  circuitry in the CS4373A to create precision differential or common mode analog AC output signals from the encoded digital test bit stream (TBS) input.

### 4.4 DC Test Modes

With MCLK active, selecting a DC test mode (MODE 4, 5) causes the CS4373A to generate precision DC voltages on the analog outputs. DC test modes use switch-capacitor level-shifting buffer circuitry in the CS4373A to create differential or common mode DC analog output voltages from the voltage reference input.

## 5. OPERATIONAL MODES

The CS4373A has six operational modes and two sleep modes selected by the MODE2, MODE1, and MODE0 pins.

Selection	MODE[2:0]	Mode Description
0	0 0 0	Sleep mode.
1	0 0 1	AC OUT and BUF outputs.
2	0 1 0	AC OUT only, BUF high-z.
3	0 1 1	AC BUF only, OUT high-z.
4	1 0 0	DC common mode output.
5	1 0 1	DC differential output.
6	1 1 0	AC common mode output.
7	1 1 1	Sleep mode.

**Table 2. Operational Modes**

### 5.1 Sleep Modes

Sleep modes (MODE 0, 7) save power during normal acquisition by turning off the AC and DC test circuitry after system self-tests are complete. In sleep mode the *OUT* and *BUF* analog outputs are high impedance.

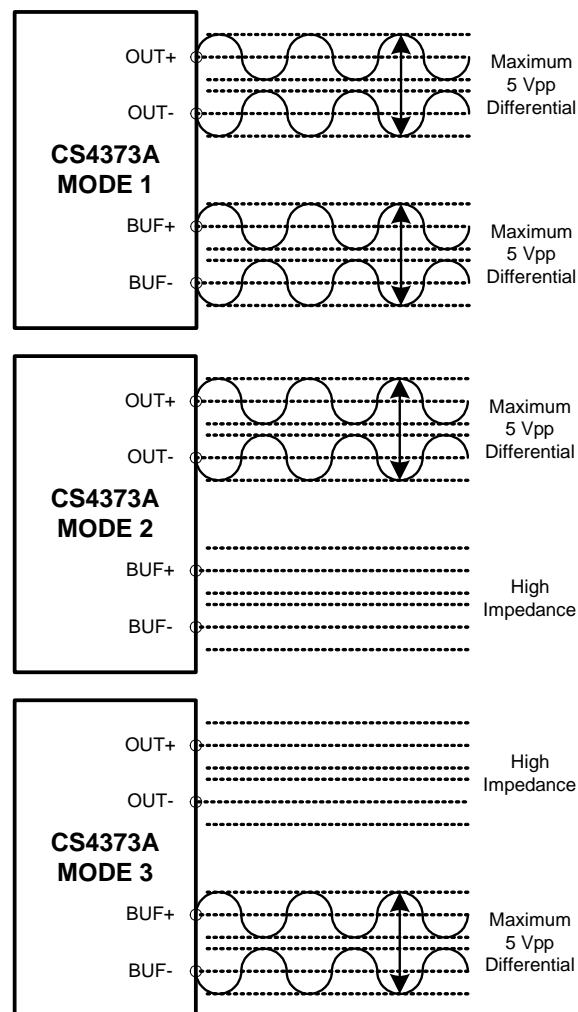
### 5.2 AC Test Modes

AC test modes use the digital test bit stream (TBS) input from the CS5376A digital filter to construct analog AC waveforms. The digital bit stream input to the TDATA pin encodes the analog waveform as over-sampled one bit  $\Delta\Sigma$  data, which is then converted into precision differential or common mode analog AC signals by the CS4373A.

#### 5.2.1 AC Differential

The first three AC test modes (MODE 1, 2, 3) create precision differential analog signals for THD and impulse testing of the measurement channel. In mode 1, both sets of differential analog outputs (*OUT* and *BUF*) are enabled. In mode 2 only the *OUT* analog output is enabled, and *BUF* is high impedance. In mode 3

only the *BUF* analog output is enabled, and *OUT* is high impedance.



**Figure 8. AC Differential Modes**

Differential AC signals out of the CS4373A consist of two halves with equal but opposite magnitude, varying about a common mode voltage. A full-scale 5 V<sub>PP</sub> differential AC signal centered on a -0.15 V common mode voltage will have:

$$\text{SIG+} = -0.15 \text{ V} + 1.25 \text{ V} = +1.1 \text{ V}$$

$$\text{SIG-} = -0.15 \text{ V} - 1.25 \text{ V} = -1.4 \text{ V}$$

$$\text{SIG+ is } +2.5 \text{ V relative to SIG-}$$

For the opposite case:

$$\text{SIG+} = -0.15 \text{ V} - 1.25 \text{ V} = -1.4 \text{ V}$$

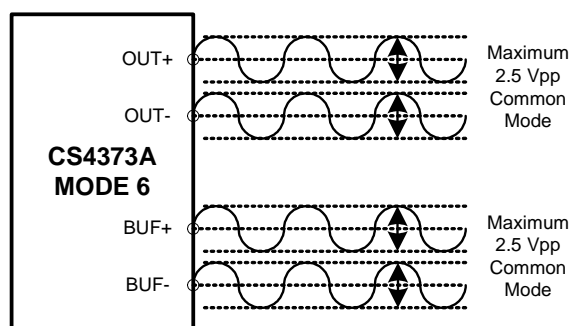
$$\text{SIG-} = -0.15 \text{ V} + 1.25 \text{ V} = +1.1 \text{ V}$$

SIG+ is -2.5 V relative to SIG-

So the total swing for SIG+ relative to SIG- is  $(+2.5 \text{ V}) - (-2.5 \text{ V}) = 5 \text{ V}_{\text{pp}}$  differential. A similar calculation can be done for SIG- relative to SIG+. It's important to note that a  $5 \text{ V}_{\text{pp}}$  differential signal centered on a -0.15 V common mode voltage never exceeds +1.1 V with respect to ground and never drops below -1.4 V with respect to ground on either half. By definition, differential voltages are measured with respect to the opposite half, not relative to ground. A voltmeter differentially measuring between SIG+ and SIG- in the above example would read  $1.767 \text{ V}_{\text{rms}}$ , or  $5 \text{ V}_{\text{pp}}$ .

### 5.2.2 AC Common Mode

The final AC test mode (MODE 6) creates a matched AC common mode analog signal for CMRR testing of the measurement channel. In mode 6, both sets of analog outputs (OUT and BUF) are enabled. There is no common mode AC waveform output for an attenuator setting of 1/64.



**Figure 9. AC Common Mode**

Gross leakage in the sensor channel can be detected by applying a full-scale AC common mode signal. If there is a significant differential mismatch in the channel due to sensor leakage, the AC common mode signal will be con-

verted to a measurable differential signal at the fundamental frequency.

### 5.2.3 AC Stability

For the CS4373A low-power  $\Delta\Sigma$  architecture to remain stable, the TDATA input bit stream should only encode 100 Hz or lower bandwidth analog signals. For TDATA bit stream frequencies above 100 Hz (for example, TBS impulse mode), the encoded amplitude must be reduced -20 dB below full scale to guarantee stability.

If the CS4373A low-power  $\Delta\Sigma$  architecture becomes unstable, persistent elevated noise will be present on the analog outputs and AC linearity will be poor. To recover stability, place the CS4373A into power down or sleep mode and restart the CS5376A test bit stream generator before placing the CS4373A back into an AC test mode.

## 5.3 DC Test Modes

DC test modes create precision level-shifted and buffered versions of the voltage reference input as precision DC common mode and DC differential analog outputs. The absolute accuracy of the DC test modes is highly dependent on the absolute accuracy of the voltage reference input voltage.

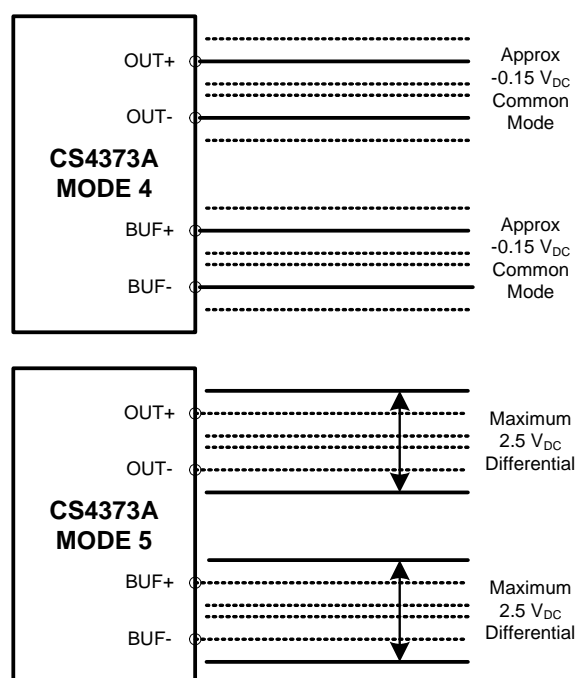
### 5.3.1 DC Common Mode

The first DC test mode (MODE 4) creates a matched DC common mode analog output voltage as a baseline measurement for gain calibration and differential pulse tests. In mode 4, both sets of analog outputs (OUT and BUF) are enabled.

### 5.3.2 DC Differential

The second DC test mode (MODE 5) creates a precision differential DC analog output voltage as the final measurement for gain calibration and as the step/pulse output for differential pulse tests. In mode 5, both sets of analog outputs (OUT and BUF) are enabled.

In DC differential output mode (MODE 5) the level-shifting buffer circuitry adds low-level 32 kHz switched-capacitor noise to the DC output. This noise is out of the measurement bandwidth for systems designed with CS3301A / CS3302A amplifiers and CS5371A / CS5372A modulators, and is rejected by the CS5376A digital filter. This 32 kHz switch-capacitor noise does not affect DC system tests, though it may be visible on an oscilloscope at high gain levels.



**Figure 10. DC Test Modes**

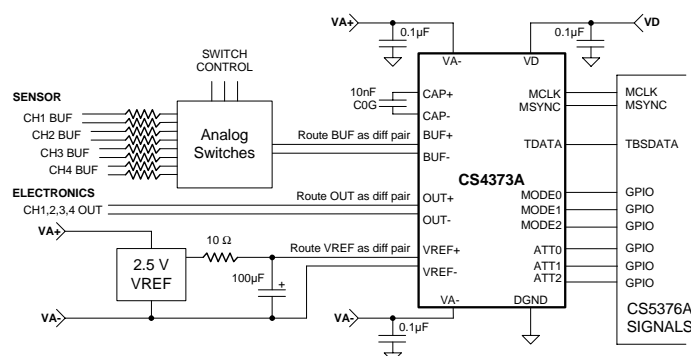
By measuring both DC test modes (MODE 4, 5), precision gain-calibration coefficients can be calculated for the measurement

channel. By first measuring the differential offset of the DC common mode output (MODE 4) and then measuring the DC differential mode amplitude (MODE 5), a precise offset corrected volts-to-codes conversion ratio can be calculated. This known ratio is then used to normalize the full-scale amplitude using the CS5376A digital filter GAIN registers to match other channels in the measurement network.

By switching between DC common mode (MODE 4) and DC differential mode (MODE 5), pulse waveforms can be created to characterize the step response of the measurement channel. If a pulse test requires precise timing control, an external controller should directly toggle the MODE pins of the CS4373A to avoid delays associated with writing to the CS5376A digital filter GPIO registers.

Sensor impedance can be measured using DC differential mode (MODE 5), provided matched series resistors are installed between the *BUF* analog outputs and the sensor. Applying the known DC differential voltage to the resistor-sensor-resistor string permits a ratio-metric sensor impedance calculation from the measured voltage drop across the sensor.

Switching between DC differential mode (MODE 5) and sleep mode (MODE 0, 7) can, in the case of a moving-coil geophone, test basic parameters of the electro-mechanical transfer function. The voltage relaxation characteristic of the sensor when switching the analog outputs from a differential DC voltage to high impedance depends primarily on the geophone resonant frequency and damping factor.



**Figure 11. Digital Inputs**

## 6. DIGITAL INPUTS

The CS4373A is designed to operate with the CS5376A digital filter. The digital filter generates one-bit  $\Delta\Sigma$  test bit stream data (TDATA), a master clock (MCLK) and a synchronization signal (MSYNC). In addition, the digital filter GPIO pins control the CS4373A operational mode (MODE) and attenuator (ATT) settings.

### 6.1 TDATA Connection

The TDATA digital input expects encoded one-bit  $\Delta\Sigma$  data nominally at a 256 kHz rate. The one's density input range is approximately 25% minimum to 75% maximum, with differential mid-scale at 50% one's density.

The CS5376A digital filter test bit stream (TBS) generator can encode two types of AC signals as over-sampled, one-bit  $\Delta\Sigma$  data - a pure sine wave for THD and CMRR testing or a triggerable impulse waveform for synchronization testing and impulse response characterization. In the AC operational modes, the CS4373A converts the over-sampled bit stream digital data into precision differential or common mode analog AC signals.

The CS5376A TBS sine mode encodes an approximately 5 V<sub>pp</sub> full-scale sine wave signal with a digital filter TBSGAIN register setting of 0x04B8F2. Because TBS impulse mode encodes frequencies above 100 Hz, a maximum 0x0078E5 TBSGAIN impulse mode register setting is specified to guarantee stability of the

CS4373A low-power  $\Delta\Sigma$  circuitry. Details on the setup and operation of the digital filter TBS generator can be found in the CS5376A data sheet.

### 6.2 MCLK Connection

The CS5376A digital filter generates the master clock for CS4373A, typically 2.048 MHz, from a synchronous CLK input from the external system. By default, MCLK is disabled at reset and is enabled by writing the digital filter CONFIG register. If MCLK is disabled during operation, the CS4373A will enter power down after approximately 40  $\mu$ S.

MCLK must have low in-band jitter to guarantee full analog performance, requiring a crystal- or VCXO-based system clock into the digital filter. Clock jitter on the digital filter external CLK input directly translates to jitter on MCLK.

### 6.3 MSYNC Connection

The CS5376A digital filter also provides a synchronization signal to the CS4373A. The MSYNC signal is generated following a rising edge received on the digital filter SYNC input. By default MSYNC generation is disabled at reset and is enabled by writing to the digital filter CONFIG register.

The input SYNC signal to the CS5376A digital filter sets a common reference time  $t_0$  for mea-



surement events, thereby synchronizing analog sampling across a measurement network. The timing accuracy of the input SYNC signal from measurement node to measurement node must be  $\pm 1$  MCLK to maximize MSYNC analog sample synchronization accuracy.

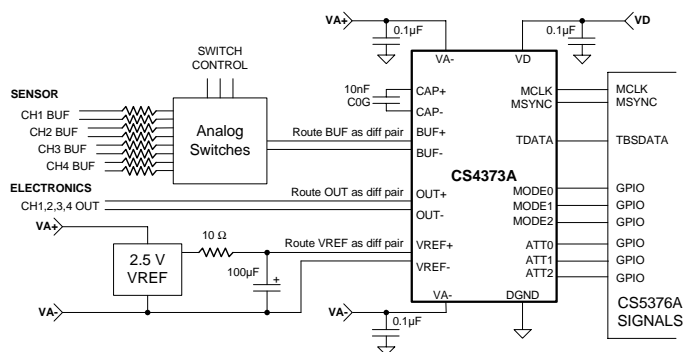
The CS4373A MSYNC input is rising-edge triggered and resets the internal MCLK counter/divider to guarantee synchronous operation with other system devices. While the MSYNC signal synchronizes the internal operation of the CS4373A, by default, it does not synchronize the phase of the encoded digital test bit stream (TBS) sine wave unless enabled in the digital filter TBSCFG register.

#### **6.4 GPIO Connections**

The CS5376A controls 12 general-purpose in-

put output (GPIO) pins through the digital filter GPCFG registers. These GPIO pins are typically assigned to operate the CS4373A mode and attenuator pins, along with the CS3301A / CS3302A amplifiers input mux and gain pins. The gain and attenuation settings of the CS3301A / CS3302A amplifiers and CS4373A are identically decoded to allow full-scale performance testing at all system gain ranges with shared GAIN and ATT control signals.

If precise timing control of operational modes is required (for example, switching between DC modes for pulse generation), an external controller should directly toggle the MODE pins of the CS4373A to avoid the delay associated with writing to the CS5376A digital filter GPCFG registers.



**Figure 12. Analog Outputs**

## 7. ANALOG OUTPUTS

The CS4373A has multiple differential analog outputs. The best possible analog performance is achieved from the precision outputs ( $OUT_{\pm}$ ), but with only minimal drive capability. A buffered output ( $BUF_{\pm}$ ) can drive an external load, but with reduced analog performance. The internal anti-alias filter requires a dedicated capacitor connection ( $CAP_{\pm}$ ) to eliminate undesired high-frequency signals.

### 7.1 Differential Signals

Differential AC signals out of the CS4373A consist of two halves with equal but opposite magnitude varying about a common mode voltage. A full-scale  $5 V_{pp}$  differential AC signal centered on a  $-0.15 V$  common mode voltage will have:

$$SIG+ = -0.15 V + 1.25 V = +1.1 V$$

$$SIG- = -0.15 V - 1.25 V = -1.4 V$$

$SIG+$  is  $+2.5 V$  relative to  $SIG-$

For the opposite case:

$$SIG+ = -0.15 V - 1.25 V = -1.4 V$$

$$SIG- = -0.15 V + 1.25 V = +1.1 V$$

$SIG+$  is  $-2.5 V$  relative to  $SIG-$

So the total swing for  $SIG+$  relative to  $SIG-$  is  $(+2.5 V) - (-2.5 V) = 5 V_{pp}$  differential. A similar calculation can be done for  $SIG-$  relative to  $SIG+$ . It's important to note that a  $5 V_{pp}$  differential signal centered on a  $-0.15 V$  common

mode voltage never exceeds  $+1.1 V$  with respect to ground and never drops below  $-1.4 V$  with respect to ground on either half. By definition, differential voltages are measured with respect to the opposite half, not relative to ground. A voltmeter differentially measuring between  $SIG+$  and  $SIG-$  in the above example would read  $1.767 V_{rms}$ , or  $5 V_{pp}$ .

### 7.2 Analog Output Attenuation

The CS4373A has seven analog output attenuation settings from  $1/1$  to  $1/64$  selected with the  $ATT2$ ,  $ATT1$ , and  $ATT0$  pins. At  $1/64$  attenuation in AC Common Mode (MODE 6) there is no output signal amplitude due to the attenuator architecture.

Selection	ATT[2:0]	Attenuation	dB
0	0 0 0	1/1	0 dB
1	0 0 1	1/2	-6.02 dB
2	0 1 0	1/4	-12.04 dB
3	0 1 1	1/8	-18.06 dB
4	1 0 0	1/16	-24.08 dB
5	1 0 1	1/32	-30.10 dB
6	1 1 0	1/64	-36.12 dB
7	1 1 1	reserved	reserved

**Table 3. Output Attenuation Settings**



When enabled, attenuation is applied to both the *OUT* and *BUF* differential analog outputs. The *OUT* $\pm$  pins connect directly into the internal attenuator resistors and so attenuation accuracy is highly sensitive to load impedance on the *OUT* $\pm$  pins. Loading on the *BUF* $\pm$  pins does not affect attenuator accuracy.

The attenuation settings of CS4373A match the gain ranges of the CS3301A / CS3302A differential amplifiers to enable full-scale testing at all gain ranges. The CS3301A / CS3302A amplifier gain settings (GAIN) are decoded identical to the CS4373A attenuator settings (ATT) and so can share GPIO signals from the digital filter.

### 7.3 *OUT* $\pm$ Precision Output

The *OUT* $\pm$  pins are precision differential analog outputs for testing the high-performance electronics measurement channel. These precision outputs have higher performance specifications than the *BUF* outputs, but with a much higher sensitivity to external loading. Excessive resistive or capacitive loading on the *OUT* $\pm$  pins will degrade the analog performance characteristics of the CS4373A in all operational modes.

The *OUT* $\pm$  precision output is optimized for direct connection to the CS3301A / CS3302A amplifier differential inputs, which have very high input impedance. These amplifiers include a pin-controlled input multiplexer to switch between an internal differential termination for noise tests and two external differential inputs. One external amplifier input is typically dedicated to sensor measurements and the other to testing the electronics channel.

The *OUT* $\pm$  outputs are enabled in all operational modes except “AC BUF Only” mode (MODE 3) and sleep modes (MODE 0, 7). In

AC BUF Only and sleep modes the *OUT* $\pm$  pins are high impedance.

### 7.4 *BUF* $\pm$ Buffered Output

The *BUF* $\pm$  pins are buffered differential analog outputs for testing external sensors such as geophones or hydrophones. The buffered outputs have reduced performance specifications compared with the *OUT* outputs, but are less sensitive to external loading.

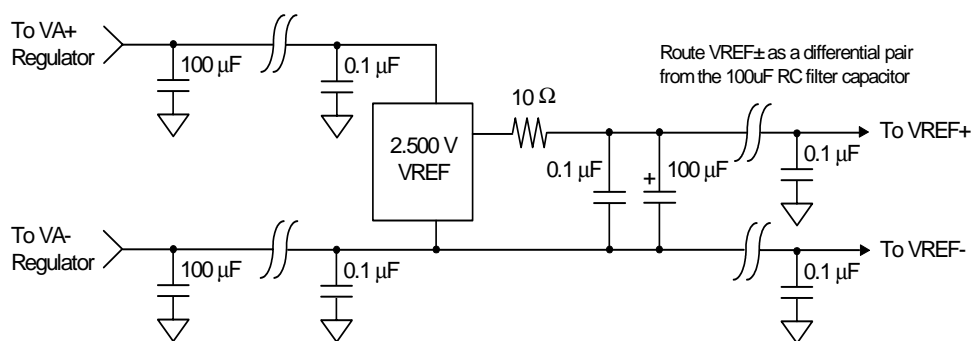
The *BUF* $\pm$  outputs are enabled in all operational modes except “AC OUT Only” mode (MODE 2) and sleep modes (MODE 0, 7). In AC OUT Only and sleep modes the *BUF* $\pm$  pins are high impedance to ensure they do not interfere with sensor operation during normal data acquisition.

For sensor impedance testing, it is required to place matched series resistors in between the *BUF* $\pm$  outputs and the differential sensor. With known series resistors and a known DC differential source voltage, sensor resistance can be calculated ratiometrically from the measured voltage drop across the sensor.

### 7.5 *CAP* $\pm$ Analog Output

The CS4373A requires a 10 nF COG or NPO-type capacitor connected differentially across the *CAP* $\pm$  pins. This capacitor creates an internal anti-alias filter to eliminate high-frequency signals from the *OUT* $\pm$  and *BUF* $\pm$  analog outputs and helps to maintain the stability of the low-power  $\Delta\Sigma$  circuitry.

A COG, NPO or similar high-quality capacitor is required for *CAP* $\pm$  since other capacitor types, such as X7R, do not have the required linearity. Using a poor-quality capacitor on *CAP* $\pm$  will significantly degrade THD performance in the AC operational modes.



**Figure 13. Voltage Reference Circuit**

## 8. VOLTAGE REFERENCE

The CS4373A requires a 2.500 V precision voltage reference to be supplied to the VREF± pins.

### 8.1 VREF Power Supply

To guarantee proper regulation headroom for the voltage reference device, the voltage reference GND pin should be connected to VA- instead of system ground, as shown in [Figure 13](#). This connection results in VREF- voltage equal to VA- and VREF+ voltage very near ground potential  $[(VA-) + 2.500 \text{ VREF}]$ .

Power supply inputs to the voltage reference device should be bypassed to system ground with 0.1 µF capacitors placed as close as possible to the power and ground pins. In addition to 0.1 µF local bypass capacitors, at least 100 µF of bulk capacitance to system ground should be placed on each power supply near the voltage regulator outputs. Bypass capacitors should be X7R, C0G, tantalum, or other high-quality dielectric type.

### 8.2 VREF RC Filter

A primary concern in selecting a precision voltage reference is noise performance in the measurement bandwidth. The [Linear Technol-](#)

[ogy LT1019AIS8-2.5](#) voltage reference yields acceptable noise levels if the output is filtered with a low-pass RC filter.

A separate RC filter is required for each system device connected to a given voltage reference. By sharing a common RC filter, signal-dependent sampling of the voltage reference by one system device could cause unwanted tones to appear in the measurement bandwidth of another system device via common impedance coupling.

### 8.3 VREF PCB Routing

To minimize the possibility of outside noise coupling into the CS4373A voltage reference input, the VREF± traces should be routed as a differential pair from the large capacitor of the voltage reference RC filter. Careful control of the voltage reference source and return currents by routing VREF± as a differential pair will improve immunity from external noise.

To further improve noise rejection of the VREF± routing, include 0.1 µF bypass capacitors to system ground as close as possible to the VREF+ and VREF- pins of the CS4373A.

#### 8.4 VREF Input Impedance

The switched-capacitor input architecture of the VREF± inputs results in an input impedance that depends on the internal capacitor size and the clock frequency. With a 15 pF internal capacitor and a 2.048 MHz MCLK the VREF input impedance is approximately  $[1 / [(2.048 \text{ MHz}) * (15 \text{ pF})]] = 32 \text{ k}\Omega$ . While the size of the internal capacitor is fixed, the voltage reference input impedance will vary with MCLK.

The voltage reference external RC filter series resistor creates a voltage divider with the VREF input impedance to reduce the effective applied input voltage. To minimize gain error resulting from this voltage divider effect, the RC filter series resistor should be the minimum size recommended in the voltage reference device data sheet.

#### 8.5 VREF Accuracy

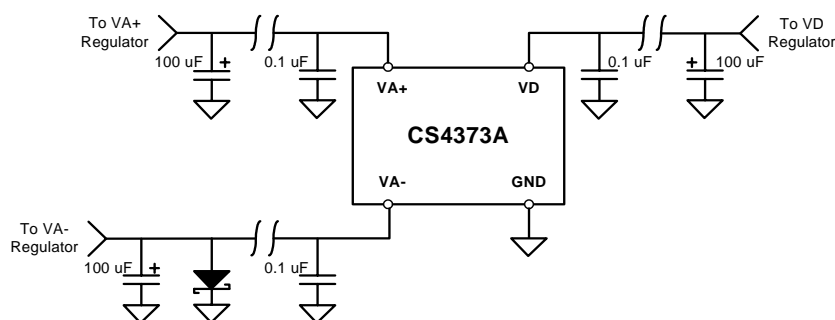
The nominal voltage reference input is specified as 2.500 V across the VREF± pins, and all CS4373A gain accuracy specifications are measured with a nominal voltage reference input. Any variation from a nominal VREF input will proportionally vary the analog full-scale gain accuracy.

Since temperature drift of the voltage reference results in gain drift of the analog full-scale amplitude, care should be taken to minimize temperature drift effects through careful selection of passive components and the voltage reference device itself. Gain drift specifications of the CS4373A do not include the temperature drift effects of external passive components or of the voltage reference device itself.

#### 8.6 VREF Independence

If the test signal source is required to be fully independent of the measurement channel, a separate voltage reference device for the CS4373A is required. Using a separate voltage reference minimizes the possibility of undetected ratiometric errors when the same voltage reference is used by both the test signal source and the measurement channel.

Because modern precision voltage references are highly reliable, requirements for separate modulator and test DAC voltage references should be considered carefully. In the unlikely event of voltage reference failure independent of other system components, the CS4373A volts-to-codes ratio will be out of spec and performance will be poor during system self-tests.



**Figure 14. Power Supply Diagram**

## 9. POWER SUPPLIES

The CS4373A has a positive analog power supply pin (VA+), a negative analog power supply pin (VA-), a digital power supply pin (VD), and a ground pin (GND).

For proper operation, power must be supplied to all power supply pins, and the ground pin must be connected to system ground. The CS4373A digital power supply (VD) and the CS5376A digital power supplies (VDD1 / VDD2) must share a common power supply voltage.

### 9.1 Power Supply Bypassing

The VA+, VA-, and VD power supplies should be bypassed to system ground with 0.1  $\mu$ F capacitors placed as close as possible to the power pins of the device. In addition to the 0.1  $\mu$ F local bypass capacitors, at least 100  $\mu$ F bulk capacitance to system ground should be placed on each power supply near the voltage regulator output, with additional power supply bulk capacitance placed among the analog component route if space permits. Bypass capacitors should be X7R, C0G, tantalum, or other high-quality dielectric type.

### 9.2 PCB Layers and Routing

The CS4373A is a high-performance device, and special care must be taken to ensure power and ground routing is correct. Power can be supplied either through dedicated power

planes or routed traces. When routing power traces, it is recommended to use a “star” routing scheme with the star point either at the voltage regulator output or at a local power supply bulk capacitor.

It is also recommended to dedicate a full PCB layer to a solid ground plane, without splits or routing. All bypass capacitors should connect between the power supply circuit and the solid ground plane as near as possible to the device power supply pins.

The CS4373A analog outputs are differentially routed and do not normally require connection to a separate analog ground. However, if a separate analog ground is required, it should be routed using a “star” routing scheme on a separate layer from the solid ground plane and connected to the ground plane only at the star point. Be sure all active devices and passive components connected to the analog ground are included in the “star” route to ensure sensitive analog currents do not return through the ground plane.

### 9.3 Power Supply Rejection

Power supply rejection of the CS4373A is frequency dependent. The CS5376A digital filter rejects power supply noise for frequencies above the selected digital filter corner frequency. Power supply noise frequencies between DC and the digital filter corner frequency are

rejected as specified in the [Power Supply Characteristics](#) table.

#### 9.4 SCR Latch-up

The VA- pin is tied to the CS4373A CMOS substrate and must always be the most-negative voltage applied to the device to ensure SCR latch-up does not occur. In general, latch-up may occur when any pin voltage exceeds the limits of the [Absolute Maximum Ratings](#) table.

It is recommended to connect the VA- power supply to system ground (GND) with a reverse-biased Schottky diode. At power up, if the VA+ power supply ramps before the VA- supply is established, the VA- pin voltage could be pulled above ground potential through the CS4373A device. If the VA- supply is pulled 0.7 V or more above GND, SCR latch-up can occur. A reverse-biased Schottky diode will clamp the VA- voltage a maximum of 0.3 V above ground to ensure SCR latch-up does not occur at power up.

#### 9.5 DC-DC Converters

Many low-frequency measurement systems

are battery powered and utilize DC-DC converters to efficiently generate power supply voltages. To minimize interference effects, operate the DC-DC converter at a frequency which is rejected by the digital filter, or operate it synchronous to the MCLK rate.

A synchronous DC-DC converter whose operating frequency is derived from MCLK will theoretically minimize the potential for “beat frequencies” to appear in the measurement bandwidth. However this requires the source clock to remain jitter-free within the DC-DC converter circuitry. If clock jitter can occur within the DC-DC converter (as in a PLL-based architecture), it’s better to use a non-synchronous DC-DC converter whose switching frequency is rejected by the digital filter.

During PCB layout, do not place high-current DC-DC converters near sensitive analog components. Carefully routing a separate DC-DC “star” ground will help isolate noisy switching currents away from the sensitive analog components.

## 10. TERMINOLOGY

- **Signal-to-Noise Ratio (Dynamic Range)** - Ratio of the rms magnitude of the full-scale signal to the integrated rms noise from DC to 430 Hz. The following formula is used to calculate SNR:

$$SNR = 20\log \left( \frac{\text{rms magnitude of full scale signal}}{\text{rms magnitude of noise floor}} \right)$$

- **Total Harmonic Distortion** - Ratio of the power of the fundamental frequency to the sum of the powers of all harmonic frequencies from DC to 430 Hz. The following formula is used to calculate THD:

$$THD = 10\log \left( \frac{\text{sum of the powers of the harmonic frequencies}}{\text{power of the fundamental frequency}} \right)$$

- **Full-scale Bandwidth** - The bandwidth in which the converter can generate a full-scale signal while maintaining performance specifications.
- **Impulse Amplitude** - The maximum amplitude of the output signal beyond the full-scale bandwidth.
- **Differential Output Level** - The voltage between the analog output pins of the device.
- **Full-scale Accuracy** - Variation in the measured output voltage from the theoretical full-scale output voltage at 1x attenuation. The following formula is used to calculate full-scale accuracy:

$$\text{full scale accuracy} = \left| \left( \frac{\text{measured full scale voltage} - \text{theoretical full scale voltage}}{\text{theoretical full scale voltage}} \right) \cdot 100\% \right|$$

- **Relative Accuracy** - Variation in the measured output voltage from the theoretical attenuated output voltage at each of the attenuation ranges. The following formula is used to calculate relative accuracy:

$$\text{relative accuracy} = \left| \left( \frac{\text{measured attenuated voltage} - \text{theoretical attenuated voltage}}{\text{theoretical attenuated voltage (relative to the measured full scale voltage)}} \right) \cdot 100\% \right|$$

- **Full Scale Drift** - The variation of the measured full-scale voltage across the specified temperature range.
- **Common Mode Drift** - The variation in the measured common mode voltage across the specified temperature range.



## 11. PIN DESCRIPTION

Positive Capacitor Output	<b>CAP+</b>	1	28	<b>GND</b>	System Ground
Negative Capacitor Output	<b>CAP-</b>	2	27	<b>MODE0</b>	Mode Select
Positive Buffered Output	<b>BUF+</b>	3	26	<b>MODE1</b>	Mode Select
Negative Buffered Output	<b>BUF-</b>	4	25	<b>MODE2</b>	Mode Select
Positive High Precision Output	<b>OUT+</b>	5	24	<b>ATT0</b>	Attenuation Range Select
Negative High Precision Output	<b>OUT-</b>	6	23	<b>ATT1</b>	Attenuation Range Select
Positive Analog Power Supply	<b>VA+</b>	7	22	<b>ATT2</b>	Attenuation Range Select
Negative Analog Power Supply	<b>VA-</b>	8	21	<b>TDATA</b>	Signal Bitstream Input
Negative Voltage Reference	<b>VREF-</b>	9	20	<b>VD</b>	Positive Digital Power Supply
Positive Voltage Reference	<b>VREF+</b>	10	19	<b>GND</b>	System Ground
No Connect	<b>NC</b>	11	18	<b>MCLK</b>	Master Clock Input
No Connect	<b>NC</b>	12	17	<b>MSYNC</b>	Master Sync Input
No Connect	<b>NC</b>	13	16	<b>DNC</b>	Do Not Connect
No Connect	<b>NC</b>	14	15	<b>DNC</b>	Do Not Connect

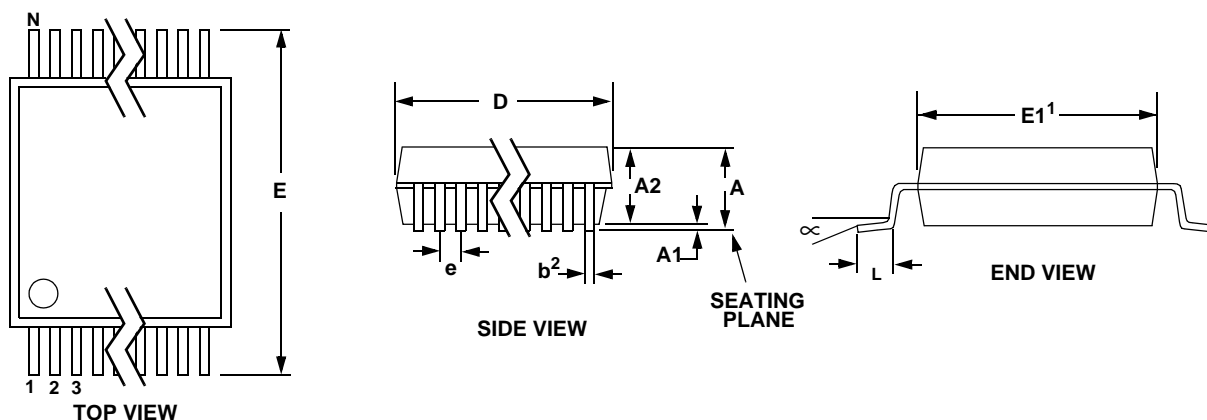
Pin Name	Pin #	I/O	Pin Description
<b>CAP+, CAP-</b>	1 2	O	Capacitor connection for internal anti-alias filter.
<b>BUF+, BUF-</b>	3 4	O	Buffered differential analog output.
<b>OUT+, OUT-</b>	5 6	O	Precision differential analog output.
<b>VA+, VA-</b>	7 8	I	Analog power supply. Refer to the Specified Operating Conditions.
<b>VREF-, VREF+</b>	9 10	I	Voltage reference input. Refer to the Specified Operating Conditions.
<b>MSYNC</b>	17	I	Master Sync Input. Low to high transition resets the internal clock phasing.
<b>MCLK</b>	18	I	Master Clock Input. CMOS compatible clock input.
<b>GND</b>	19		System ground.
<b>VD</b>	20		Digital power supply. Refer to the Specified Operating Conditions.
<b>TDATA</b>	21	I	Test Bit Stream input from digital filter TBS generator.

Pin Name	Pin #	I/O	Pin Description																																								
ATT2, ATT1, ATT0	22, 23, 24	I	Attenuation Range. Selects the output attenuation range.																																								
			<table><tr><th colspan="4">Attenuation</th></tr><tr><th>Selection</th><th>ATT[2:0]</th><th>Attenuation</th><th>dB</th></tr><tr><td>0</td><td>0 0 0</td><td>1/1</td><td>0 dB</td></tr><tr><td>1</td><td>0 0 1</td><td>1/2</td><td>-6.02 dB</td></tr><tr><td>2</td><td>0 1 0</td><td>1/4</td><td>-12.04 dB</td></tr><tr><td>3</td><td>0 1 1</td><td>1/8</td><td>-18.06 dB</td></tr><tr><td>4</td><td>1 0 0</td><td>1/16</td><td>-24.08 dB</td></tr><tr><td>5</td><td>1 0 1</td><td>1/32</td><td>-30.10 dB</td></tr><tr><td>6</td><td>1 1 0</td><td>1/64</td><td>-36.12 dB</td></tr><tr><td>7</td><td>1 1 1</td><td>reserved</td><td>reserved</td></tr></table>	Attenuation				Selection	ATT[2:0]	Attenuation	dB	0	0 0 0	1/1	0 dB	1	0 0 1	1/2	-6.02 dB	2	0 1 0	1/4	-12.04 dB	3	0 1 1	1/8	-18.06 dB	4	1 0 0	1/16	-24.08 dB	5	1 0 1	1/32	-30.10 dB	6	1 1 0	1/64	-36.12 dB	7	1 1 1	reserved	reserved
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			4	1 0 0	1/16	-24.08 dB																																					
			5	1 0 1	1/32	-30.10 dB																																					
			6	1 1 0	1/64	-36.12 dB																																					
7	1 1 1	reserved	reserved																																								
MODE2, MODE1, MODE0	25, 26, 27	I	Mode Selection. Determines the operational mode of the device.																																								
			<table><tr><th>Selection</th><th>MODE[2:0]</th><th>Mode Description</th></tr><tr><td>0</td><td>0 0 0</td><td>Sleep mode.</td></tr><tr><td>1</td><td>0 0 1</td><td>AC OUT and BUF outputs.</td></tr><tr><td>2</td><td>0 1 0</td><td>AC OUT only, BUF tri-state.</td></tr><tr><td>3</td><td>0 1 1</td><td>AC BUF only, OUT tri-state.</td></tr><tr><td>4</td><td>1 0 0</td><td>DC common mode output.</td></tr><tr><td>5</td><td>1 0 1</td><td>DC differential output.</td></tr><tr><td>6</td><td>1 1 0</td><td>AC common mode output.</td></tr><tr><td>7</td><td>1 1 1</td><td>Sleep mode.</td></tr></table>	Selection	MODE[2:0]	Mode Description	0	0 0 0	Sleep mode.	1	0 0 1	AC OUT and BUF outputs.	2	0 1 0	AC OUT only, BUF tri-state.	3	0 1 1	AC BUF only, OUT tri-state.	4	1 0 0	DC common mode output.	5	1 0 1	DC differential output.	6	1 1 0	AC common mode output.	7	1 1 1	Sleep mode.													
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7	1 1 1	Sleep mode.																																									
GND	28		System ground.																																								



## 12. PACKAGE DIMENSIONS

### 28L SSOP PACKAGE DRAWING



DIM	INCHES			MILLIMETERS			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.15	0.25	
A2	0.064	0.069	0.074	1.62	1.75	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.390	0.4015	0.413	9.90	10.20	10.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.0354	0.041	0.63	0.90	1.03	
∞	0°	4°	8°	0°	4°	8°	

**JEDEC #: MO-150**

*Controlling Dimension is Millimeters*

- Notes:
1. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
  2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
  3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

## 13.ORDERING INFORMATION

Model	Temperature	Package
CS4373A-ISZ (lead free)	-40 to +85 °C	28-pin SSOP

## 14.ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS4373A-ISZ (lead free)	260 °C	3	7 Days

\* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

## 15.REVISION HISTORY

Revision	Date	Changes
PP1	MAR 2003	Preliminary release for CS4373.
PP2	SEP 2005	Update for new CS4373A features and most-current characterization data.
PP3	NOV 2005	Remove references to CS5378. Update for most-current characterization data.
F1	DEC 2005	Updated with final characterization data.
F2	DEC 2006	Updated to final status with most-recent characterization data for Cirrus QPL process.

## Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to [www.cirrus.com](http://www.cirrus.com)

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