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Kind regards,

Team Nexperia

# DATA SHEET

**74F00**

Quad 2-input NAND gate

Product specification

1990 Oct 04

IC15 Data Handbook

Quad 2-input NAND gate

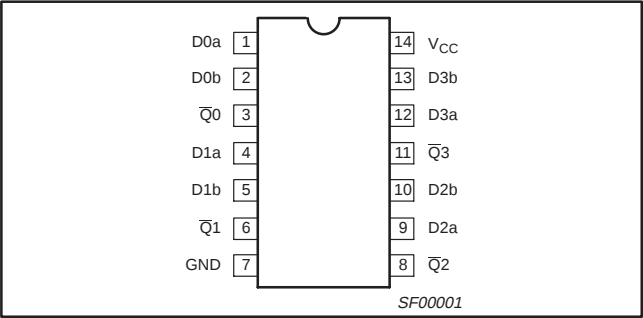
74F00

FEATURE

- Industrial temperature range available (−40°C to +85°C)

| TYPE  | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|-------|---------------------------|--------------------------------|
| 74F00 | 3.4ns                     | 4.4mA                          |

PIN CONFIGURATION



ORDERING INFORMATION

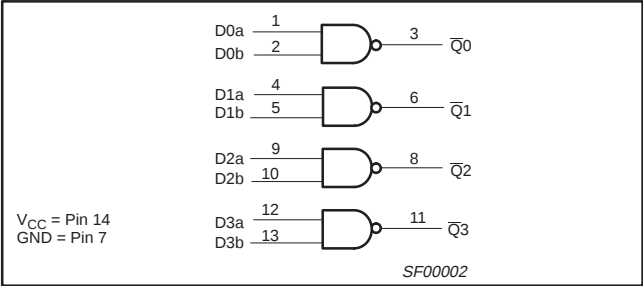
| DESCRIPTION        | ORDER CODE                                                                            |                                                                                         | PKG DWG # |
|--------------------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|-----------|
|                    | COMMERCIAL RANGE<br>$V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ | INDUSTRIAL RANGE<br>$V_{CC} = 5V \pm 10\%$ , $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$ |           |
| 14-pin plastic DIP | N74F00N                                                                               | I74F00N                                                                                 | SOT27-1   |
| 14-pin plastic SO  | N74F00D                                                                               | I74F00D                                                                                 | SOT108-1  |

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

| PINS        | DESCRIPTION | 74F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|-------------|-------------|---------------------|---------------------|
| Dna, Dnb    | Data inputs | 1.0/1.0             | 20μA/0.6mA          |
| $\bar{Q}_n$ | Data output | 50/33               | 1.0mA/20mA          |

NOTE: One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM

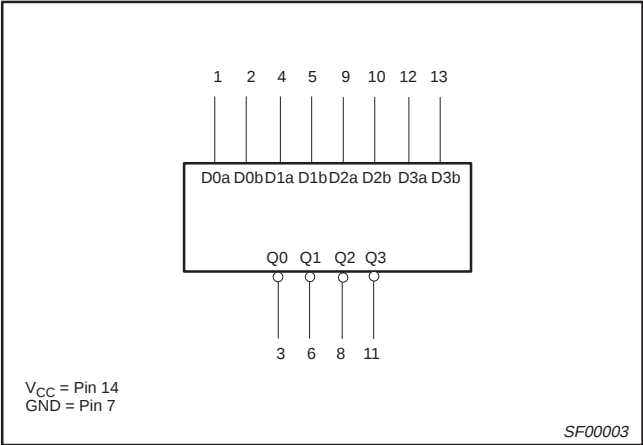


FUNCTION TABLE

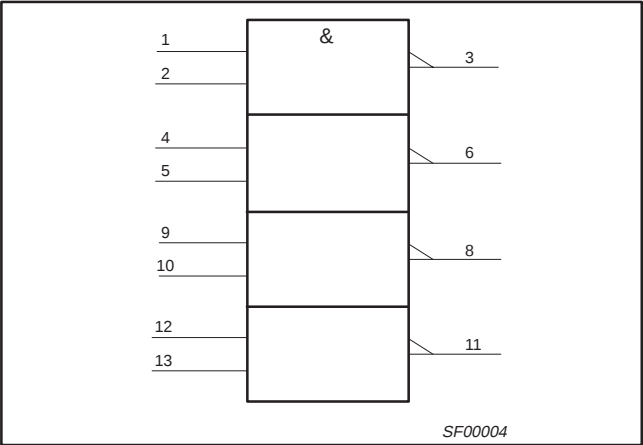
| INPUTS |     | OUTPUT      |
|--------|-----|-------------|
| Dna    | Dnb | $\bar{Q}_n$ |
| L      | L   | H           |
| L      | H   | H           |
| H      | L   | H           |
| H      | H   | L           |

NOTES:  
H = High voltage level  
L = Low voltage level

LOGIC SYMBOL



IEC/IEEE SYMBOL



## Quad 2-input NAND gate

74F00

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free air temperature range.)

| SYMBOL    | PARAMETER                                      |                  | RATING           | UNIT |
|-----------|------------------------------------------------|------------------|------------------|------|
| $V_{CC}$  | Supply voltage                                 |                  | -0.5 to +7.0     | V    |
| $V_{IN}$  | Input voltage                                  |                  | -0.5 to +7.0     | V    |
| $I_{IN}$  | Input current                                  |                  | -30 to +5        | mA   |
| $V_{OUT}$ | Voltage applied to output in high output state |                  | -0.5 to $V_{CC}$ | V    |
| $I_{OUT}$ | Current applied to output in low output state  |                  | 40               | mA   |
| $T_{amb}$ | Operating free air temperature range           | Commercial range | 0 to +70         | °C   |
|           |                                                | Industrial range | -40 to +85       | °C   |
| $T_{stg}$ | Storage temperature range                      |                  | -65 to +150      | °C   |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL    | PARAMETER                            |                  | LIMITS |     |     | UNIT |
|-----------|--------------------------------------|------------------|--------|-----|-----|------|
|           |                                      |                  | MIN    | NOM | MAX |      |
| $V_{CC}$  | Supply voltage                       |                  | 4.5    | 5.0 | 5.5 | V    |
| $V_{IH}$  | High-level input voltage             |                  | 2.0    |     |     | V    |
| $V_{IL}$  | Low-level input voltage              |                  |        |     | 0.8 | V    |
| $I_{IK}$  | Input clamp current                  |                  |        |     | -18 | mA   |
| $I_{OH}$  | High-level output current            |                  |        |     | -1  | mA   |
| $I_{OL}$  | Low-level output current             |                  |        |     | 20  | mA   |
| $T_{amb}$ | Operating free air temperature range | Commercial range | 0      |     | +70 | °C   |
|           |                                      | Industrial range | -40    |     | +85 | °C   |

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL   | PARAMETER                                 |           | TEST CONDITIONS <sup>1</sup>                                                             |                        | LIMITS |                  |      | UNIT          |
|----------|-------------------------------------------|-----------|------------------------------------------------------------------------------------------|------------------------|--------|------------------|------|---------------|
|          |                                           |           |                                                                                          |                        | MIN    | TYP <sup>2</sup> | MAX  |               |
| $V_{OH}$ | High-level output voltage                 |           | $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$<br>$V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$ | $\pm 10\%V_{CC}$       | 2.5    |                  |      | V             |
|          |                                           |           |                                                                                          | $\pm 5\%V_{CC}$        | 2.7    | 3.4              |      | V             |
| $V_{OL}$ | Low-level output voltage                  |           | $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$<br>$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$ | $\pm 10\%V_{CC}$       |        | 0.30             | 0.50 | V             |
|          |                                           |           |                                                                                          | $\pm 5\%V_{CC}$        |        | 0.30             | 0.50 | V             |
| $V_{IK}$ | Input clamp voltage                       |           | $V_{CC} = \text{MIN}, I_I = I_{IK}$                                                      |                        |        | -0.73            | -1.2 | V             |
| $I_I$    | Input current at maximum input voltage    |           | $V_{CC} = \text{MAX}, V_I = 7.0\text{V}$                                                 |                        |        |                  | 100  | $\mu\text{A}$ |
| $I_{IH}$ | High-level input current                  |           | $V_{CC} = \text{MAX}, V_I = 2.7\text{V}$                                                 |                        |        |                  | 20   | $\mu\text{A}$ |
| $I_{IL}$ | Low-level input current                   |           | $V_{CC} = \text{MAX}, V_I = 0.5\text{V}$                                                 |                        |        |                  | -0.6 | mA            |
| $I_{OS}$ | Short-circuit output current <sup>3</sup> |           | $V_{CC} = \text{MAX}$                                                                    |                        | -60    |                  | -150 | mA            |
| $I_{CC}$ | Supply current (total)                    | $I_{CCH}$ | $V_{CC} = \text{MAX}$                                                                    | $V_{IN} = \text{GND}$  |        | 1.9              | 2.8  | mA            |
|          |                                           | $I_{CCL}$ | $V_{CC} = \text{MAX}$                                                                    | $V_{IN} = 4.5\text{V}$ |        | 6.8              | 10.2 | mA            |

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{amb} = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

Quad 2-input NAND gate

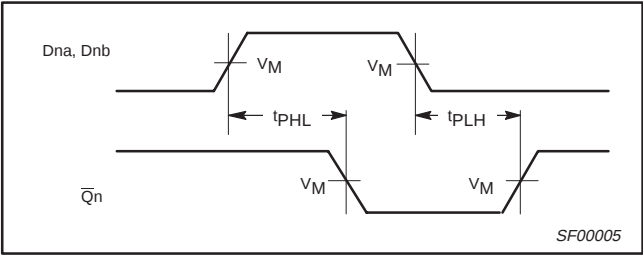
74F00

AC ELECTRICAL CHARACTERISTICS

| SYMBOL                               | PARAMETER                           | TEST<br>CONDITION | LIMITS                                                                                              |            |            |                                                                                                                  |            |                                                                                                                    |            |    | UNIT |
|--------------------------------------|-------------------------------------|-------------------|-----------------------------------------------------------------------------------------------------|------------|------------|------------------------------------------------------------------------------------------------------------------|------------|--------------------------------------------------------------------------------------------------------------------|------------|----|------|
|                                      |                                     |                   | V <sub>CC</sub> = +5.0V<br>T <sub>amb</sub> = +25°C<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |            |            | V <sub>CC</sub> = +5.0V ± 10%<br>T <sub>amb</sub> = 0°C to +70°C<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |            | V <sub>CC</sub> = +5.0V ± 10%<br>T <sub>amb</sub> = −40°C to +85°C<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |            |    |      |
|                                      |                                     |                   | MIN                                                                                                 | TYP        | MAX        | MIN                                                                                                              | MAX        | MIN                                                                                                                | MAX        |    |      |
|                                      |                                     |                   |                                                                                                     |            |            |                                                                                                                  |            |                                                                                                                    |            |    |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>Dna, Dnb to Qn | Waveform 1        | 2.4<br>2.0                                                                                          | 3.7<br>3.2 | 5.0<br>4.3 | 2.4<br>2.0                                                                                                       | 6.0<br>5.3 | 2.0<br>1.5                                                                                                         | 6.5<br>6.0 | ns |      |

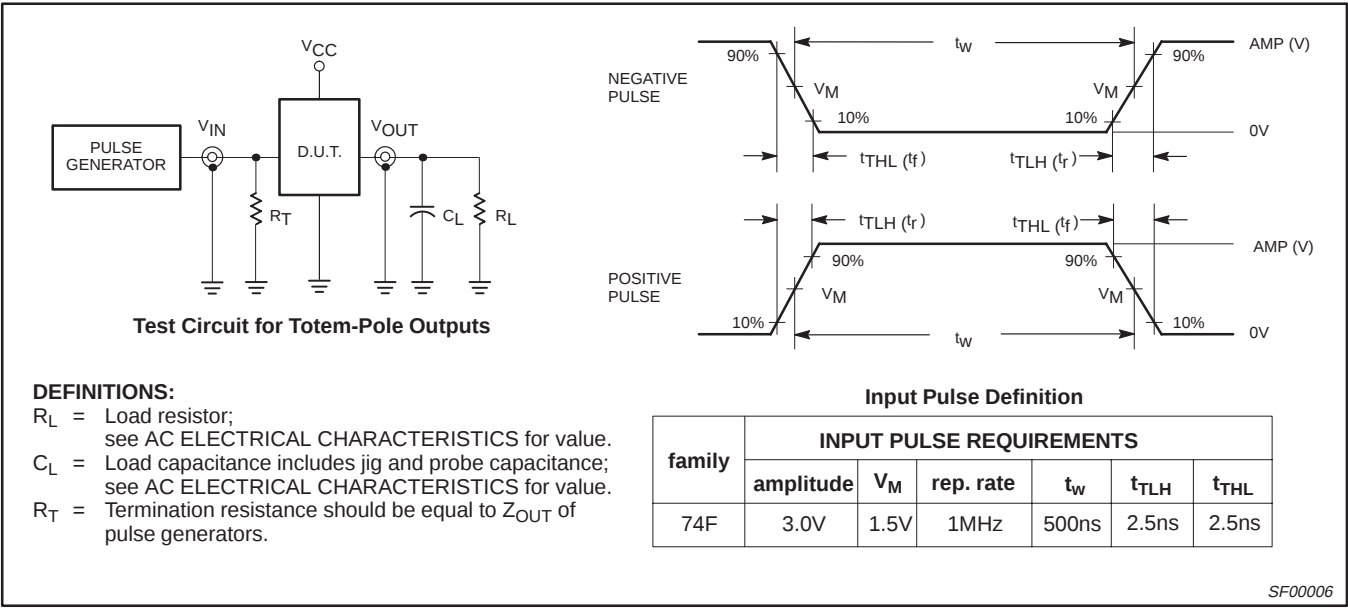
AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$ .



Waveform 1. Propagation delay for inverting outputs

TEST CIRCUIT AND WAVEFORM

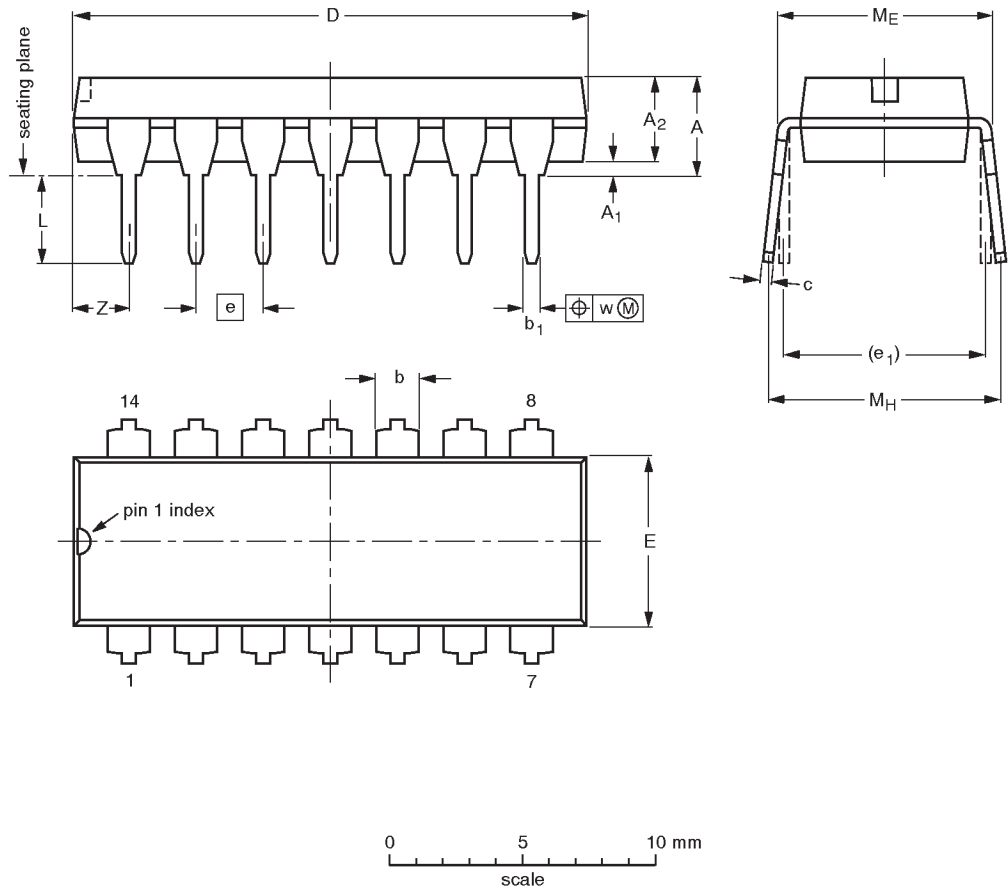


Quad 2-input NAND gate

74F00

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A<br>max. | A <sub>1</sub><br>min. | A <sub>2</sub><br>max. | b              | b <sub>1</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>1</sub> | L            | M <sub>E</sub> | M <sub>H</sub> | w     | Z <sup>(1)</sup><br>max. |
|--------|-----------|------------------------|------------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|--------------------------|
| mm     | 4.2       | 0.51                   | 3.2                    | 1.73<br>1.13   | 0.53<br>0.38   | 0.36<br>0.23   | 19.50<br>18.55   | 6.48<br>6.20     | 2.54 | 7.62           | 3.60<br>3.05 | 8.25<br>7.80   | 10.0<br>8.3    | 0.254 | 2.2                      |
| inches | 0.17      | 0.020                  | 0.13                   | 0.068<br>0.044 | 0.021<br>0.015 | 0.014<br>0.009 | 0.77<br>0.73     | 0.26<br>0.24     | 0.10 | 0.30           | 0.14<br>0.12 | 0.32<br>0.31   | 0.39<br>0.33   | 0.01  | 0.087                    |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

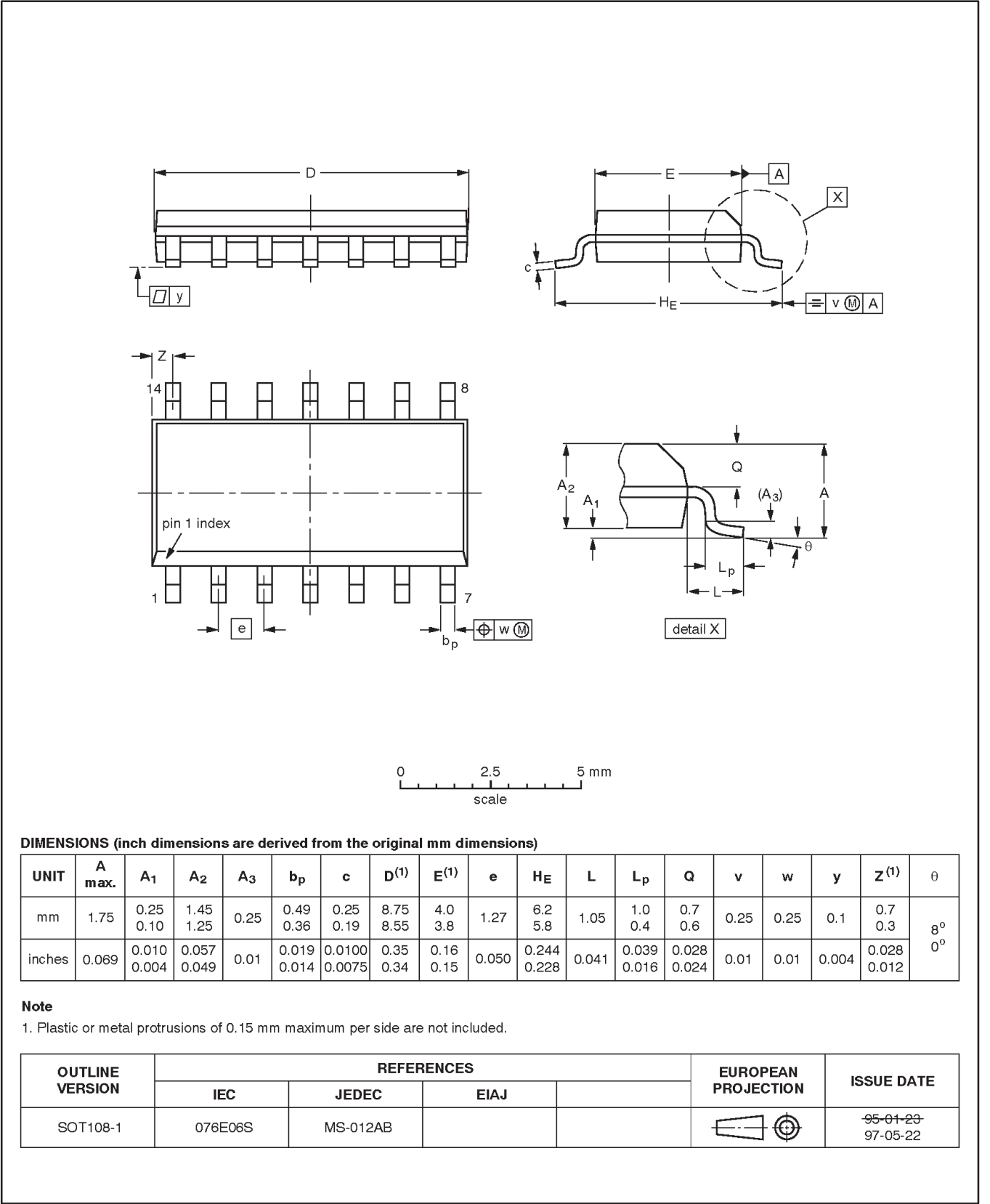
| OUTLINE<br>VERSION | REFERENCES |          |      |  | EUROPEAN<br>PROJECTION | ISSUE DATE           |
|--------------------|------------|----------|------|--|------------------------|----------------------|
|                    | IEC        | JEDEC    | EIAJ |  |                        |                      |
| SOT27-1            | 050G04     | MO-001AA |      |  |                        | 92-11-17<br>95-03-11 |

Quad 2-input NAND gate

74F00

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



|                        |       |
|------------------------|-------|
| Quad 2-input NAND gate | 74F00 |
|------------------------|-------|

NOTES

## Quad 2-input NAND gate

74F00

## Data sheet status

| Data sheet status         | Product status | Definition [1]                                                                                                                                                                                                                                             |
|---------------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Objective specification   | Development    | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.                                                                                                          |
| Preliminary specification | Qualification  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification     | Production     | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.                                                       |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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