CBT3251

1-of-8 FET multiplexer/demultiplexer

Rev. 5 — 18 April 2024 Product data sheet

1. General description

The CBT3251 is a single-pole, 8-throw bus switch. The device features an output enable input ($\overline{OE}$) and three select inputs (S0, S1 and S2). When $\overline{OE}$ is LOW the switch is enabled and the select inputs can be used to connect the A terminal to one of the eight B terminals.

2. Features and benefits

- 5 Ω switch connection between two ports
- Direct interface with TTL levels
- Overvoltage tolerant control inputs to 5.5 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Minimal propagation delay through the switch
- Latch-up protection exceeds 100 mA per JEDEC standard JESD78 class II level A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
CBT3251D	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
CBT3251PW	-40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

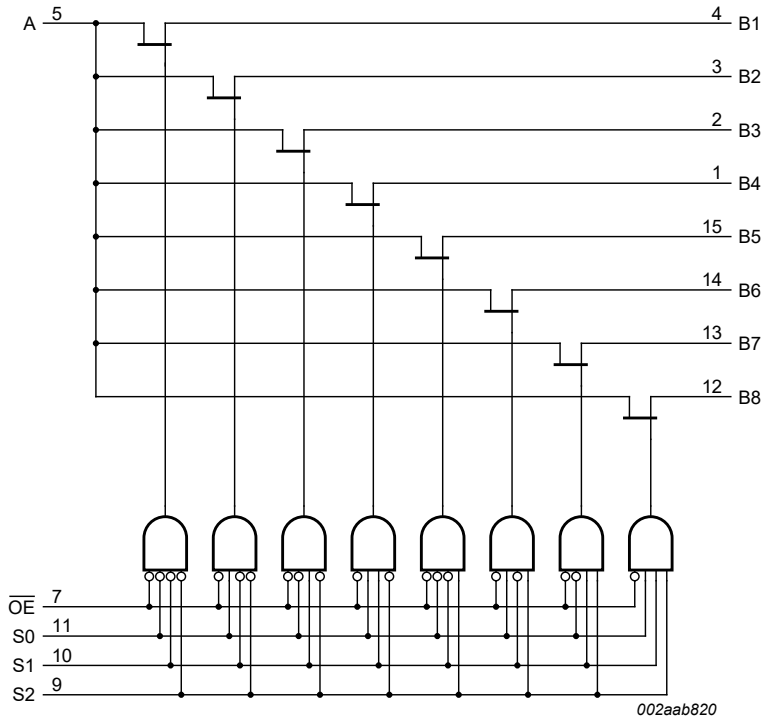
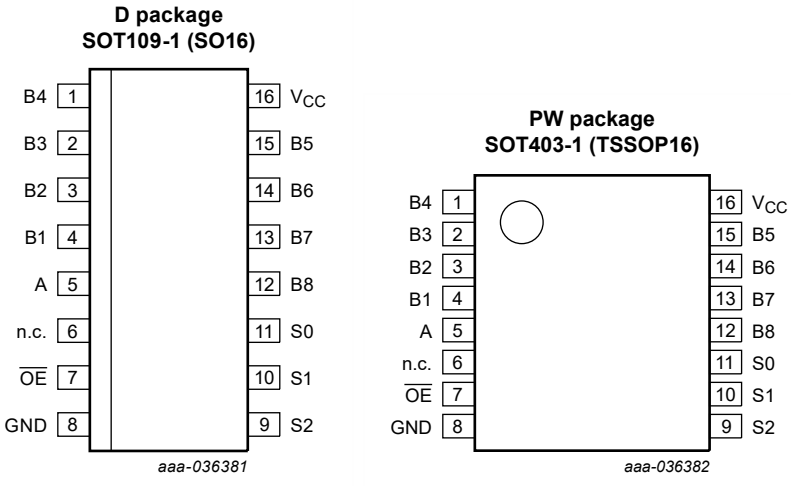


Fig. 1. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
B1, B2, B3, B4, B5, B6, B7, B8	1, 2, 3, 4, 12, 13, 14, 15	B outputs/inputs
A	5	A input/output
n.c.	6	not connected
$\overline{OE}$	7	output enable (active LOW)
S2, S1, S0	9, 10, 11	select control input
GND	8	ground (0 V)
V_{CC}	16	positive supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Inputs				Switch
$\overline{OE}$	S2	S1	S0	
L	L	L	L	A to B1
L	L	L	H	A to B2
L	L	H	L	A to B3
L	L	H	H	A to B4
L	H	L	L	A to B5
L	H	L	H	A to B6
L	H	H	L	A to B7
L	H	H	H	A to B8
H	X	X	X	switch off

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[1]	-0.5	+7.0	V
I_{SW}	switch current	continuous current through each switch	-	128	mA
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.5	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	V
V_{IL}	LOW-level input voltage		-	0.8	V
T_{amb}	ambient temperature	operating in free-air	-40	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C.			Unit
			Min	Typ	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_I = -18 mA	-	-	-1.2	V
V_{pass}	pass voltage	$V_I = V_{CC}$ = 5.0 V; I_O = -100 µA [1]	3.6	3.9	4.2	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	-	-	±1	µA
I_{CC}	supply current	V_{CC} = 5.5 V; I_O = 0 mA; $V_I = V_{CC}$ or GND	-	-	3	µA
ΔI_{CC}	additional supply current	per input; V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND [2]	-	-	2.5	mA
C_I	input capacitance	control pins; V_I = 3 V or 0 V [1]	-	3.5	-	pF
$C_{io(off)}$	off-state input/output capacitance	A port; V_O = 3 V or 0 V; $\overline{OE} = V_{CC}$ [1]	-	17.5	-	pF
		B port; V_O = 3 V or 0 V; $\overline{OE} = V_{CC}$ [1]	-	4.0	-	pF
R_{ON}	ON resistance	V_{CC} = 4.5 V [3]				
		V_I = 0 V; I_I = 64 mA [1]	-	5	7	Ω
		V_I = 0 V; I_I = 30 mA [1]	-	5	7	Ω
		V_I = 2.4 V; I_I = -15 mA [1]	-	10	15	Ω

[1] Typical value is measured at V_{CC} = 5 V; T_{amb} = 25 °C.
[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
[3] Measured by the voltage drop between the A and the Bn terminals at the indicated current through the switch. The lowest voltage of the two (A or Bn) terminals determines the ON resistance.

10. Dynamic characteristics

Table 7. Dynamic characteristics

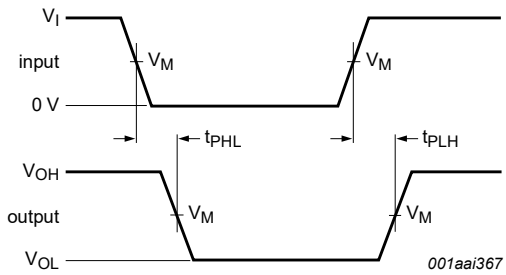
V_{CC} = 4.5 V to 5.5 V; for test circuit, see Fig. 4.

Symbol	Parameter	Conditions		T_{amb} = -40 °C to +85 °C		Unit
				Min	Max	
t_{pd}	propagation delay	A to Bn or Bn to A; see Fig. 2	[1] [2]	-	0.25	ns
		Sn to A; see Fig. 2	[1] [2]	1.5	5.5	ns
t_{en}	enable time	$\overline{OE}$ to A or Bn; see Fig. 3	[2]	1.5	5.6	ns
		Sn to Bn; see Fig. 3	[2]	1.6	5.8	ns
t_{dis}	disable time	$\overline{OE}$ to A or Bn; see Fig. 3	[2]	1.9	6.4	ns
		Sn to Bn; see Fig. 3	[2]	2.3	6.2	ns

[1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] t_{PLH} and t_{PHL} are the same as t_{pd}.
t_{PZL} and t_{PZH} are the same as t_{en}.
t_{PLZ} and t_{PHZ} are the same as t_{dis}.

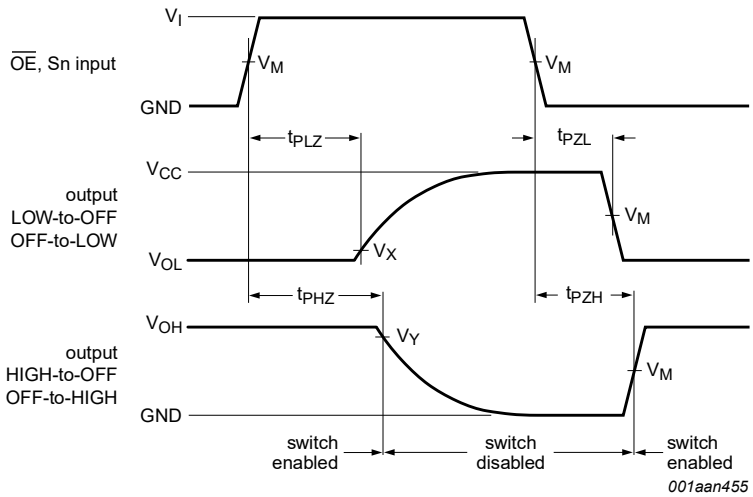
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 2. The input (A; Bn) to output (Bn; A) or input (Sn) to output (A) propagation delay times



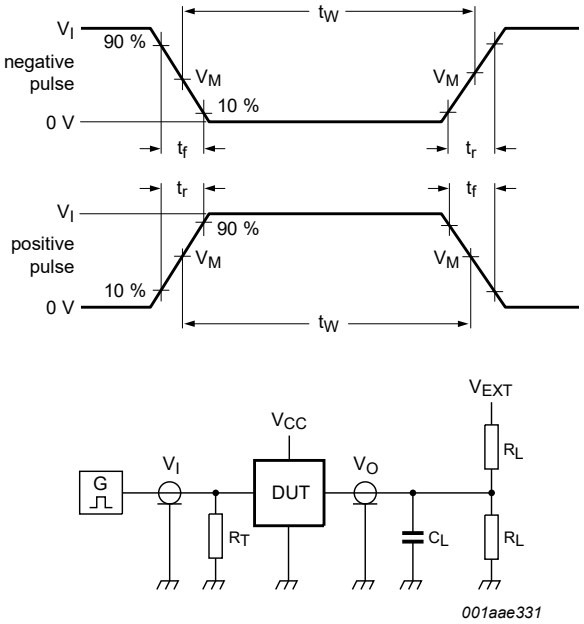
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 3. Enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
4.5 V to 5.5 V	GND to 3.0 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

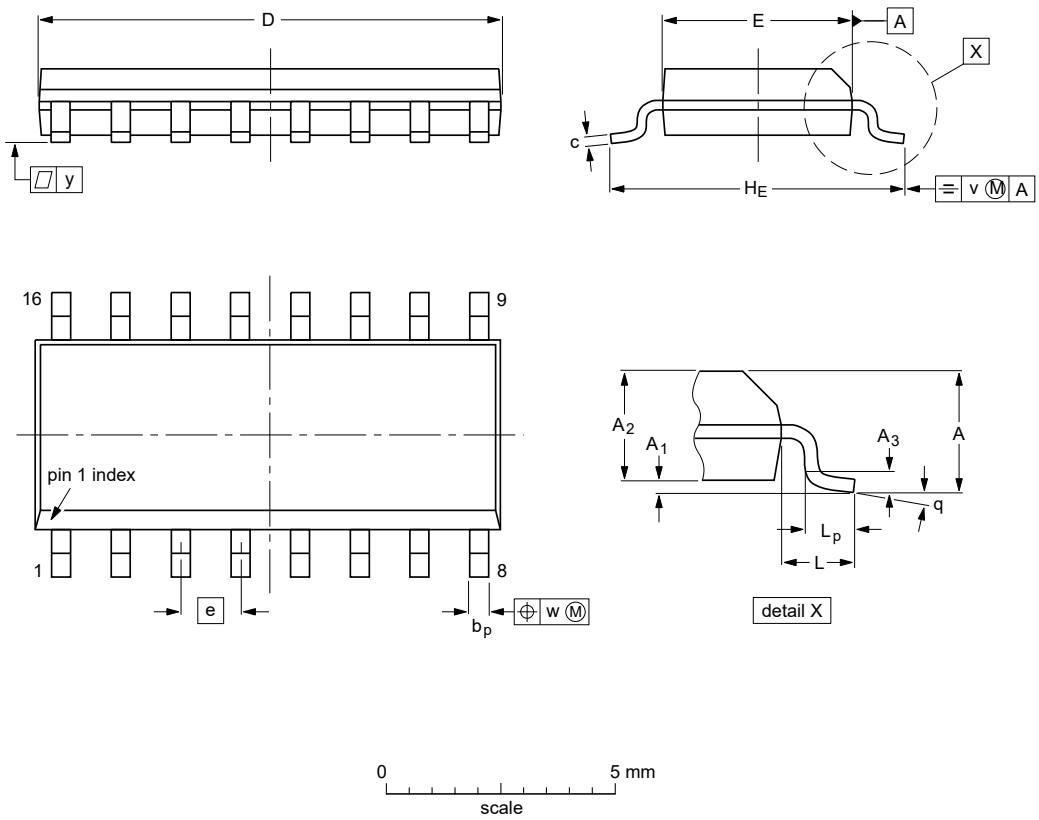
Fig. 4. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
4.5 V to 5.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

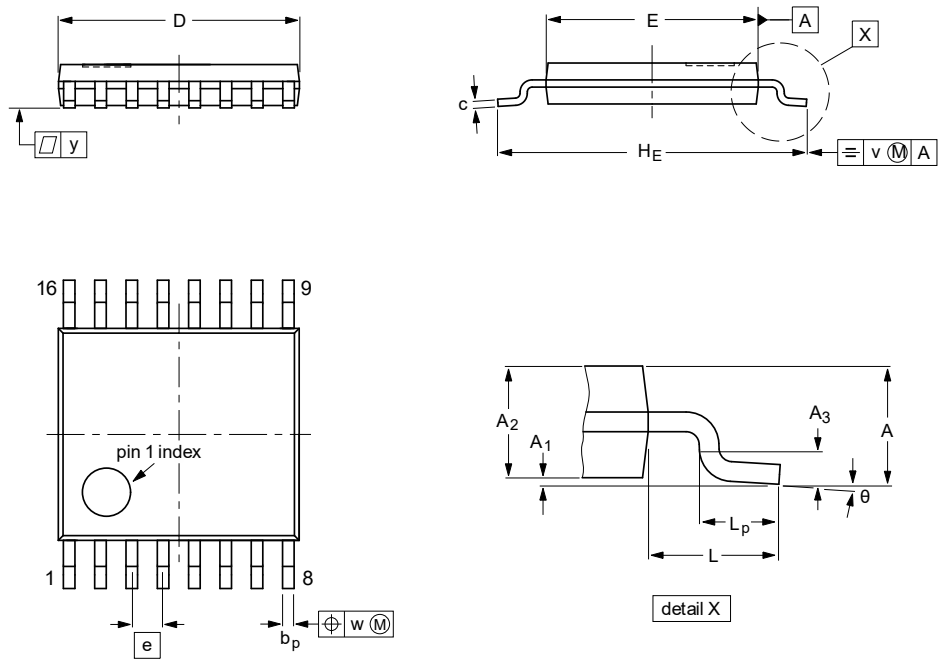
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

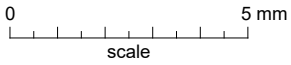
sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 5. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 6. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3251 v.5	20240418	Product data sheet	-	CBT3251 v.4
Modifications:	• Fig. 5, Fig. 6: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard. • Section 9: R_{ON} specification updated in line with CBT family.			
CBT3251 v.4	20210324	Product data sheet	-	CBT3251 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Type number CBT3251DB (SOT338-1 / SSOP16) removed.			
CBT3251 v.3	20160316	Product data sheet	-	CBT3251 v.2
Modifications:	• Type number CBT3251DS removed			
CBT3251 v.2	20130916	Product data sheet	-	CBT3251 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 6 pass voltage modified.			
CBT3251 v.1	20051221	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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