Identification ROM

Description

The V4082 is a 64-bit read only memory (ROM) which contains a unique laser engraved serial number. The data in the ROM is partitioned into three sections: An 8-bit identifier code, a 48-bit serial number and an 8-bit cyclical redundancy check (CRC). The serial number is incremented in fabrication such that no two parts have the same code. Communication for reading and writing is done serially via a single data lead (and ground return) using a single wire protocol. Power for reading is derived from the data line itself with no need for an extra power source. The circuit is available in SOT 223 or TO 92 package.

Features

- Unique 48-bit silicon serial number gives 10^{14} combinations
- Factory lasered and tested, no two parts alike
- 8-bit cyclic redundancy check ensures error-free reading
- Presence detect indicates to the system when first contact is made
- Zero standby power required
- Custom serial numbers available
- Pin compatible with DS 2400, DS 2401 in TO-92 and SOT-223

Applications

- Socket identification
- PCB identification
- Equipment registration

Typical Operating Configuration

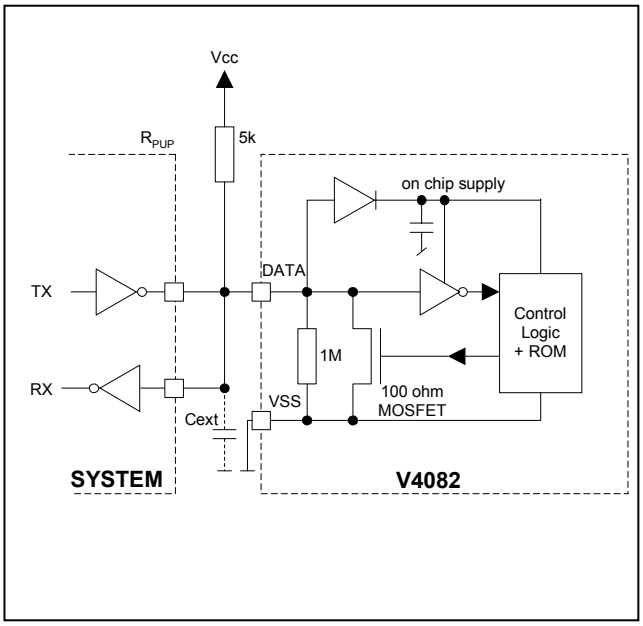
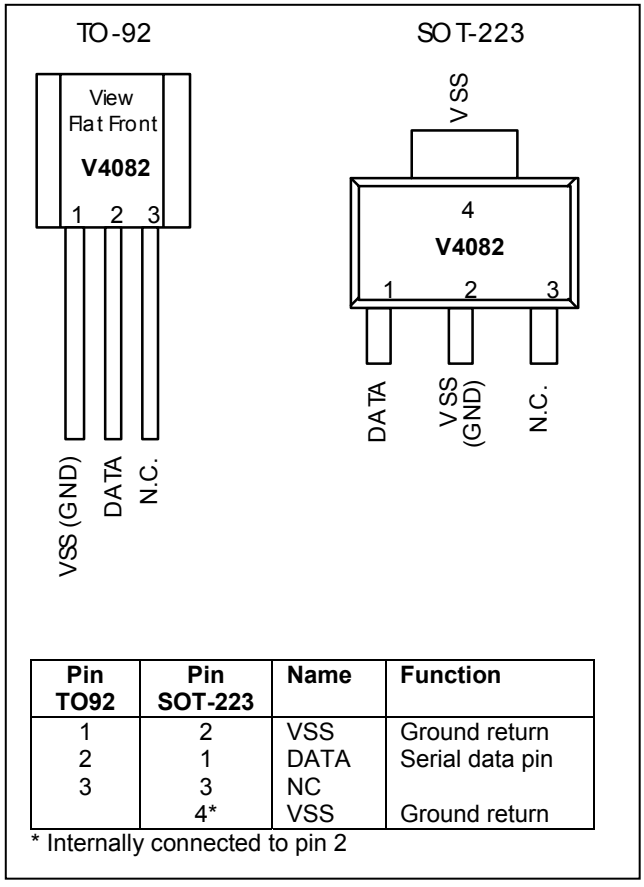


Fig. 1

Pin Assignment



Pin TO92	Pin SOT-223	Name	Function
1	2	VSS	Ground return
2	1	DATA	Serial data pin
3	3	NC	
	4*	VSS	Ground return

* Internally connected to pin 2

Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage on Data Pin vs V_{SS}	V_{DATA}	-0.5 to 7.0V
Max. injected current into DATA pin	Idata	-20 to +20 mA
Storage Temperature	T_{STD}	-55 to +125 °C
Power Dissipation	Pw	10 mW

Table 1

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
External pull up voltage	V_{CC}	4.5	5.0	5.5	V
External pull up resistance	R_{PUP}		5		kΩ
External capacitance	Cext			800	pF
Operating temperature	T_A	-40	25	+85	°C

Table 2

Electrical Characteristics

Unless otherwise specified: All voltages are referenced to V_{SS}, V_{DD}= 5.0V, T_A=-40 to +85°C.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC Characteristics						
Data Input Logic Low	VIL		-0.2		0.4	V
Data Input Logic High	VIH		2.2		V_{CC}	V
Sink Current	IL	VOUT = 0.4V	4.0			mA
Output Logic Low	VOL	I = 4mA			0.4	V
Output Logic High	VOH				V_{CC}*	V
Input Resistance	RIN	Modulator FET off		1.2		MΩ
Operating Charge (after supply diode)	COP	Modulator FET on, 72 time slots			30	nC
Current consumption	Idata	Modulator FET off			16	µA

* Depends on resistive divider RIN / (RPUP+RIN)

Table 3

Timing Characteristics

Unless otherwise specified: V_{DD}= 5.0V ±10%, T_A=-40 to +85°C cf. remarks under "Effect of C_{ext}"

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Time Slot Period	TSLOT		60		120	µs
Write 1 Low Time	TLOW1		1		15	µs
Write 0 Low Time	TLOW0		60		120	µs
Read Data Valid	TRDV				15	µs
Read Data Setup	TSU		1			µs
Frame Sync	TSYC		1			µs
Reset Low Time	TRSTL		480			µs
Reset High Time	TRSTH		480			µs
Presence Detect High	TPDH		5		50	µs
Presence Detect Low	TPDL		60		240	µs

Table 4

Timing Waveforms

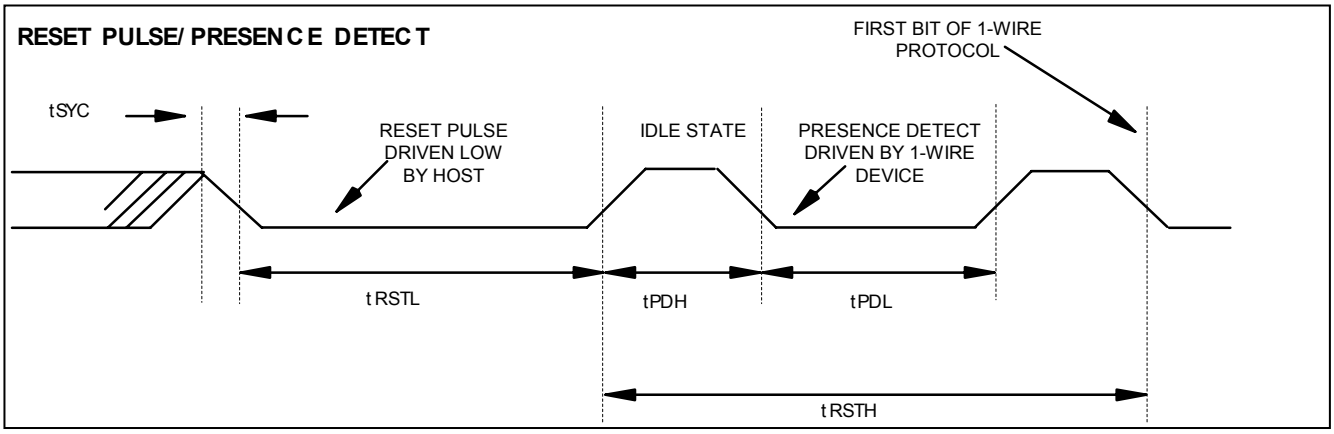


Fig. 3

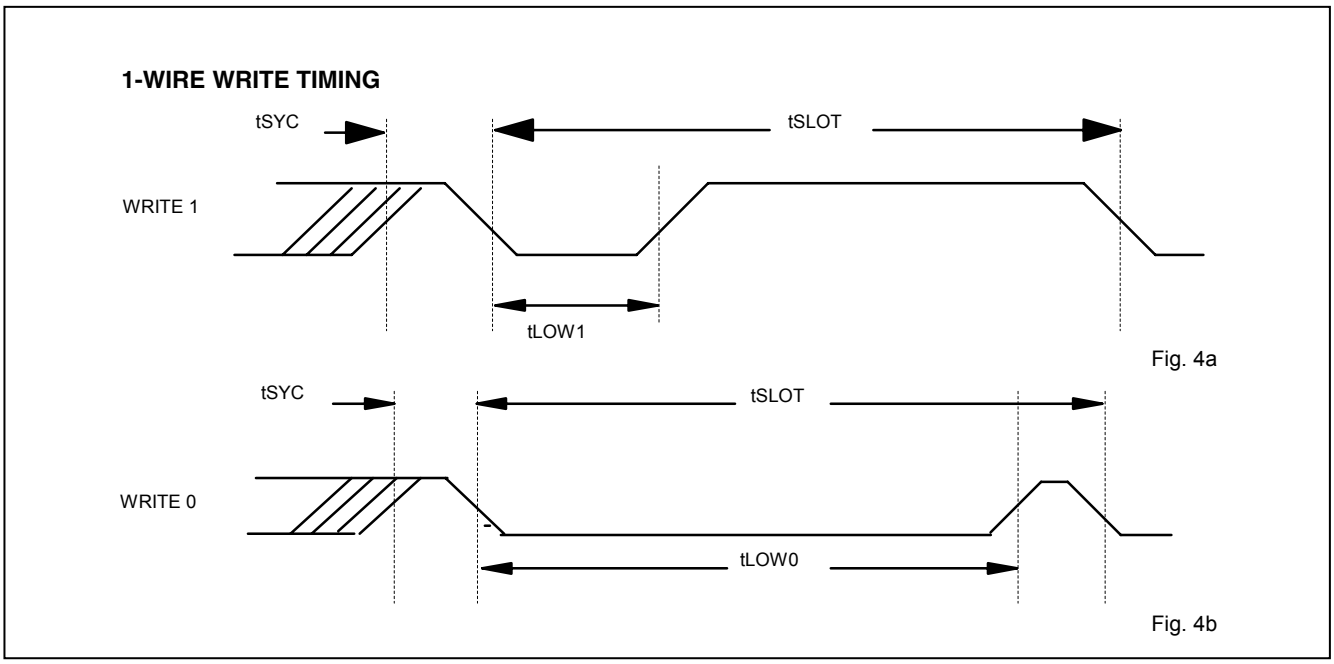


Fig. 4a

Fig. 4b

1-WIRE READ TIMING

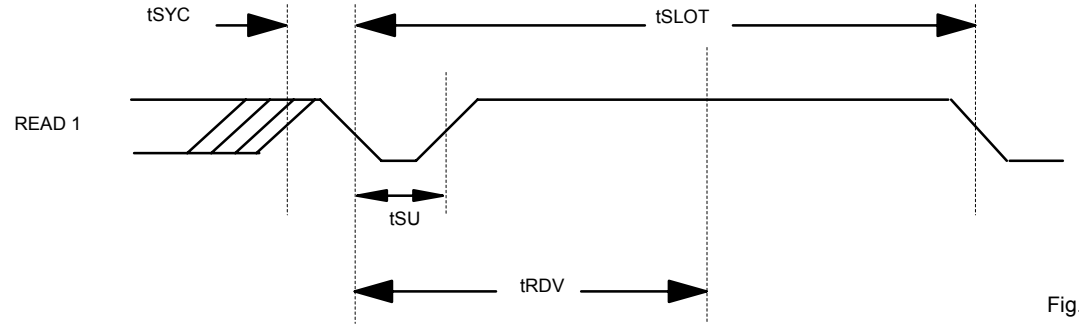


Fig. 5a

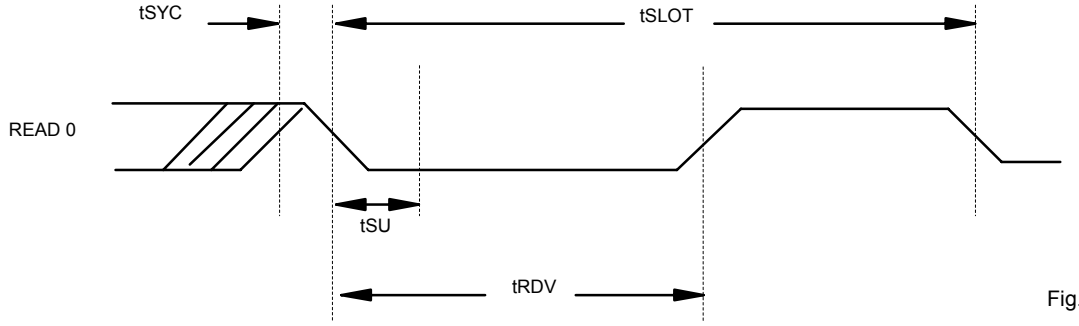


Fig. 5b

1-WIRE PROTOCOL

State 1: RESET (from System)

↓

State 2: COMMAND WORD (from System)

↓

State 3: TYPE IDENTIFIER (to System)

↓

State 4: SERIAL NUMBER AND CRC (to System and CRC Value)

Fig. 6

Functional Description

The V4082 is a 64-bit read only memory (ROM) which contains a unique laser engraved serial number, the data in the ROM is partitioned into three sections: an 8-bit type identifier code, a 48-bit serial number and an 8-bit cyclical redundancy check (CRC). A signal interface lead provides communication for reading and writing. Power for reading is derived from the data line itself with no need for an external power source. The circuit is available in SOT 223 or TO-92 package.

Operation

All communication to and from the V4082 Silicon Serial Number is accomplished via a single interface lead. Data contained within the V4082 is accessed through the use of time slots and a single wire protocol. Power to the part is derived from the high going pulse at the beginning of a write or read time slot.

Write time slots

A write time slot is initiated when the system pulls the data line from a high logic level to a low logic level. There are two types of write time slots: write one and write zero. All write slots must be a minimum of 60 microseconds and a maximum of 120 microseconds in duration with a minimum of a 1 microsecond syncpulse between individual write cycles.

For the system to generate a write one time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot (see Figure 4a).

For the system to generate a write zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot (see Figure 4b).

Read time slots

The system generates read time slots when data is to be read from the V4082. A read time slot is initiated when the system pulls the data line from a logic high level to a logic low level. The data line must remain at a low logic level for a minimum of 1 microsecond and a maximum of 15 microseconds. This maximum time of 15 microseconds includes the time required for the data line to pull up to a high level after it is released. The state of the V4082 data must be read by the system within 15 microseconds after the start of the read time slot. After this time, the state of the data is not guaranteed (see Figure 5). All read time slots must be a minimum of 1 microsecond syncpulse between individual read time slots.

Single wire protocol

To communicate with the V4082 a specific protocol is utilized. The single wire protocol consists of four separate states which are used to reset the device, issue a command word, read the type identifier number and read the unique silicon serial number and CRC byte (see Figure 4).

To initially set the V4082 into a known state, a reset pulse must be sent to it. The reset pulse is a logic low generated by the system which must remain low for a minimum of 480 microseconds and then be followed by a 480 microsecond logic high level (see Figure 3). During these 480 microsecond high time the V4082 will assert a presence detect signal. This signal is generated by the V4082 and consists of a logic low level which is held for a maximum of 240 microseconds and minimum of 60 microseconds. This signal can be used to detect that a V4082 is attached to the single wire interface after the issuance of a reset command.

Once the V4082 has been set into a known state, the command word is transmitted to the V4082 with eight write time slots. LSB first. The command word for the V4082 is a hexadecimal 0Fh.

Upon recognition of the command word, the V4082 is ready to respond with its data. The data in the ROM is partitioned into three sections: an 8-bit identifier code, a 48-bit serial number and an 8-bit CRC. The type identifier code for the V4082 is 81h. The 48-bit serial number in each V4082 is unique. The single wire CRC algorithm calculates an 8-bit CRC, from the type identifier code and the serial number (56 bits) and generates an 8-bit value. This value is lasered into the part at the time of manufacture. To terminate a read operation: either give 64 read time slots or issue a reset sequence.

CRC generation

To validate that the transmitted data from the V4082 has been received correctly by the system, a comparison of the system-generated CRC and the received V4082 CRC must be made. If the two CRC values match, the transmission was error-free.

The equivalent polynomial function of the CRC is: CRC = $x^8 + x^5 + x^4 + 1$

Recommended system interface

The system must have an open drain driver with a pull up resistor of approximately 5KΩ to VCC on the data signal line. The V4082 has an internal open drain driver with a 1.2MΩ pulldown resistor to ground. The pulldown resistor holds the data input pin at ground potential when the V4082 is not connected to a single wire interface. To avoid unnecessary current consumption, VCC may either be disconnected or pulled to ground when the V4082 is not used.

Effect of Cext

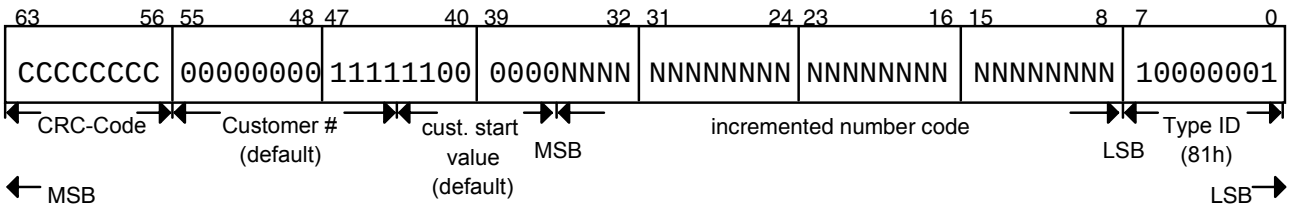
Any capacitance on the data pin forms a time constant together with the external pull-up resistor RPUP or the pull-down resistances of either the external open-drain driver or the modulator FET of the V4082. The pull-up time constant TPUP = RPUP*Cext is normally the most critical one. Please note that all timing parameters as given in Table 4 are with respect to the Data Input Logic Thresholds VIL and VIH. In the case of read operation, the VIH of the external master circuit (RX input) has to be taken into account. Cext has to be kept sufficiently low to allow the pulling-up of the DATA pin to VIH of the master circuit before the Read Data Valid Time (TRDV) in case of a Read 1. For the very first pulling-up of the data pin, i.e. after a reset pulse, the on-chip supply buffer capacitance (approx. 500 pF) has to be considered as well. Later on this capacitance has less influence on the operation, the on-chip supply is well above the VIH level and the on-chip capacitor is decoupled by the diode from the data pin for VDATA voltages lower than the on-chip supply.

Custom V4082

Upon special request, the V4082 is available with portions of the 48-bit serial number defined by the customer. These special parts are designated V4082xxx. The custom 48-bit number has two specific subfields of which EM Microelectronic-Marin will assign a customer IC number in the most significant 12 bits.

The next most significant 8 bits are selectable by the customer as a starting value, and the least significant 28 bits are non-selectable and will increment by one, starting at 0000h. The type identifier code for a custom V4082 is 81h.

The default memory map is as follows (first bit out (LSB) = Bit 0):



Repetitive Read-out of data

If the system generates more read time slots than necessary, the V4082 continues to output the ROM code, restarting from zero address. By issuing a reset sequence, this procedure can be stopped. The V4082 will then again issue a presence detect signal and expect the command word from the system.

Package Information

Dimensions of TO-92 Package

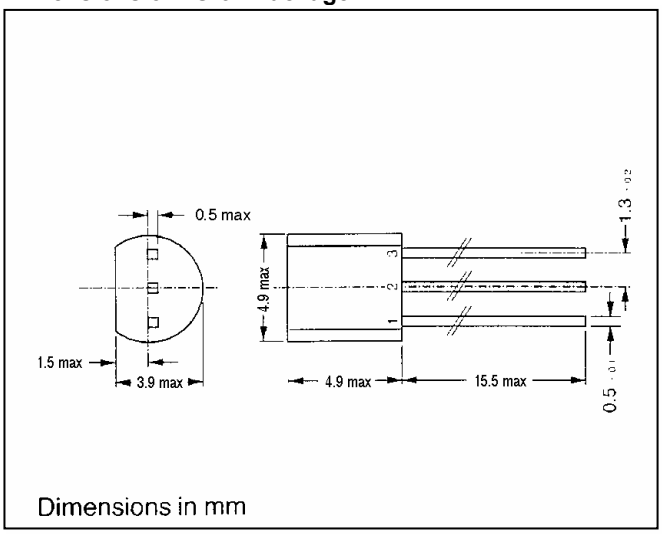


Fig. 7

Dimensions of SOT_223 Package

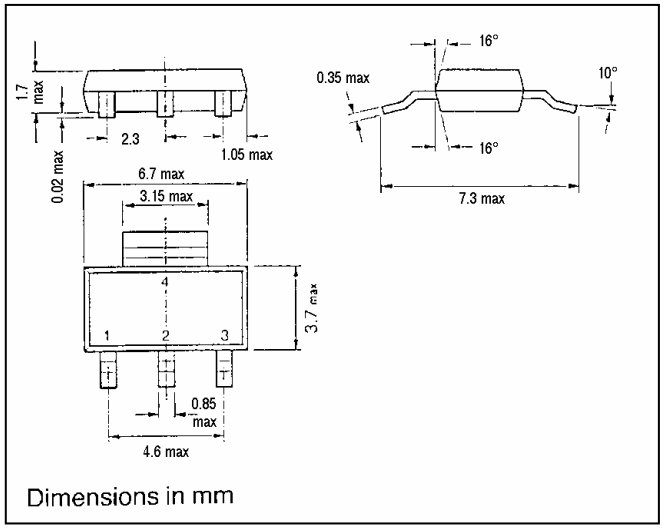


Fig. 8

Ordering Information

When ordering, please specify the complete Part Number below

Part Number	Version	Package	Delivery Form	Package Marking
V4082V1T03E	V01	TO-92	Ammopack	4082 01
V4082V1ST3B		SOT-223	Tape & Reel	4082 01
V4082V2T03E	V02	TO-92	Ammopack	4082 02
V4082V2ST3B		SOT-223	Tape & Reel	4082 02

Note: Version 01 (V01) corresponds to the standard version. Other versions might be available upon request for a minimum order quantity (Please contact EM Microelectronic at http://www.emmicroelectronic.com or info@emmicroelectronic.com)