

Advanced Power MOSFET

IRFR/U120A

FEATURES

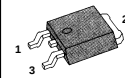
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10 μ A (Max.) @ $V_{DS} = 100V$
- Lower $R_{DS(ON)}$: 0.155 Ω (Typ.)

$$BV_{DSS} = 100 V$$

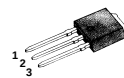
$$R_{DS(on)} = 0.2 \Omega$$

$$I_D = 8.4 A$$

D-PAK



I-PAK



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current ($T_C=25^\circ C$)	8.4	A
	Continuous Drain Current ($T_C=100^\circ C$)	5.3	
I_{DM}	Drain Current-Pulsed ①	34	A
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy ②	141	mJ
I_{AR}	Avalanche Current ①	8.4	A
E_{AR}	Repetitive Avalanche Energy ①	3.2	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.5	V/ns
P_D	Total Power Dissipation ($T_A=25^\circ C$) *	2.5	W
	Total Power Dissipation ($T_C=25^\circ C$)	32	W
	Linear Derating Factor	0.26	W/ $^\circ C$
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	3.9	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient *	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount).

Electrical Characteristics (T_g=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV _{DSS}	Drain-Source Breakdown Voltage	100	--	--	V	V _{GS} =0V, I _D =250 μA
ΔBV/ΔT _J	Breakdown Voltage Temp. Coeff.	--	0.12	--	V/°C	I _D =250 μA See Fig 7
V _{GS(th)}	Gate Threshold Voltage	2.0	--	4.0	V	V _{DS} =5V, I _D =250 μA
I _{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	V _{GS} =20V
	Gate-Source Leakage , Reverse	--	--	-100		V _{GS} =-20V
I _{DSS}	Drain-to-Source Leakage Current	--	--	10	μA	V _{DS} =100V
		--	--	100		V _{DS} =80V, T _C =125°C
R _{DS(on)}	Static Drain-Source On-State Resistance	--	--	0.2	Ω	V _{GS} =10V, I _D =4.2A ④
g _{fs}	Forward Transconductance	--	6.29	--	Ω	V _{DS} =40V, I _D =4.2A ④
C _{iss}	Input Capacitance	--	370	480	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz See Fig 5
C _{oss}	Output Capacitance	--	95	110		
C _{rss}	Reverse Transfer Capacitance	--	38	45		
t _{d(on)}	Turn-On Delay Time	--	14	40	ns	V _{DD} =50V, I _D =9.2A, R _G =18Ω See Fig 13 ④⑤
t _r	Rise Time	--	14	40		
t _{d(off)}	Turn-Off Delay Time	--	36	90		
t _f	Fall Time	--	28	70		
Q _g	Total Gate Charge	--	16	22	nC	V _{DS} =80V, V _{GS} =10V, I _D =9.2A See Fig 6 & Fig 12 ④⑤
Q _{gs}	Gate-Source Charge	--	2.7	--		
Q _{gd}	Gate-Drain("Miller") Charge	--	7.8	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I _S	Continuous Source Current	--	--	8.4	A	Integral reverse pn-diode in the MOSFET
I _{SM}	Pulsed-Source Current ①	--	--	34		
V _{SD}	Diode Forward Voltage ④	--	--	1.5	V	T _J =25°C, I _S =8.4A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	--	98	--	ns	T _J =25°C, I _F =9.2A
Q _{rr}	Reverse Recovery Charge	--	0.34	--	μC	di _F /dt=100A/μs ④

Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② L=3mH, I_{AS}=8.4A, V_{DD}=25V, R_G=27Ω, Starting T_J=25°C
- ③ I_{SD} ≤ 9.2A, di/dt ≤ 300A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J=25°C
- ④ Pulse Test : Pulse Width = 250 μs, Duty Cycle ≤ 2%
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

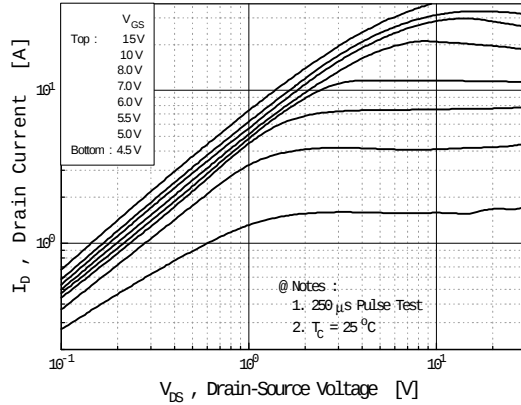


Fig 2. Transfer Characteristics

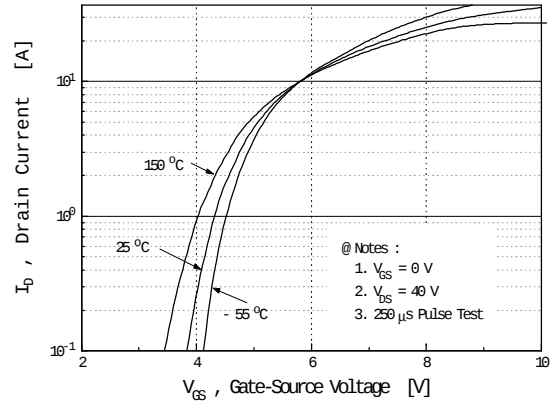


Fig 3. On-Resistance vs. Drain Current

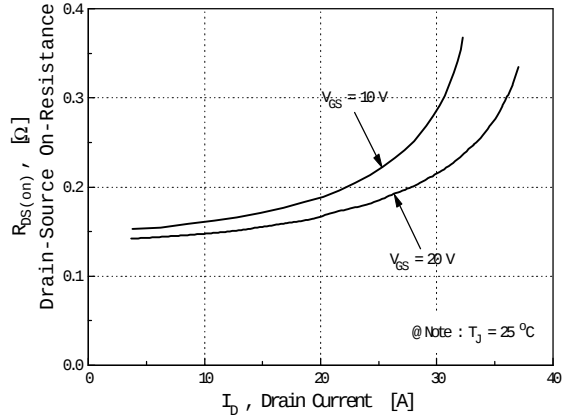


Fig 4. Source-Drain Diode Forward Voltage

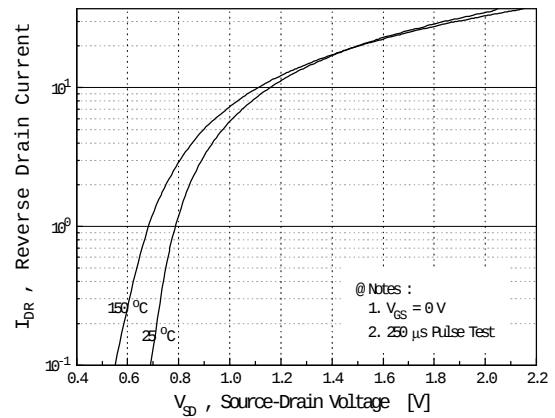


Fig 5. Capacitance vs. Drain-Source Voltage

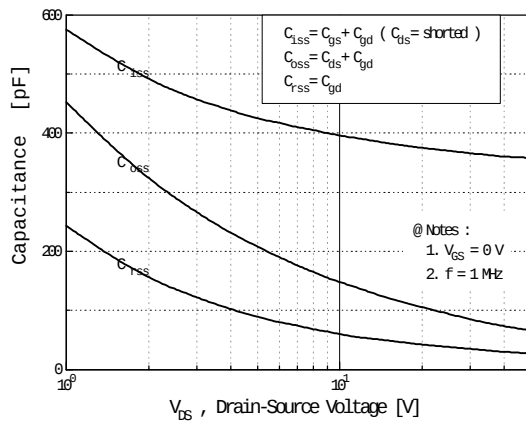
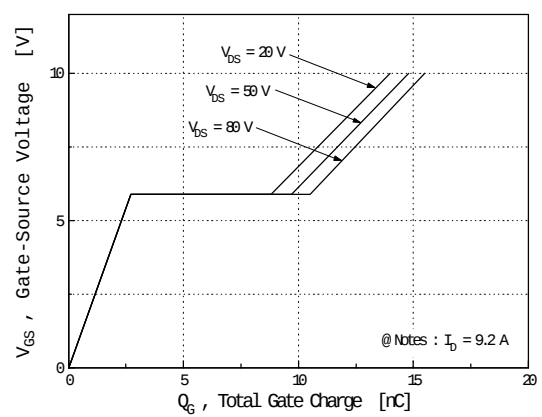


Fig 6. Gate Charge vs. Gate-Source Voltage



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N-CHANNEL POWER MOSFET

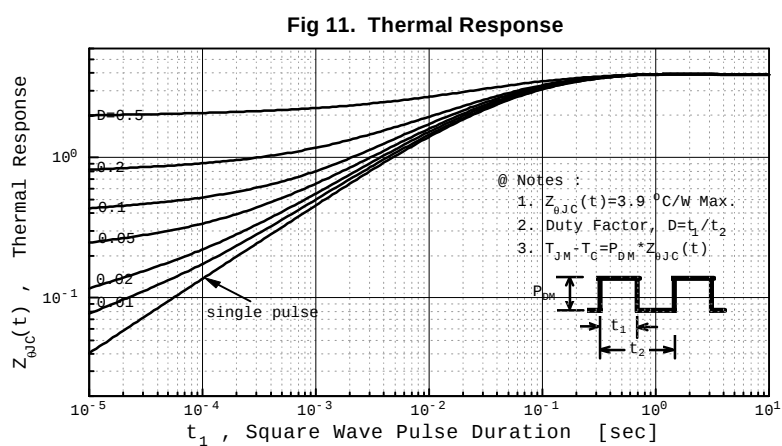
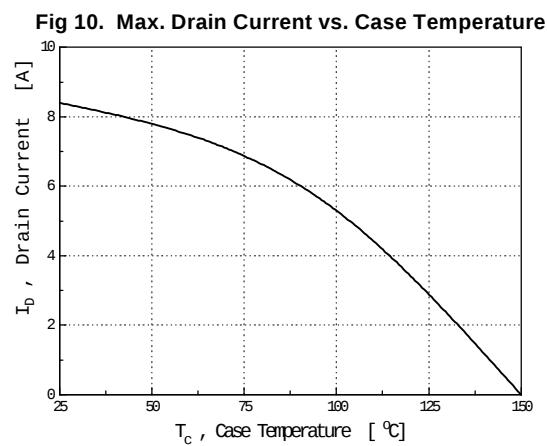
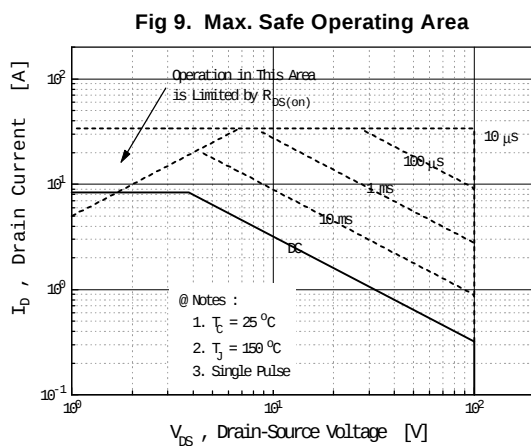
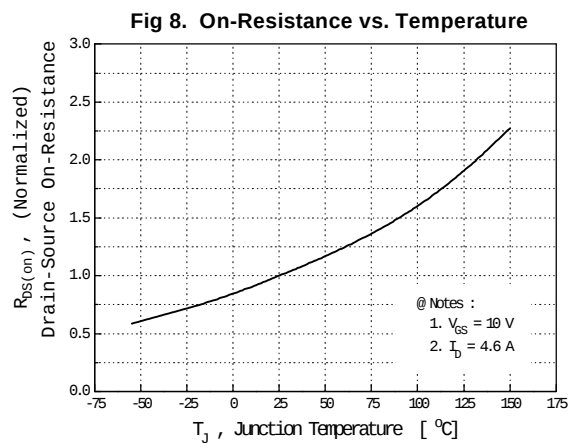
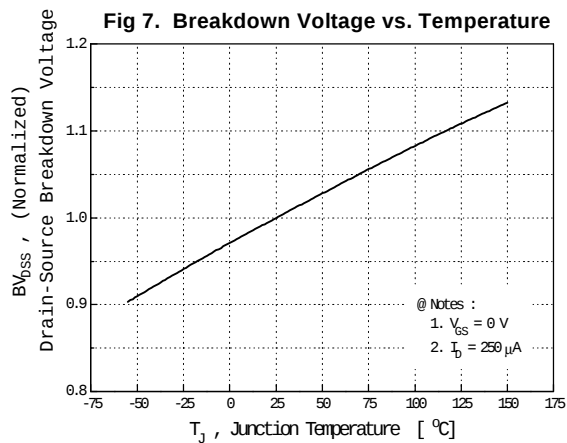


Fig 12. Gate Charge Test Circuit & Waveform

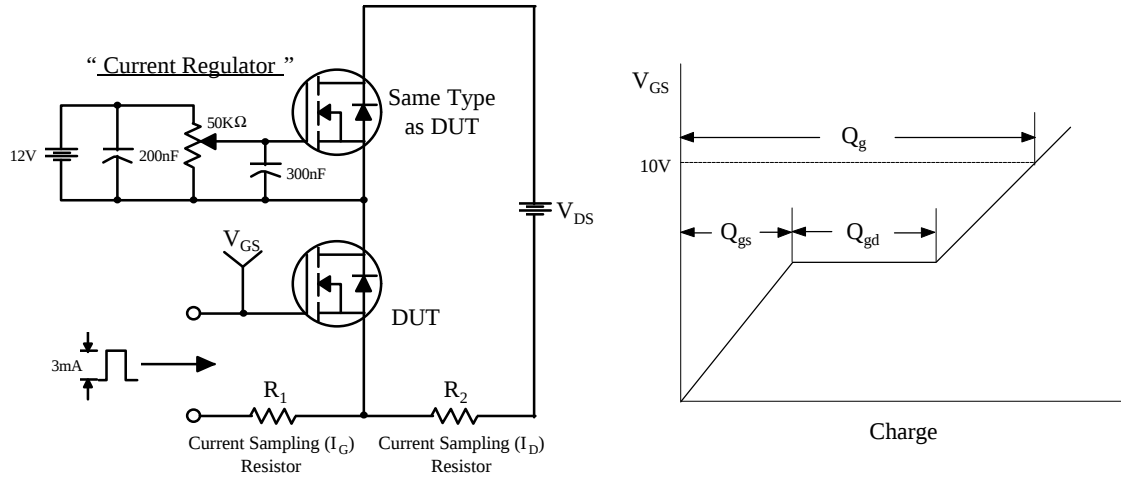


Fig 13. Resistive Switching Test Circuit & Waveforms

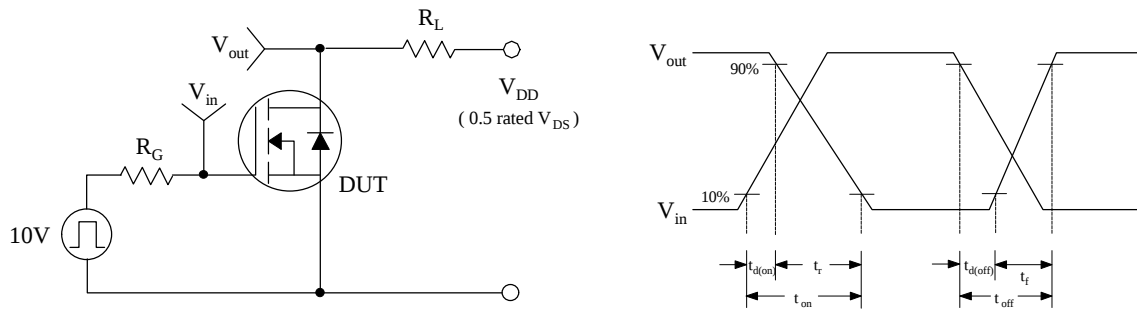


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

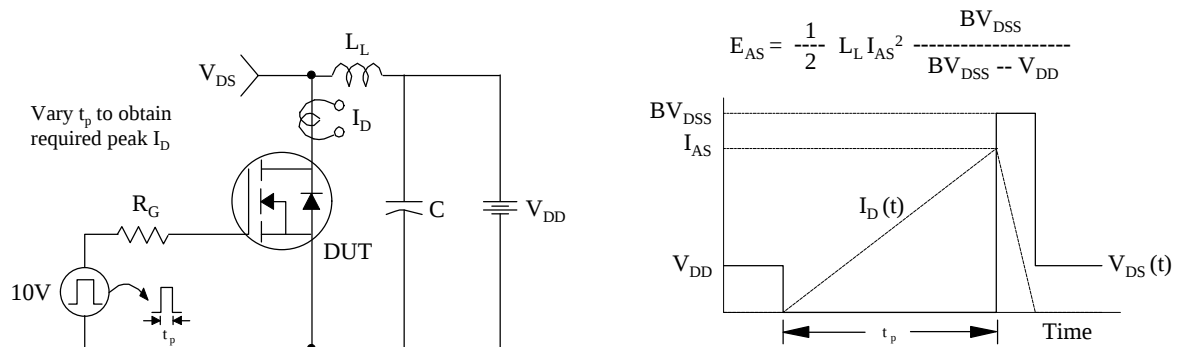
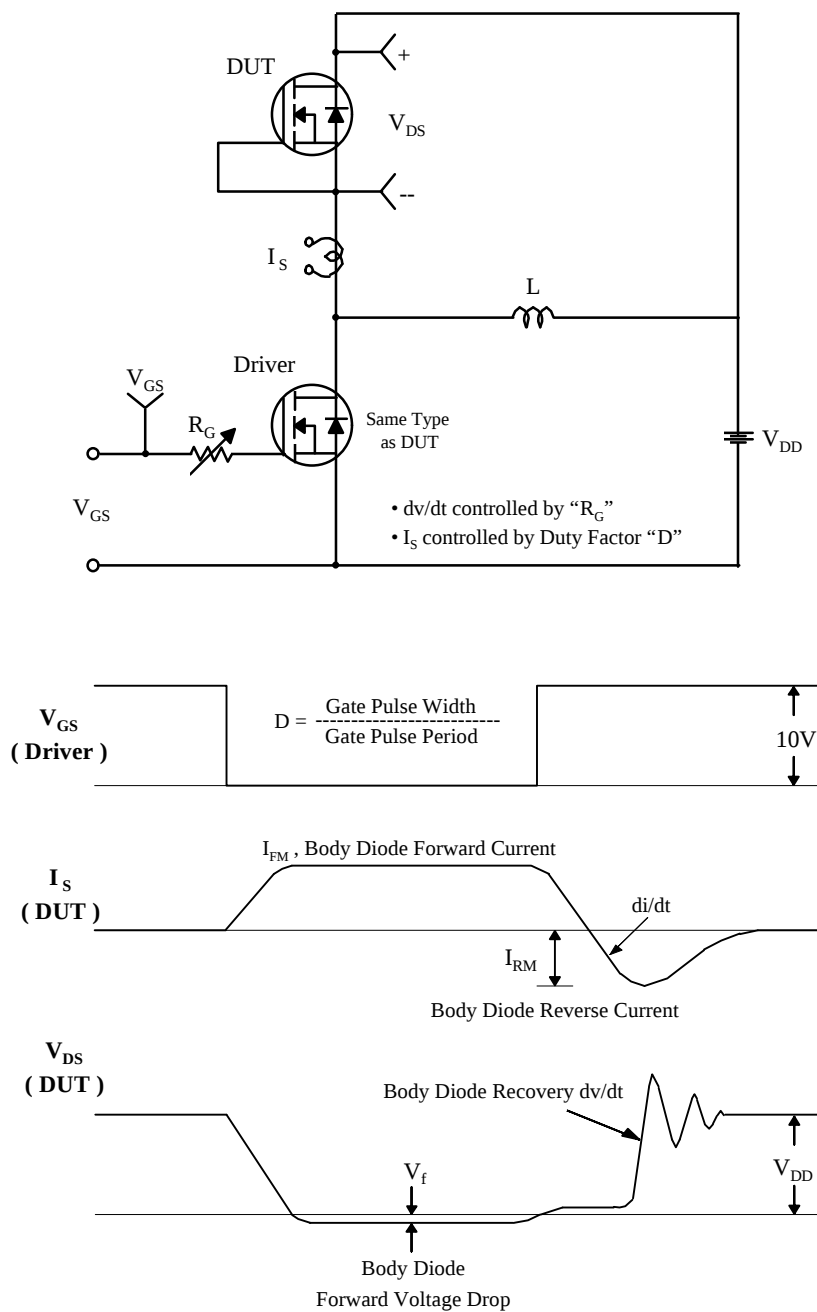


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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