AN-2255 LM3463 Evaluation Board

1 Introduction

The LM3463 is a 6-channel linear LED driver with Dynamic Headroom Control (DHC) designed to drive six strings of high brightness LEDs at maximum supply voltage up to 95V. Each output channel of the LM3463 evaluation board is designed to deliver 200 mA of LED driving current. The LED turn on voltage is set to 48V by default, thus the board is able to deliver up to 57.6W total output power. The six output channels are divided into 4 individual groups to facilitate average LED current control by means of PWM dimming. The PWM dimming control interface of the LM3463 can accept standard TTL level PWM signals, analog voltage or serial data to control the dimming duty of the four LED groups individually. The analog dimming control interface accepts an analog control voltage in the range from 0V to 2.5V to adjust the reference voltage of the linear current regulators, which enables true LED current adjustment. This evaluation board is designed to be connected to an external primary power supply. Using three connection wires, the VIN, GND and VFB, the dynamic Headroom Control (DHC) circuit of the LM3463 adjusts the output voltage of the primary power supply to maximize system efficiency.

2 Standard Settings of the LM3463 Evaluation Board

- Input voltage range: 12V to 95V
- LED turn on voltage: 48V
- Nominal forward voltage of a LED string: 42V
- Output current per ch.: 200 mA
- System clock freq.: 246 kHz
- DHC cut-off freq.: 0.1Hz
- Mode of dimming control: Direct PWM Mode

3 LM3463 Evaluation Board Schematic

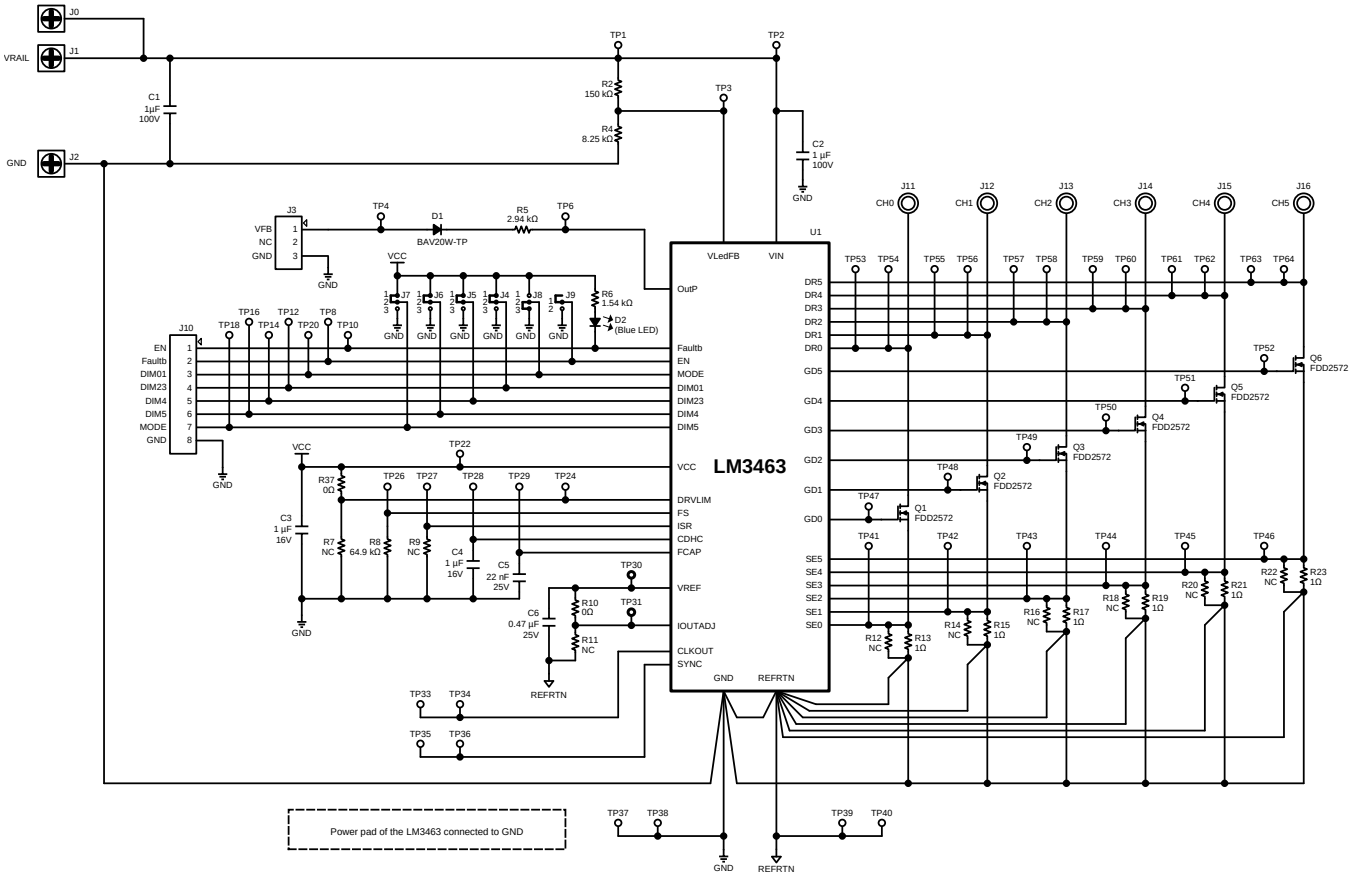

Figure 1. Circuit diagram of the LM3463 evaluation board

4 Bill Of Materials

Designator	Description	Package	Part Number	Manufacturer
U1	LED driver	WQFN-48	LM3463	Texas Instruments
C1, C2	Capacitor, 1uF, 100V, X7R	1206	GRM31CR72A105KA01L	MuRata
C3, C4	Capacitor, 1uF, 16V, X7R	0603	C1608X7R1C105K	TDK
C5	Capacitor, 2200 pF, 25V, X7R	0603	GRM188R71E222KA01D	MuRata
C6	Capacitor, 0.47uF, 25V, X5R	0603	GRM188R61E474KA12D	MuRata
D1	Diode, 200V, 200 mA	SOD-123	BAV20W-TP	Micro Commercial
D2	Green LED	Gull-wing	HLMP-6500-F0011	Avago Technologies
J0, J1, J2	Terminal screw	vertical, snap-in	7693	Keystone
J3	3 Pos. connector	100 mil pitch	3-641216-3	TE Connectivity
J4, J5, J6, J7, J8	3 Pos. header	100 mil pitch	TSW-103-07-G-S	Samtec
J9	2 Pos. header	100 mil pitch	TSW-102-07-G-S	Samtec
J10	8 Pos. connector	100 mil pitch	3-641216-8	TE Connectivity
J11, J12, J13, J14, J15, j16	Banana jack connector	8.9 mm dia.	575-8	Keystone
Q1, Q2, Q3, Q4, Q5, Q6	MOSFET, N-CH, 150V, 29A	DPAK	FDD2572	Fairchild Semiconductor
R2	Resistor, 150 kΩ, 1%, 0.1W	0603	CRCW0603150KFKEA	Vishay-Dale
R4	Resistor, 8.25 kΩ, 1%, 0.1W	0603	CRCW06038K25FKEA	Vishay-Dale
R5	Resistor, 2.94 kΩ, 1%, 0.1W	0603	CRCW06032K94FKEA	Vishay-Dale
R6	Resistor, 1.54 kΩ, 1%, 0.1W	0603	CRCW06031K54FKEA	Vishay-Dale
R8	Resistor, 64.9 kΩ, 1%, 0.1W	0603	CRCW060364K9FKEA	Vishay-Dale
R10, R37	Resistor, 0Ω, 5%, 0.1W	0603	CRCW06030000Z0EA	Vishay-Dale
R13, R15, R17, R19, R21, R23	Resistor, 1.00Ω, 1%, 0.125W	0805	CRCW08051R00FKEA	Vishay-Dale
R7, R9, R11	Resistor, 1.00kΩ, 1%, 0.1W	0603	CRCW06031K00FKEA	Vishay-Dale
R12, R14, R16, R18, R20, R22	Resistor, 1.00 kΩ, 1%, 0.125W	0603	CRCW08051K00FKEA	Vishay-Dale
TP1, TP4, TP6, TP8, TP10, TP12, TP14, TP16, TP18, TP20, TP22, TP24, TP31, TP33, TP35, TP37, TP40, TP54, TP56, TP58, TP60, TP62, TP64	Terminal, Turret		1502–2	Keystone
TP3, TP26, TP27, TP28, TP29, TP30, TP34, TP36, TP41, TP42, TP43, TP44, TP45, TP46, TP47, TP48, TP49, TP50, TP51, TP52, TP53, TP55, TP57, TP59, TP61, TP63		Orange	5008	Keystone
TP2	Test Point	Red	5005	Keystone
TP38	Test Point	White	5007	Keystone
TP39	Test Point	Black	5006	Keystone

5 Board Layout

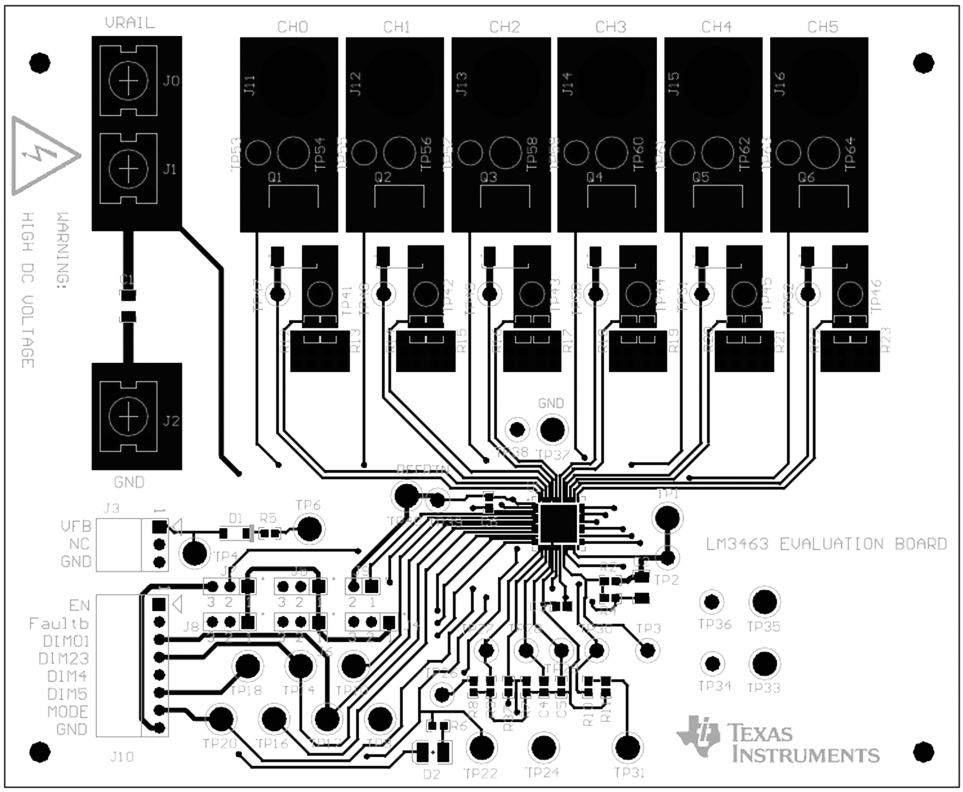

Figure 2. Top Layer

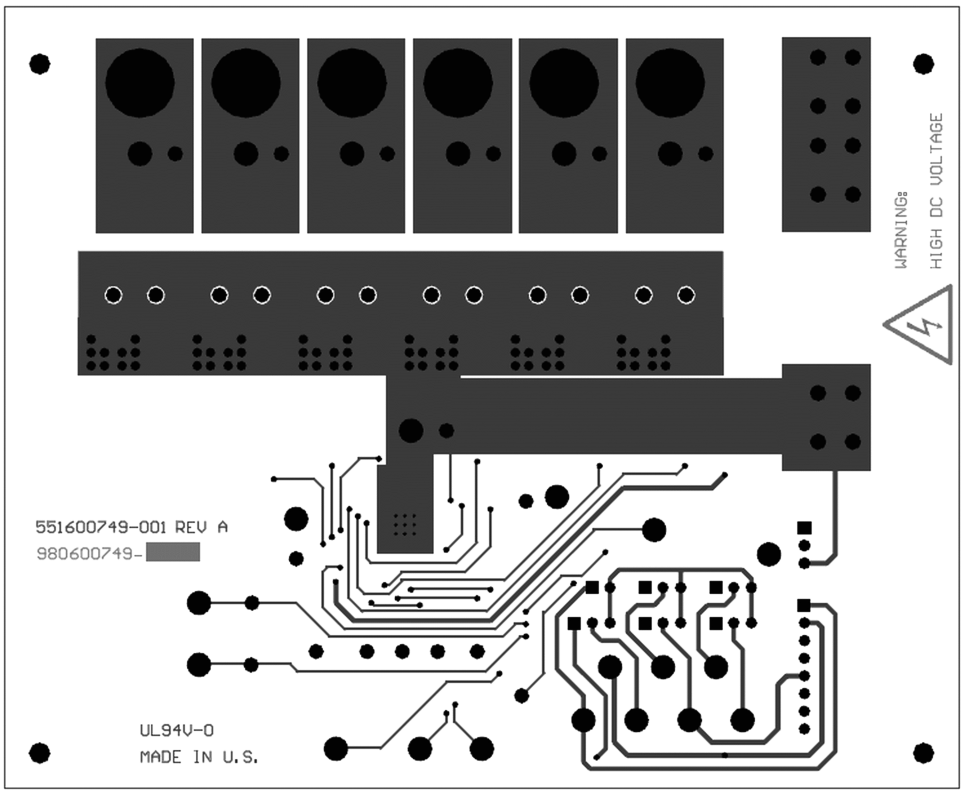

Figure 3. Bottom Layer

6 Connection Diagram

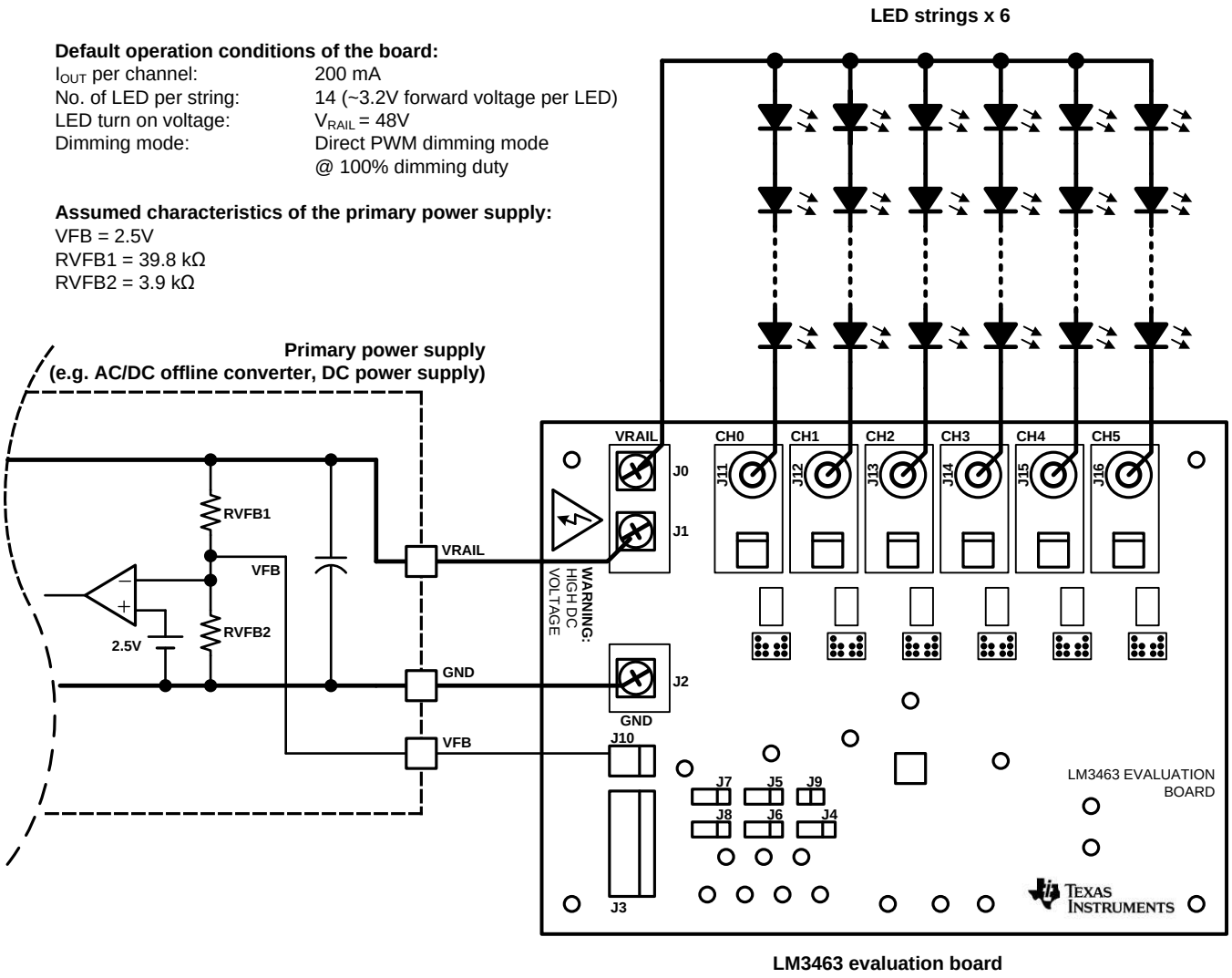

Figure 4. Connecting the LM3463 evaluation board to a primary power supply

7 Primary Power Supply

The LM3463 evaluation board is designed to operate with an external primary power supply. A primary power supply can be any kind of DC power supply with an accessible output voltage feedback node. For instance, either an AC/DC off-line power converter or a DC/DC switching converter can be used as a primary power supply. The LM3463 evaluation board should connect to the primary power supply via three terminals, the VRAIL, GND and VFB as shown in Figure 1.

The board includes three screw type connectors for high current connections, namely J0, J1 and J2. The J1 and J2 should connect to the positive and GND output terminals of the primary power supply accordingly with minimum of wire 18 AWG.

Generally, the board is designed to drive from one to six LED strings of 14 serial LEDs per string. The driving current of each sting is set to 200 mA by default, thus assuming each LED carries a 3.2V forward voltage, the maximum total output power of this evaluation board under steady state is about 54W.

Because the output voltage of the primary power supply, V_{RAIL} is controlled by the Dynamic Headroom Control (DHC) circuit of the LM3463 to maintain maximum system efficiency, therefore the V_{RAIL} must have a wide and adjustable voltage range.

Generally the required range of the V_{RAIL} is determined by the highest and lowest possible forward voltages of the LED strings (respectively, $V_{LED-MAX-COLD}$ and $V_{LED-MIN-HOT}$). Since the forward voltage of the LED strings varies according to the changing of the ambient temperature, the voltage for turning the LEDs on at system startup must be set higher than the $V_{LED-MAX-COLD}$.Figure 5 shows the different voltage level of V_{RAIL} at system startup.

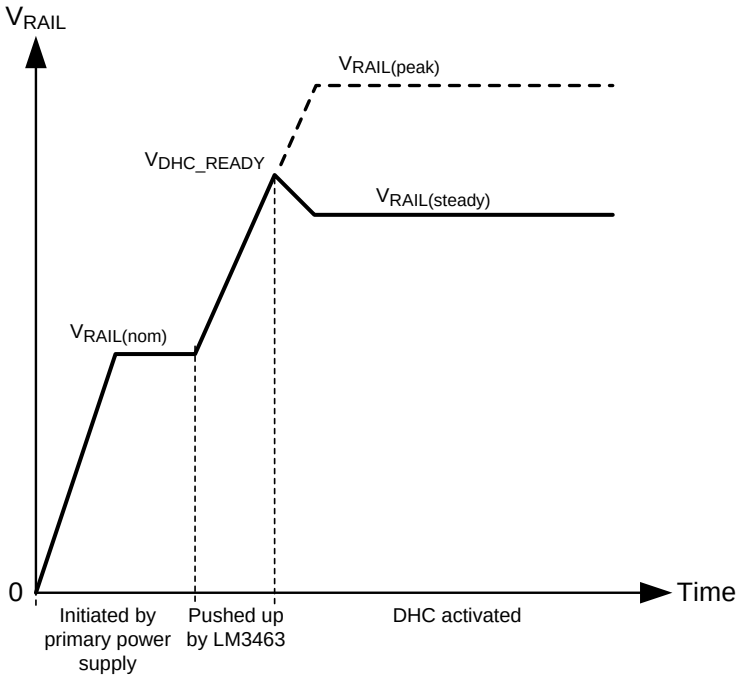

Figure 5. Different voltage levels of the V_{RAIL} at system startup

In Figure 5, the V_{RAIL} is the output voltage of the primary power supply under the control of the LM3463. $V_{RAIL(peak)}$ is the highest level of V_{RAIL} when the voltage of the OutP pin of the LM3463 equals 0V. V_{DHC_READY} is the voltage level that the LM3463 turns all output channels on. $V_{RAIL(nom)}$ is the nominal output voltage of the primary power supply when the OutP pin voltage is higher than V_{FB}+0.6V (i.e. prior to DHC starting)

In order to secure sufficient rail voltage to maintain regulated LED currents when enabling the output channels, the $V_{RAIL(peak)}$ and V_{DHC_READY} must be set higher than $V_{LED-MAX-COLD}$ (the highest forward voltage of the LED strings under low ambient temperature). The following settings are suggested to ensure correct system startup sequence:

1. $V_{RAIL(nom)} = V_{LED-MIN-HOT} - 5V$
2. $V_{DHC\_READY} = V_{LED-MAX-COLD} + 5V$
3. $V_{RAIL(peak)} = V_{DHC\_READY} + 5V$

Figure 6 shows a suggested procedure to determine the $V_{RAIL(nom)}$, V_{DHC_READY} and $V_{RAIL(peak)}$.

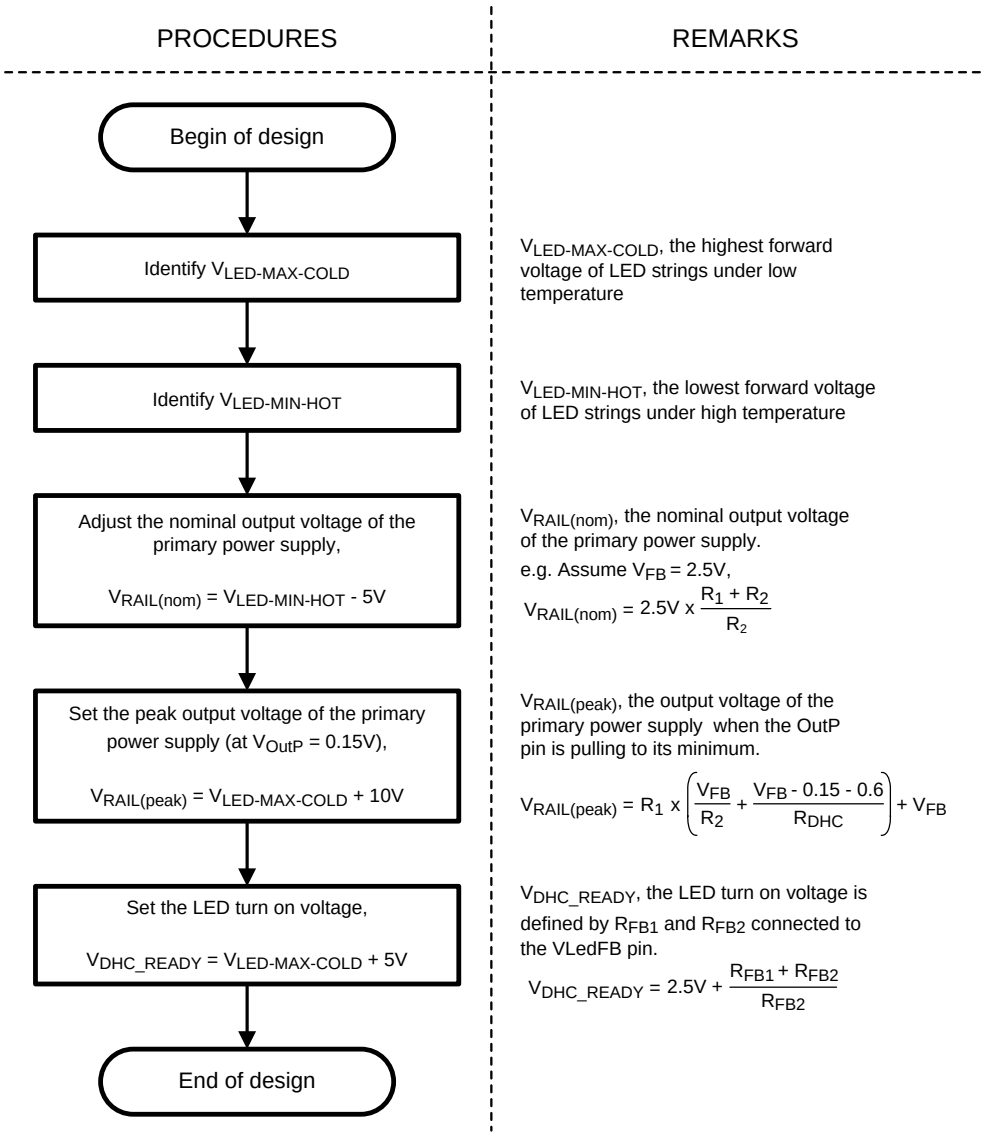

Figure 6. Procedures of setting the rail voltage levels.

Because the $V_{RAIL(peak)}$ is the possible highest output voltage of the primary power supply with the LEDs turned on, the primary power supply must be able to deliver an output power no less than the total LED current multiplied by the $V_{RAIL(peak)}$. The flow chart in Figure 7 shows the recommended procedure of selecting a power supply for the LM3463 evaluation board. If the power supply is an off-the-shelf product, the output voltage and value of the output voltage feedback resistor divider may need to be changed to allow DHC.

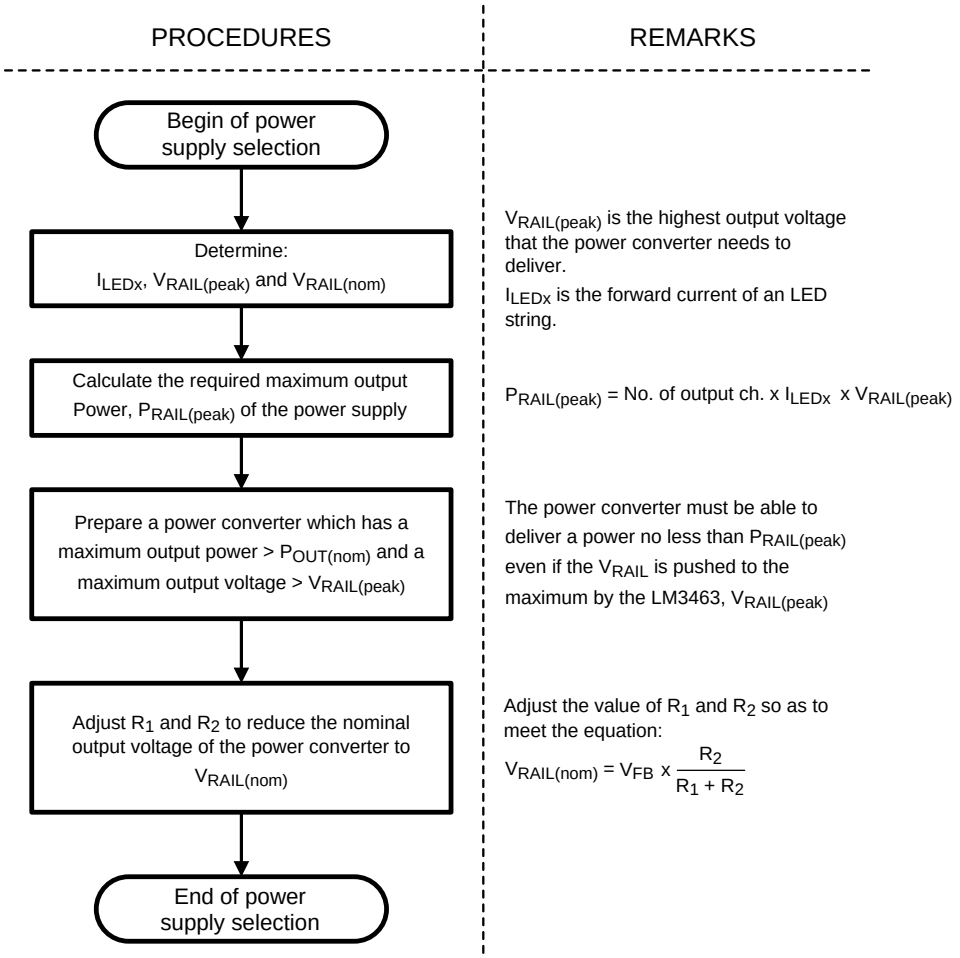

Figure 7. Procedure of selecting a primary power supply

Going through the above procedures, the value of the R5, R2 and R4 are determined. The values of the R5, R2 and R4 on the LM3463 evaluation board are 2.94 kΩ, 150 kΩ and 8.25 kΩ respectively. The resistors may need replacing as needed to interface the board to a primary power supply.

8 Response of the DHC Loop

The cut-off frequency of the DHC loop $f_{C(LM3463)}$ is determined by the value of the external capacitor, C4. The $f_{C(LM3463)}$ is governed by the following equation.

$$f_{C(LM3463)} = \left(\frac{1}{2\Pi \times CDHC \times R_{CDHC\text{-}SOURCE}} \right) Hz \quad (1)$$

The default value of the C4 on the board is 1 uF which sets the cut-off frequency of the DHC loop to 0.1Hz.

In order to secure stable operation of the system, the cut-off frequency of the DHC loop of the LM3463 must be set lower than that of the primary power supply. Usually a DHC response of 1/10 of which of the primary power supply is enough to secure stable operation. In the case where the primary power supply has an unknown frequency response, the selection of the value of the C4 can be based on estimation. Use a 1 uF ceramic capacitor as an initial value and reduce the value of C4 to increase the DHC loop response as needed.

9 Reducing the System Startup Time

The total system startup time is generally dependent on the frequency response of both the primary power supply and DHC loop of the LM3463. The slower response of the two circuits, the longer time the system takes to startup. Because the response of the primary is usually not user programmable, the overall system startup time can be reduced by shortening the time for the V_{RAIL} to increase from $V_{RAIL(nom)}$ to V_{DHC_READY}, namely the t_{ST}. as shown in Figure 8. The t_{ST} is adjusted dependent on the value of the C4 and RISR, which governed by the following equation:

$$t_{ST} = \left[\frac{3.6V - V_{OutP}}{\left(7.33\mu A + \frac{1.25V}{R_{ISR}}\right)} \right] \times C_{CDHC} \text{ in sec.} \quad (2)$$

where

$$V_{OutP} = \left[V_{FB} - 0.6V - R_{DHC} \times \left(\frac{V_{DHC\text{-}READY} - V_{FB}}{R_1} - \frac{V_{FB}}{R_2} \right) \right] \quad (3)$$

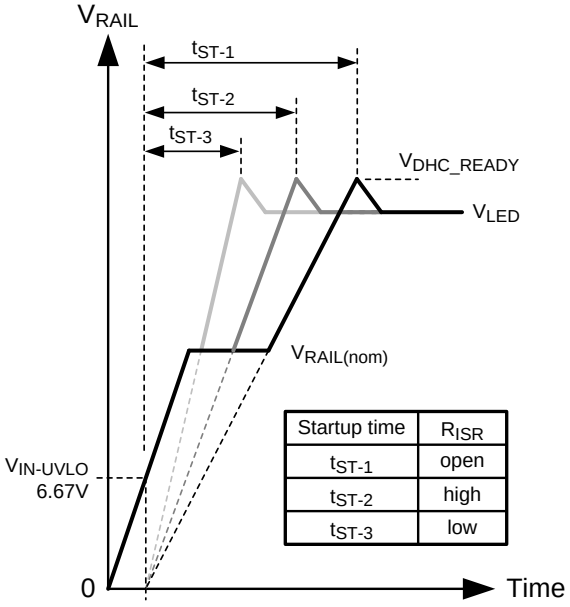

Figure 8. Adjusting the tST with different value of RISR

The R9 on this evaluation board is opened by default, thus the system startup time is set to the longest. The startup time of the board can be reduced by putting a 0603 resistor to the position of R9. The value of the R9 should be no less than 130kΩ.

10 MOSFET Power Dissipation Limit

As the drain voltage of the MOSFETs (Q1, Q2, Q3, Q4, Q5 and Q6) exceeds four times the voltage of the DRVLIM pin, the output currents are reduced to reduce the power dissipations on the MOSFETs. The DRVLIM of the LM3463 of this evaluation board is connected to VCC via a 0Ω resistor, R37. Thus the drain voltage threshold to perform MOSFET power dissipation limit is about 26.4V by default.

11 Analog Dimming Control

The reference voltage for the LED current regulators can be adjusted by changing the voltage at the IOUTADJ pin of the LM3463. In this evaluation board, the reference voltage for current regulation is set to 200mV by connecting the IOUTADJ pin to VCC via a 0Ω resistor, R10. By default the pull-down resistor to the IOUTADJ pin, R11 is opened. To adjust the IOUTADJ pin voltage, the R10 and R11 should be replaced according to the required output current following the equation below:

$$I_{OUTn} = \frac{[(V_{IOUTADJ} \times 0.0782) + 4.3 \times 10^{-3}]}{R_{ISNSn}} \quad (4)$$

The IOUTADJ pin can be biased by a positive voltage in the range of 0V to 2.5V across the terminals TP31and TP39. If the IOUTADJ pin is going to be biased by an external voltage source, the R10 and R11 should be removed.

12 PWM Dimming Control

The LM3463 evaluation board allows three different modes of PWM dimming control:

- Direct PWM Dimming Mode
- Serial Interface Mode
- DC Interface Mode
- The mode of PWM dimming control is selected by changing the position of the shunt jumper of J8.

Mode of dimming control	Setting of J8
Direct PWM dimming mode	Short Pos. 2–3
Serial interface mode	Open
DC interface mode	Short Pos. 1–2

Using PWM dimming control, the six output channels of the board are grouped into four individual groups which are controlled by four individual PWM signals at the terminals TP12, TP14, TP16 and TP18.

Terminal	Involved channels
TP12	CH0, CH1
TP14	CH2, CH3
TP16	CH4
TP18	CH5

The terminals J4, J5, J6 and J7 are used to connect the DIM01(TP12), DIM23(TP14), DIM4(TP16) and DIM5(TP18) pins of the LM3463 to either VCC or GND. The jumpers on these terminals should be removed if external dimming control signals are applied to the board.

Direct PWM Dimming Mode

In the direct PWM dimming mode, the board accepts standard active high TTL level PWM signals to perform dimming control. The minimum on duty is generally limited by the gate capacitance of the external MOSFETs. Normally, an 8 µs minimum on time is suggested.

Serial Interface Mode

In the serial interface mode, the on duty of each output channel is controlled by a data byte of 8 bits wide. In this mode the terminals TP12, TP14 and TP16 on the board comprise a serial data interface to receive data bytes from external data source. The connection to the DIM5 pin is not used and should be connected to GND by shortening the pins 2 and 3 of J7. The functions of the TP12, TP14 and TP16 in the serial interface mode are as listed in the following table:

Serial Interface Mode	
Terminal	**Function**
TP12	Serial data input
TP14	Clock signal input
TP16	End Of data Frame (EOF) signal input

In the serial interface mode the LM3463 evaluation board accepts a data frame which consists of four data bytes to control the on duty of the four groups of output channels via the terminal TP12 (DIM01). Every data byte contains 8 bits in LSB (Least Significant Bit) first ordering and is clocked into the data buffer of the LM3463 at every rising edge of clock signal at the terminal TP14 (DIM23). Every time a data frame is clocked in to the LM3463 the terminal TP16 (DIM4) should be pulled low to generate a falling edge to indicate an 'End-Of-Frame (EOF)'. Figure 9 shows the typical waveform of a data frame and the corresponding clock and EOF signals.

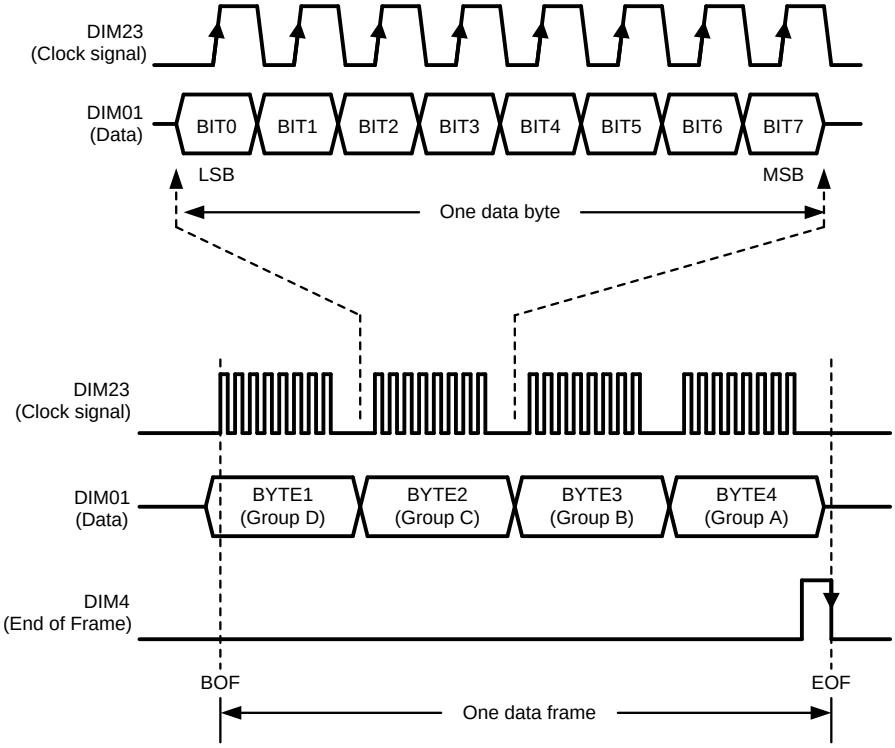

Figure 9. Typical waveforms of a complete data frame in the serial interface mode

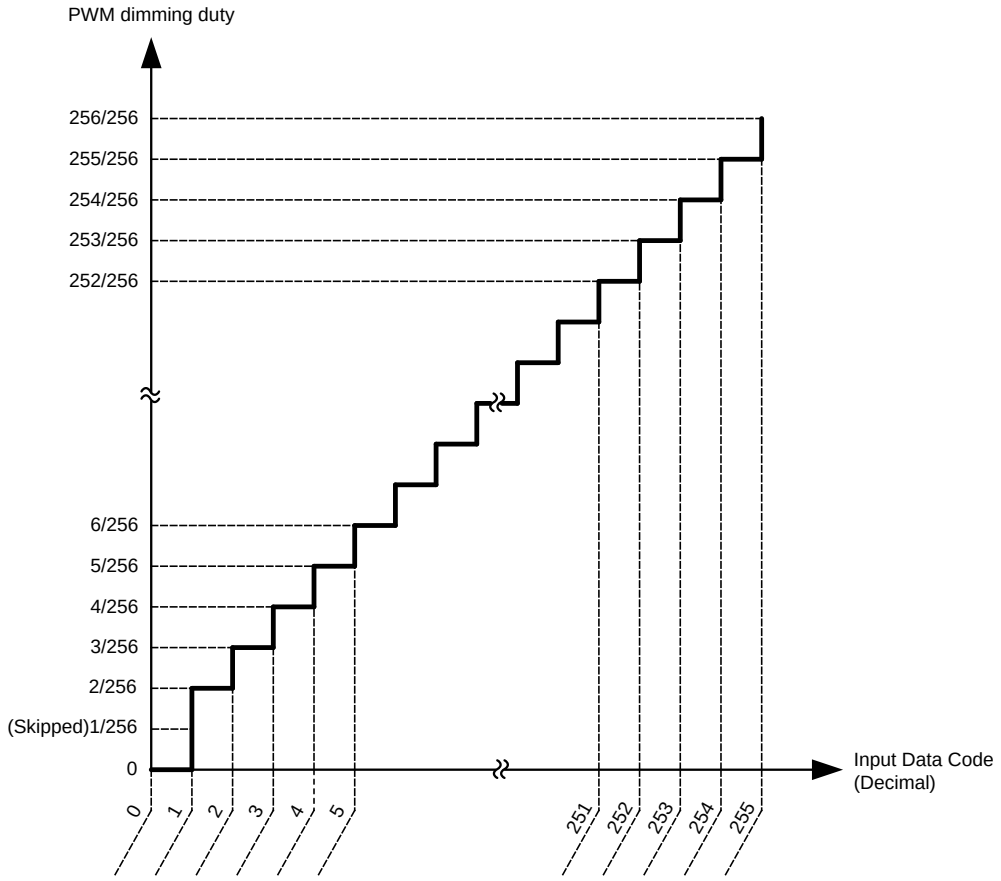

Figure 10. PWM dimming duty vs code value of a data byte

In the serial interface mode, the six output channels are grouped into four individual groups. The on duty of each group is controlled by the value of a specific data byte as listed in the following table:

Output channel	Data byte
CH0, CH1	BYTE1
CH2, CH3	BYTE2
CH4	BYTE3
CH5	BYTE4

Because the data width of a data byte is fixed to 8 bits, the step size of the LED current is equal to 1/256 of the full scale current. To allow the use of 0% on duty, the steps 1 and 2 are combined to give a 2/256 on duty. Thus either applying a hexadecimal code 001h or 002h the LM3463 will give a 2/256 on duty. The dimming duty in the serial interface mode is governed by the following equation:

$$D_{SERIAL\text{-}DIM} = \left(\frac{\text{data byte value} + 1}{256} \right) \times 100\% \quad (5)$$

Figure 10 shows the relationship of the code value of a data byte and PWM dimming duty.

DC Interface Mode

In the DC interface mode, the on duty of the output channels are adjusted according to the voltage on the terminals TP12, TP14, TP16 and TP20. In this mode, the six output channels are grouped into four groups and controlled by the voltage on four terminals individually as listed in the following table:

Output channel	Terminal
CH0, CH1	TP12
CH2, CH3	TP14
CH4	TP16
CH5	TP18

The voltage being applied to the terminals should be in the range of 0.8V to 5.7V. The dimming duty in the DC interface mode is governed by the following equation:

$$D_{DC\text{-}DIM} = \left[\left(V_{DIMn} - 0.8V \right) \times 20.4082 \right] \% \quad (6)$$

In this mode, the conversion of analog voltage to dimming duty is accomplished by an internal 8-bit ADC of the LM3463, thus the step size of the LED current is equal to 1/256 of the full scale current. To allow the use of 0% on duty, the steps 1 and 2 are combined to give a 2/256 on duty. Thus either applying a voltage in the range of 0.8V to 0.8V+V_{LSB} to the dimming control inputs will result in a 2/256 on duty. Figure 11 shows the Conversion characteristics of the analog voltage to PWM dimming control circuit:

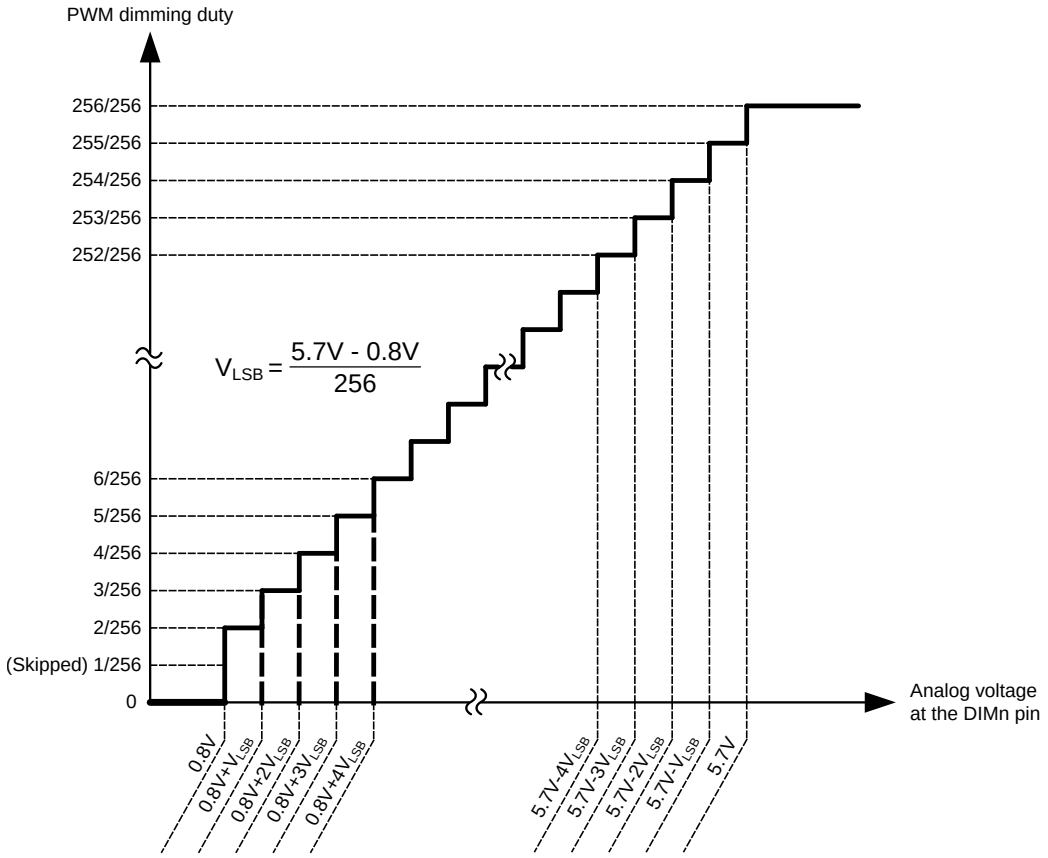

Figure 11. Conversion characteristic of the analog voltage to PWM dimming control circuit

13 Disabling Output Channel(s)

An output channel of this evaluation board can be disabled by not connecting an LED string to the output terminal. A disabled channel is excluded from the DHC loop and remained in OFF state until a falling edge at the EN pin or system repower is applied. The channel 0 must be used regardless of the number of disabled channel.

14 Cascading the LM3463 evaluation board

A number of the LM3463 evaluation boards can be cascaded to expand the number of output channels. The connection among boards differs depending on the selected mode for dimming control. The connection diagrams for the serial interface mode, DC interface mode and direct PWM mode are as illustrated in the Figure 12, Figure 13, and Figure 14, respectively.

When a number of the LM3463 evaluation boards are cascaded, one of the boards must be set as master unit and the other boards must be set as slave units. The master unit is the board which has the VFB terminal connected to the primary power supply. The master unit controls the system startup time and distributes dimming control signals to the slave units, the connections among the boards differs depending on the mode of dimming control being selected.

By default, the LM3463 evaluation board is set as a master unit in direct PWM dimming mode with 100% on duty. To set a board to be a slave unit, the resistors R2 and R4 must be removed and the terminal TP3 (VLedFB pin of the LM3463) should be connected to the terminal TP22 (VCC pin of the LM3463) using an external connection.

In cascade operation, the number of slave units is virtually unlimited. However, in high power applications the accumulated voltage drop on the power return part could impair the function of the DHC. Generally it is suggested not to cascade more than four pieces of the LM3463 evaluation board to secure stable system operation.

15 PCB Design

Good heat dissipation helps optimize the performance of the LM3463. The ground plane should be used to connect the exposed pad of the LM3463, which is internally connected to the LM3463 die substrate. The area of the ground plane should be extended as much as possible on the same copper layer around the LM3463. Using numerous vias beneath the exposed pad to dissipate heat of the LM3463 to another copper layer is also a good practice.

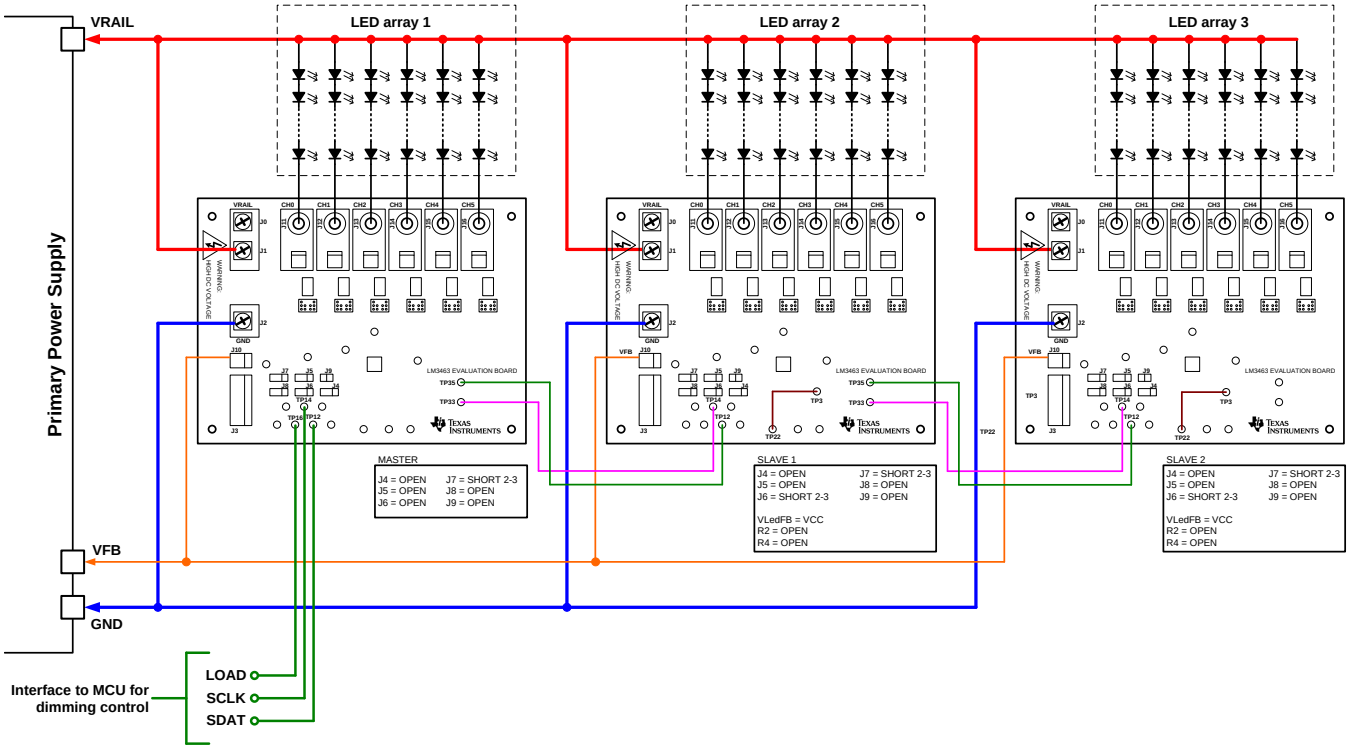

Figure 12. A 12 channel lighting system using serial interface mode for dimming control

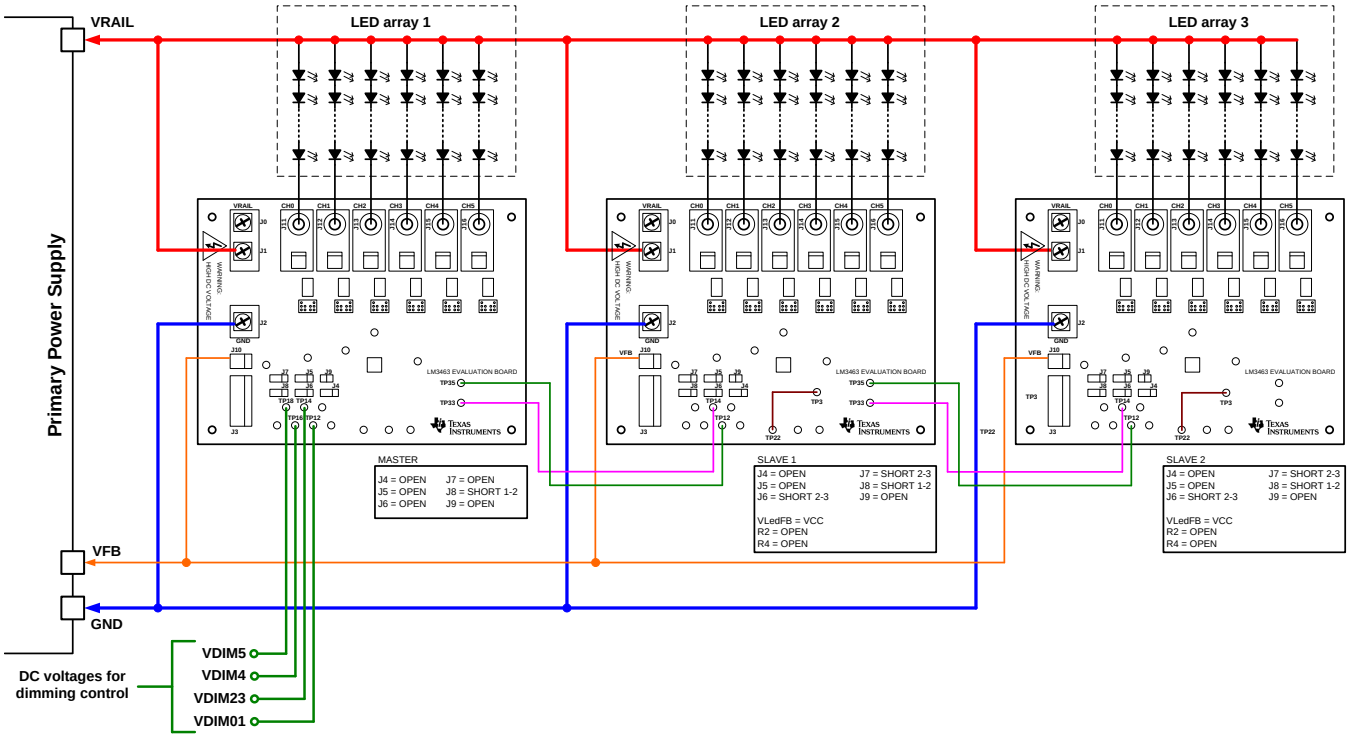

Figure 13. A 12 channel lighting system using DC interface mode for dimming control

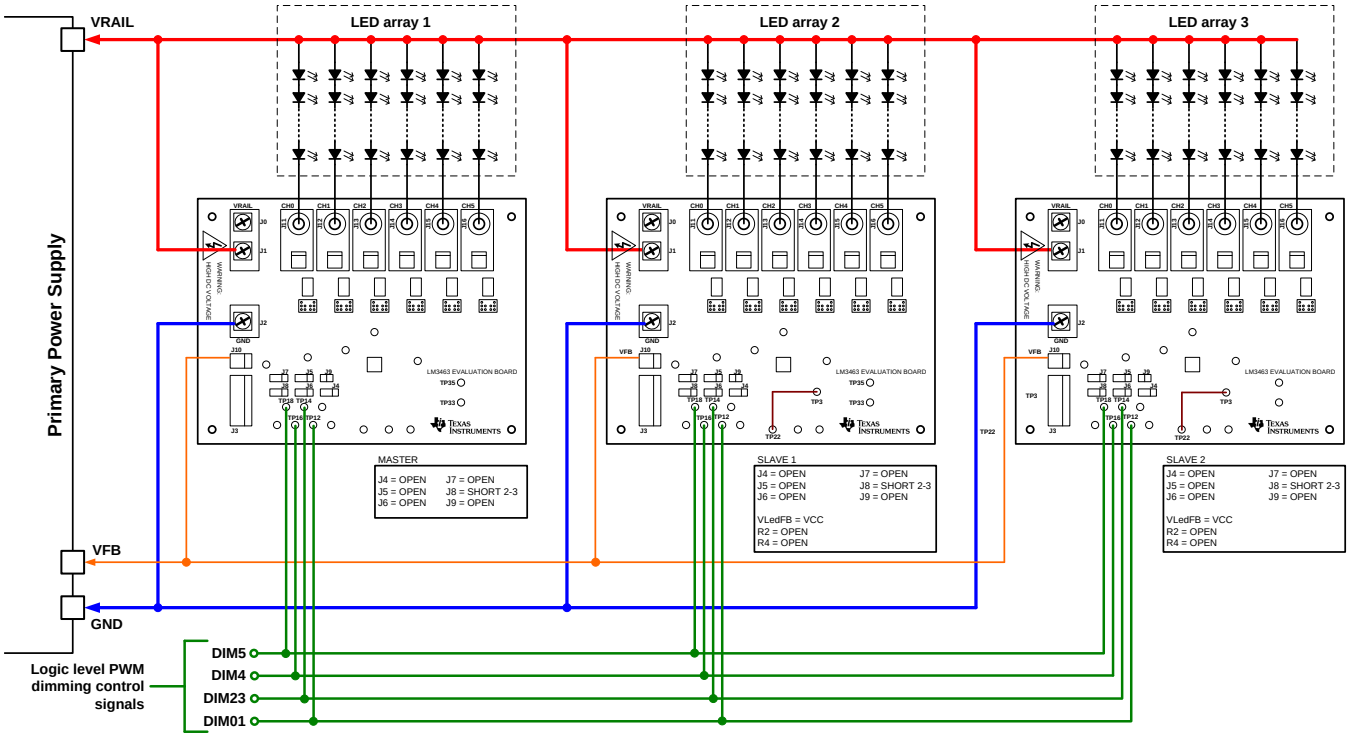

Figure 14. A 12 channel lighting system using Direct PWM mode for dimming control

16 Typical Waveforms

All curves taken at V_{IN} = 48V with configuration in typical application for driving twelve power LEDs with six output channels active and 200 mA output current per channel. T_A = 25°C, unless otherwise specified.

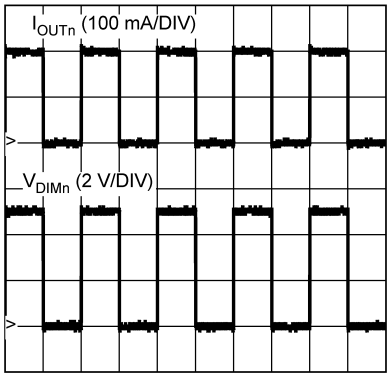

Figure 15. Direct PWM Dimming Mode 250Hz 50% dimming duty at DIMn pin

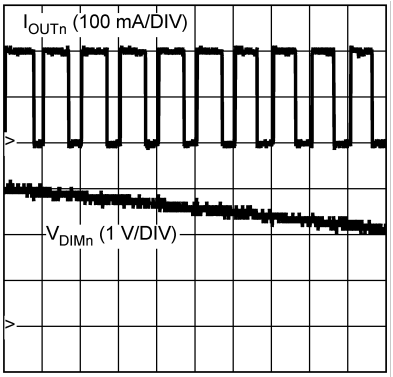

Figure 16. DC Interface Mode 10Hz 3V to 2V ramp at DIMn pin

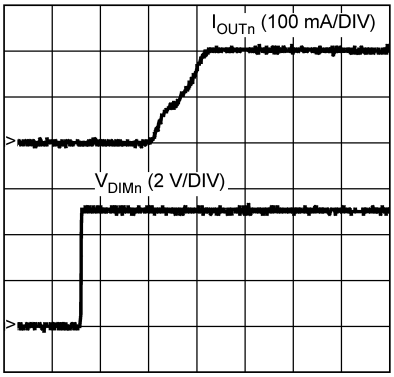

Figure 17. PWM dimming I_{OUTn} delay at V_{DIMn} rising

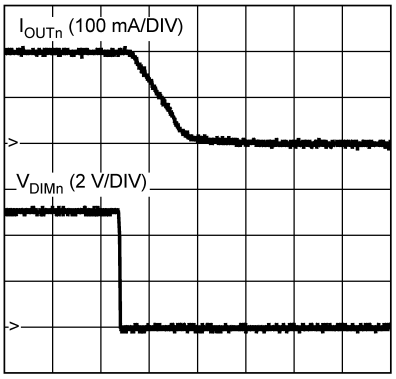

Figure 18. PWM dimming I_{OUTn} delay at V_{DIMn} falling

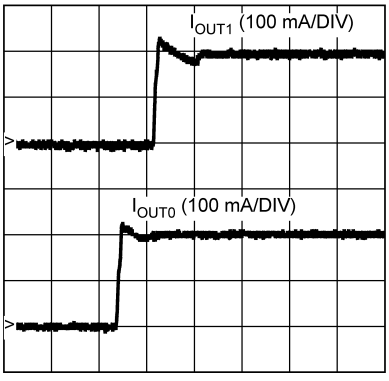

Figure 19. I_{OUTn} ch-ch delay I_{OUTn} rising

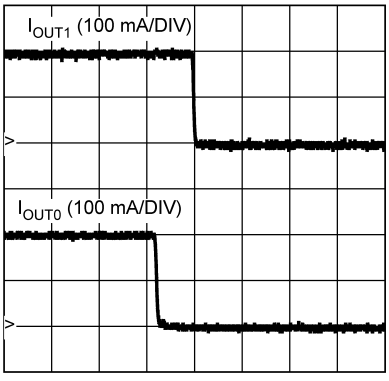

Figure 20. I_{OUTn} ch-ch delay I_{OUTn} falling

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