

- Configured for 3-Phase Brushless Motor Drive
- Low  $r_{DS(on)}$  . . . 0.25  $\Omega$  Typ
- High Voltage Output . . . 30 V
- Pulsed Current . . . 12 A Per Channel
- Input Transient and ESD Protection
- Compatible With High-Side and Low-Side Current Sense Resistors

### description

The TPIC1310 is a monolithic gate-protected power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors configured as a three-half H-bridge.

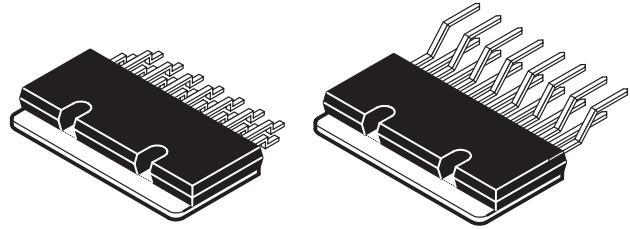
When suitably heat sunk, the TPIC1310 can drive motors requiring 2.5 A of phase current. The DMOS transistors are immune to second breakdown effects and current crowding, problems often associated with bipolar transistors.

The TPIC1310 is offered in 15-pin through-hole (KTS) and surface-mount (KTR) PowerFLEX™ packages and is characterized for operation over the case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

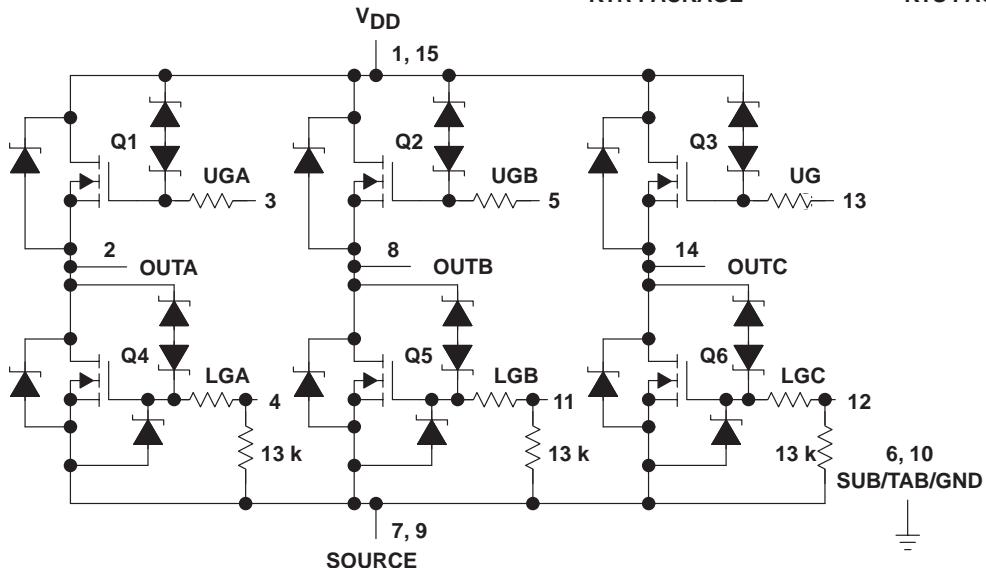
KTR or KTS PACKAGE  
(TOP VIEW)

V <sub>DD</sub>	1
OUTA	2
UGA	3
LGA	4
UGB	5
SUB/GND	6
SOURCE	7
OUTB	8
SOURCE	9
SUB/GND	10
LGB	11
LGC	12
UGC	13
OUTC	14
V <sub>DD</sub>	15

Tab is SUB/GND



### schematic



NOTES: A. Terminals 1 and 15 must be externally connected.  
B. Terminals 6 and 10 must be connected to GND.  
C. Terminals 7 and 9 must be connected to the sense resistor or GND.  
D. No terminal may be taken greater than 0.5 V below GND.



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**TPIC1310**  
**3-HALF H-BRIDGE GATE PROTECTED**  
**POWER DMOS ARRAY**

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**absolute maximum ratings over operating case temperature range (unless otherwise noted)†**

Drain-to-source voltage, $V_{DS}$ .....	30 V
Output-to-GND voltage .....	30 V
SOURCE-to-SUB/GND voltage .....	-0.3 V to 20 V
Gate-to-source voltage range, $V_{GS}$ .....	-0.3 V to 20 V
Continuous output current, each output, all outputs on, $T_C = 25^\circ\text{C}$ .....	3 A
Continuous source-to-drain diode current, $T_C = 25^\circ\text{C}$ .....	3 A
Pulsed output current, each output, $I_{max}$ , $T_C = 25^\circ\text{C}$ (see Note 1 and Figure 14) .....	12 A
Continuous $V_{DD}$ and SOURCE current, $T_C = 25^\circ\text{C}$ .....	3 A
Pulsed $V_{DD}$ and SOURCE current, $T_C = 25^\circ\text{C}$ (see Note 1) .....	12 A
Continuous total dissipation, $T_C = 25^\circ\text{C}$ (see Note 2 and Figure 14) .....	13.9 W
Operating virtual junction temperature range, $T_J$ .....	-40°C to 150°C
Operating case temperature range, $T_C$ .....	-40°C to 125°C
Storage temperature range .....	-65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds .....	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Pulse duration = 10  $\mu\text{s}$ , duty cycle  $\leq 2\%$   
2. Package is mounted in intimate contact with an infinite heat sink.

**electrical characteristics,  $T_C = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(\text{BR})\text{DSX}}$	Drain-to-source breakdown voltage	$I_D = 250 \mu\text{A}$ ,	$V_{GS} = 0$	30			V
$V_{GS(\text{th})}$	Gate-to-source threshold voltage	$I_D = 1 \text{ mA}$ ,	$V_{DS} = V_{GS}$ , See Figure 4	0.9	1.2	1.7	V
$V_{(\text{BR})\text{GS}}$	Gate-to-source breakdown voltage	Low-side	$I_{GS} = 250 \mu\text{A}$	20			V
$V_{(\text{BR})\text{SG}}$	Source-to-gate breakdown voltage	Low-side	$I_{SG} = 250 \mu\text{A}$	0.3			V
		High-side	$I_{SG} = 250 \mu\text{A}$	20			
$V_{DS(\text{on})}$	Drain-to-source on-state voltage		$I_D = 3 \text{ A}$ , $V_{GS} = 14 \text{ V}$ , See Notes 3 and 4		0.66	0.9	V
$V_{F(\text{SD})}$	Forward on-state voltage, source-to-drain		$I_S = 3 \text{ A}$ , $V_{GS} = 0$ , See Notes 3 and 4 and Figure 11		1.1	1.4	V
$I_{DSS}$	Drain current-gate shorted to source	$V_{DS} = 28 \text{ V}$ ,	$T_C = 25^\circ\text{C}$	0.05	1		$\mu\text{A}$
		$V_{GS} = 0$	$T_C = 125^\circ\text{C}$	0.5	10		
$I_{GSSF}$	Forward-gate current, drain short circuited to source	Low-side	$V_{SG} = 16 \text{ V}$ , $V_{DS} = 0$ , Internal 13 k $\Omega$ from gate to source	2	4		mA
		High-side	$V_{SG} = 16 \text{ V}$ , $V_{DS} = 0$	20	200		
$I_{GSSR}$	Reverse-gate current, drain short circuited to source		$V_{SG} = 0.3 \text{ V}$ , $V_{DS} = 0$	20	200		nA
$I_{lkg}$	Leakage current, drain-to-GND gate shorted to source	$V_{DGND} = 28 \text{ V}$	$T_C = 25^\circ\text{C}$	0.05	1		$\mu\text{A}$
			$T_C = 125^\circ\text{C}$	0.5	10		
$r_{DS(\text{on})}$	Static drain-to-source on-state resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 3 \text{ A}$ , See Notes 3 and 4 and Figures 5 and 6	$T_C = 25^\circ\text{C}$	0.27	0.37		$\Omega$
			$T_C = 125^\circ\text{C}$	0.45	0.55		
		$V_{GS} = 14 \text{ V}$ , $I_D = 3 \text{ A}$ , See Notes 3 and 4 and Figures 5 and 6	$T_C = 25^\circ\text{C}$	0.22	0.32		
			$T_C = 125^\circ\text{C}$	0.32	0.47		
$g_{fs}$	Forward transconductance	$V_{DS} = 10 \text{ V}$ , See Notes 3 and 4 and Figure 8	$I_D = 3 \text{ A}$	0.5	0.85		S
$C_{iss}$	Short-circuit input capacitance, low-side	$V_{DS} = 25 \text{ V}$ , $f = 1 \text{ MHz}$ ,	$V_{GS} = 0$ , See Figure 10	110			pF
$C_{oss}$	Short-circuit output capacitance, low-side			120			
$C_{rss}$	Short-circuit reverse transfer capacitance, low-side			60			

† Engineering estimate

NOTES: 3. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

**source-to-drain and GND-to-drain diode characteristics,  $T_C = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{rr}$	Reverse-recovery time	High-side	$I_S = 3 \text{ A}$ ,	$V_{DS} = 28 \text{ V}$ ,	30		ns
$Q_{RR}$	Total diode charge		$V_{GS} = 0$ , See Figures 1 and 13	$di/dt = 100 \text{ A}/\mu\text{s}$ ,	30		nC
$t_{rr}$	Reverse-recovery time	Low-side	$I_S = 3 \text{ A}$ ,	$V_{DS} = 28 \text{ V}$ ,	70		ns
$Q_{RR}$	Total diode charge		$V_{GS} = 0$ , See Figure 13, SUB/GND connected to SOURCE	$di/dt = 100 \text{ A}/\mu\text{s}$ ,	350		nC

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**resistive-load switching characteristics,  $T_C = 25^\circ\text{C}$**

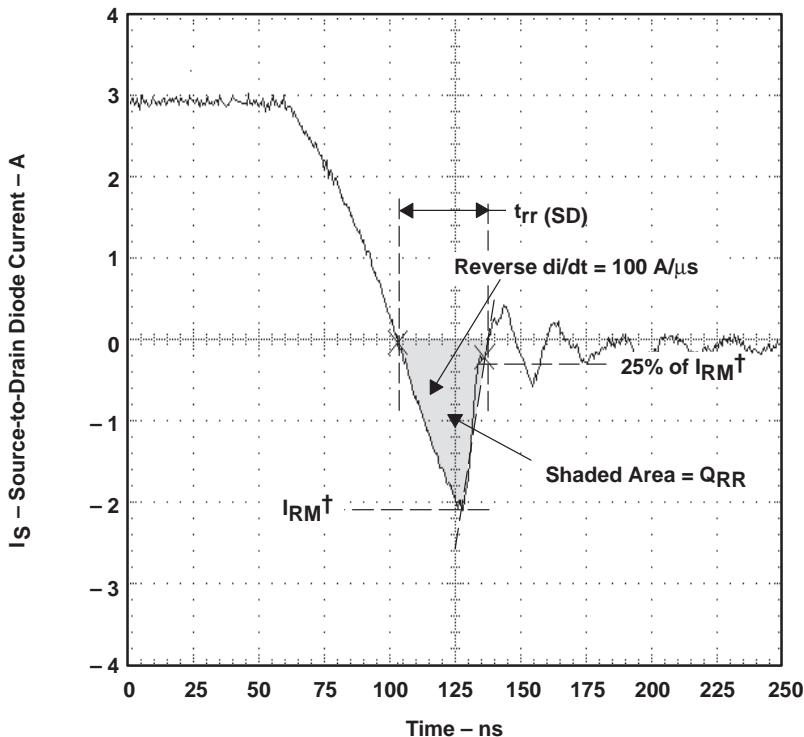
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$ Turn-on delay time	$V_{DD} = 28 \text{ V}, R_L = 9.3 \Omega, t_{en} = 10 \text{ ns}, t_{dis} = 10 \text{ ns},$ See Figure 2	70			ns
$t_{d(off)}$ Turn-off delay time		200			
$t_r$ Rise time		140			
$t_f$ Fall time		55			
$Q_g$ Total gate charge	$V_{DS} = 12 \text{ V}, I_D = 3 \text{ A}, V_{GS} = 10 \text{ V},$ See Figure 3 and Figure 12	1.6	2		nC
$Q_{gs(th)}$ Threshold gate-to-source charge		0.5	0.62		
$Q_{gd}$ Gate-to-drain charge		0.25	0.31		
$L_D$ Internal drain inductance		5			nH
$L_S$ Internal source inductance		5			
$R_g$ Internal gate resistance		500			$\Omega$

**thermal resistance**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JC}$ Junction-to-case thermal resistance, one output on	See Note 5	7.5	9		$^\circ\text{C/W}$
$R_{\theta JC}$ Junction-to-case thermal resistance, two outputs on	See Notes 5 and 6	4.5	5.5		$^\circ\text{C/W}$

NOTES: 5. Package mounted in intimate contact with infinite heatsink.  
6. Two outputs with equal power

PARAMETER MEASUREMENT INFORMATION



<sup>†</sup>  $I_{RM}$  = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

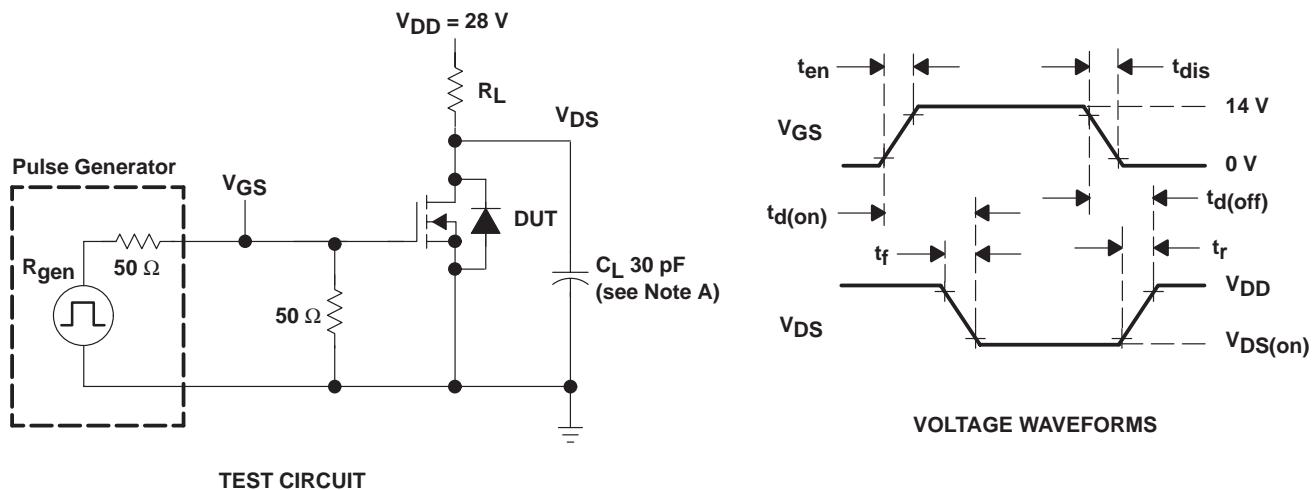


Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

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**TYPICAL CHARACTERISTICS**

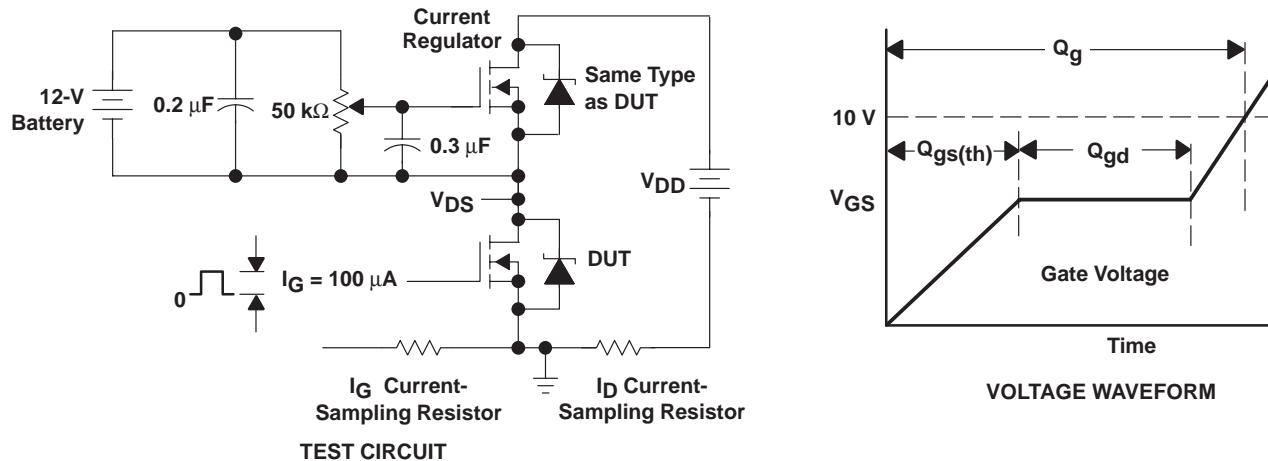


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

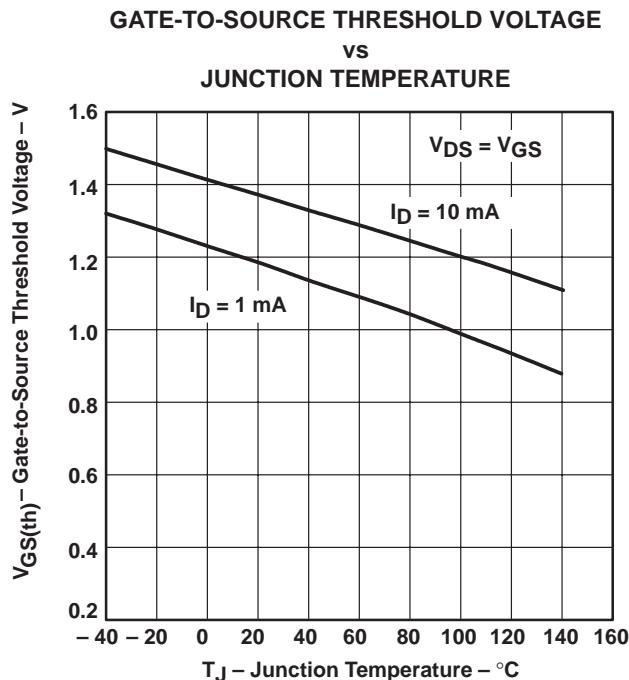


Figure 4

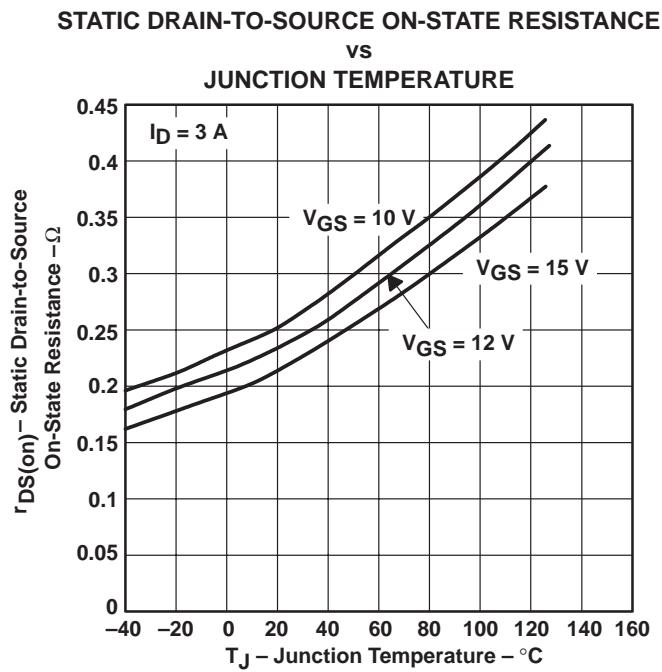


Figure 5

## TYPICAL CHARACTERISTICS

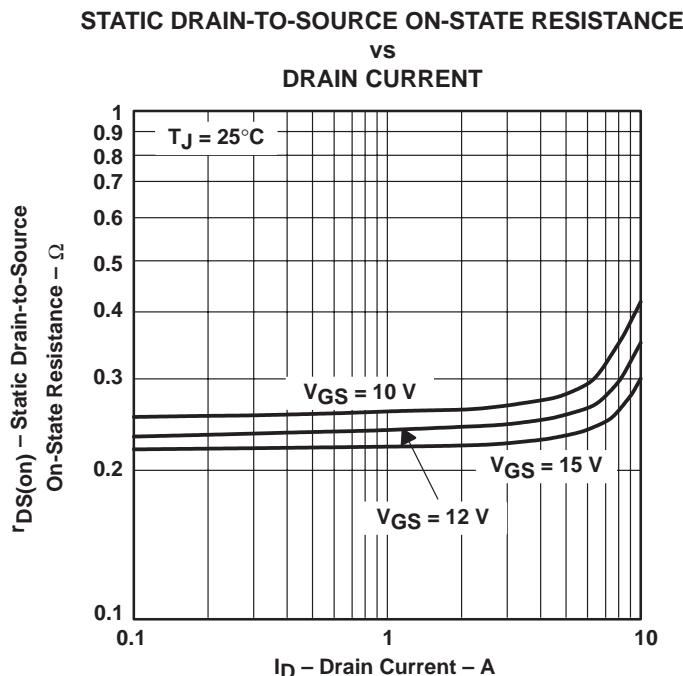


Figure 6

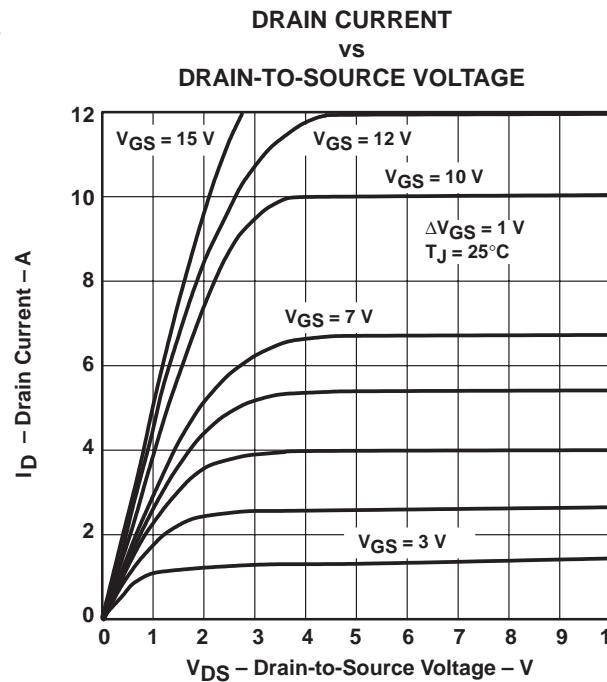


Figure 7

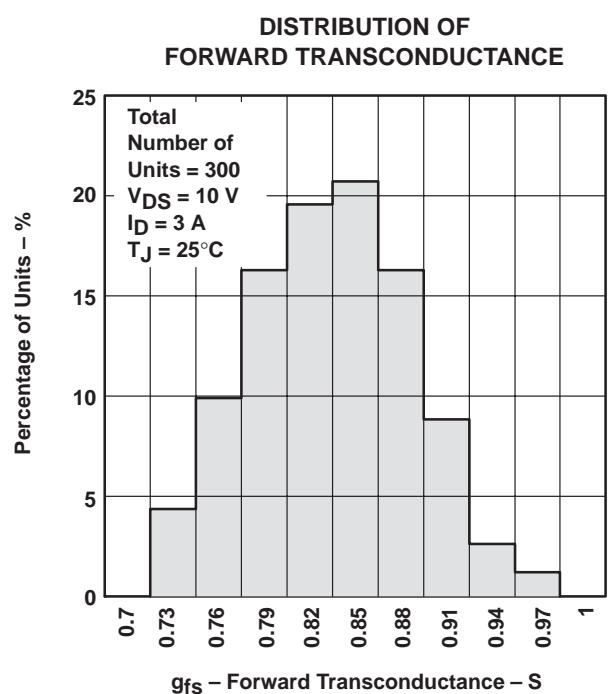


Figure 8

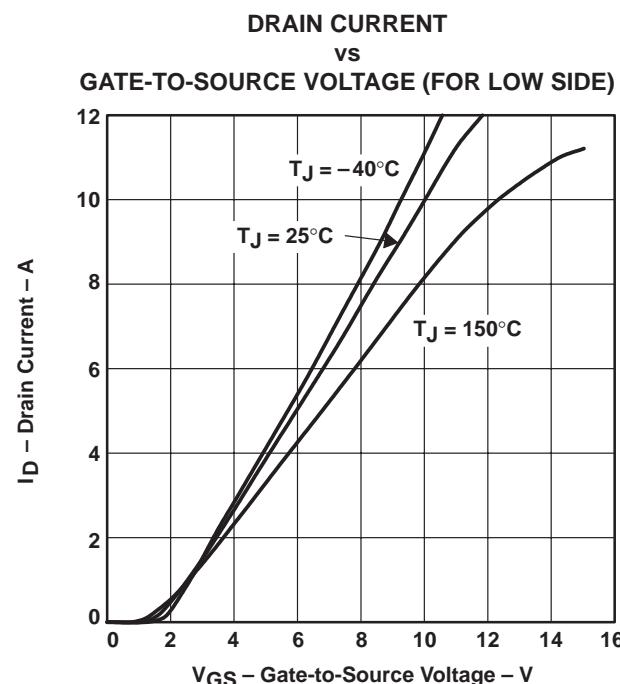


Figure 9

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**TYPICAL CHARACTERISTICS**

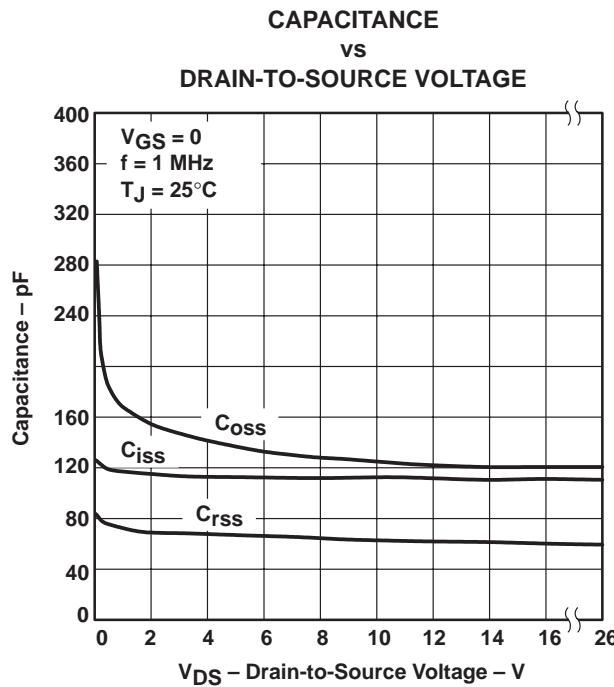


Figure 10

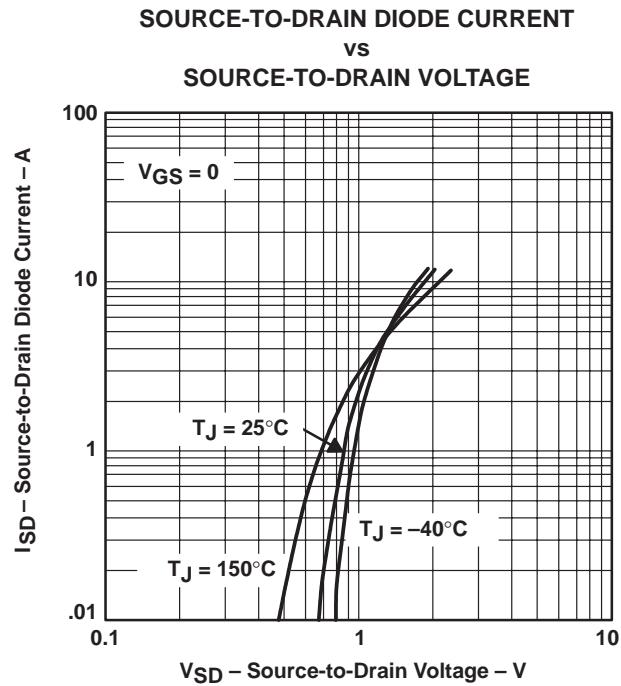


Figure 11

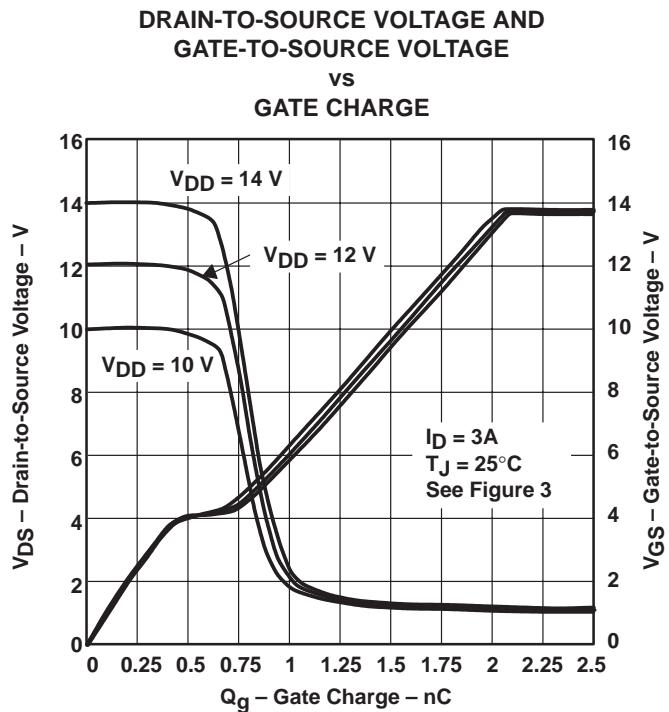


Figure 12

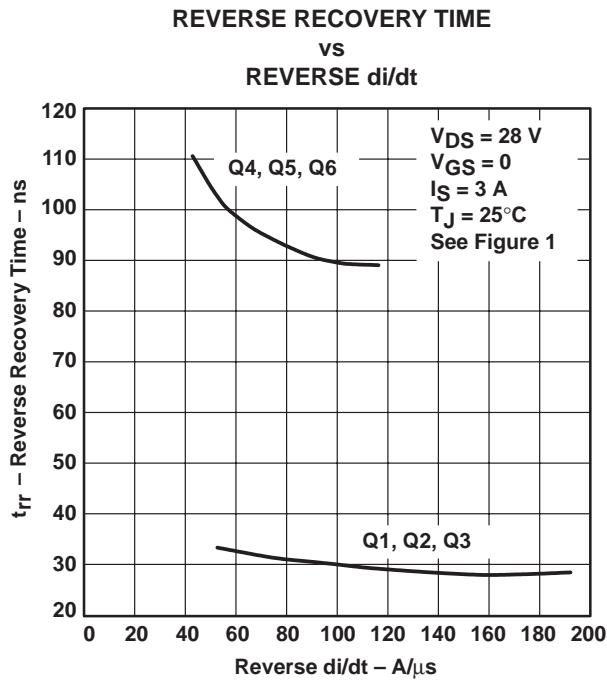
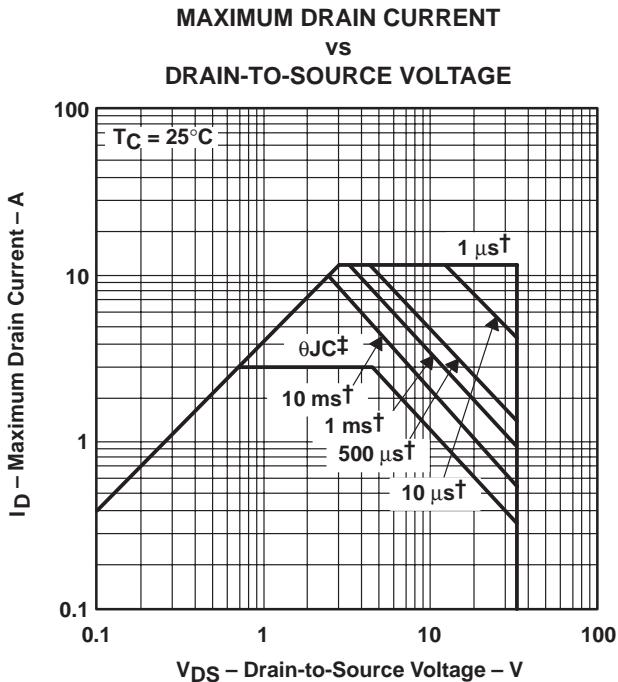


Figure 13

## THERMAL INFORMATION



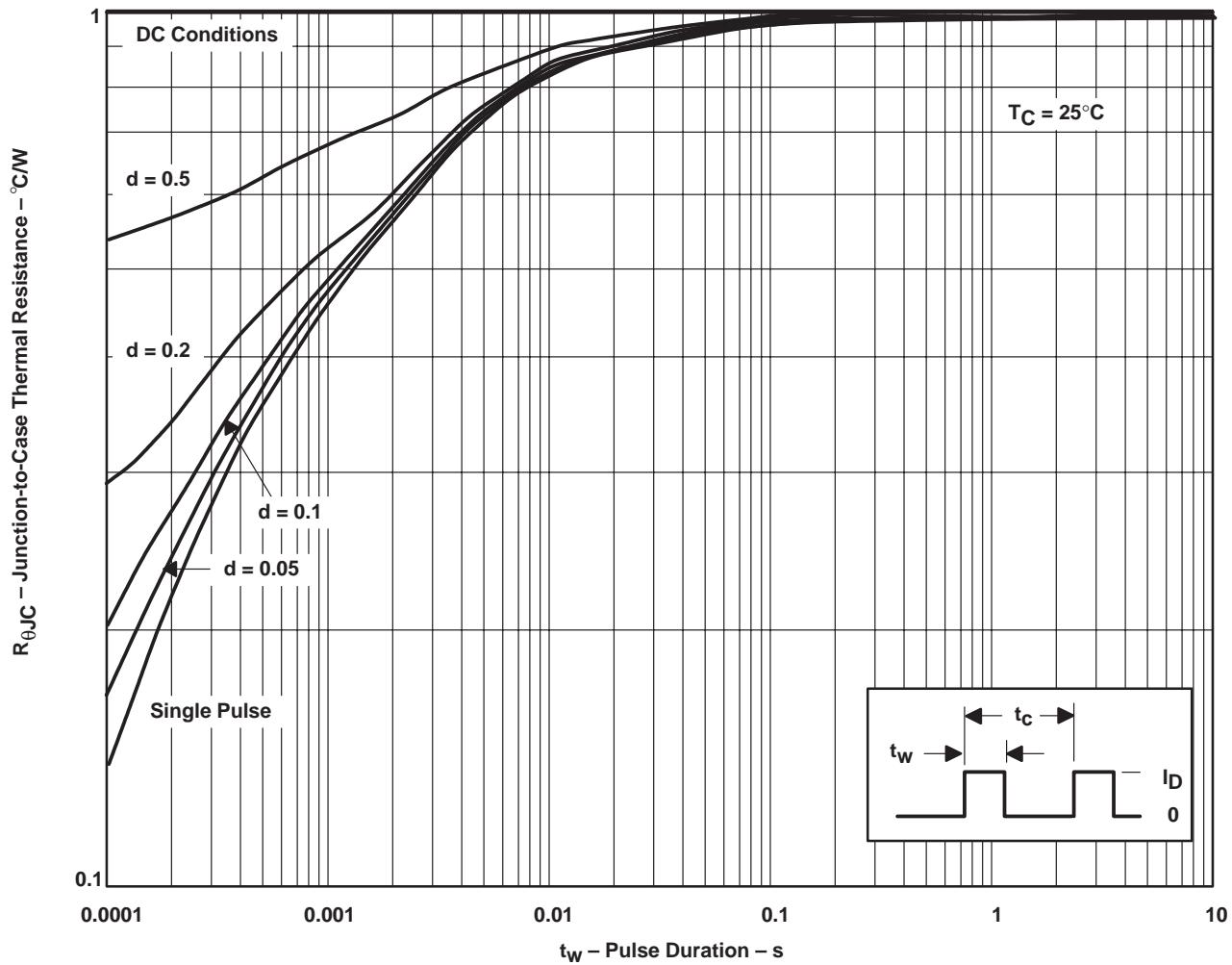
† Less than 2% duty cycle

‡ Device mounted in intimate contact with infinite heatsink.

Figure 14

## THERMAL INFORMATION

### JUNCTION-TO-CASE THERMAL RESISTANCE vs PULSE DURATION



† Package mounted in intimate contact with infinite heat sink.

NOTE E:  $Z_{\theta JC}(t) = r(t) R_{\theta JC}$

$t_w$  = pulse duration

$t_c$  = cycle time

$d$  = duty cycle =  $t_w/t_c$

Figure 15

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPIC1310KTR	OBsolete	PFM	KTR	15		TBD	Call TI	Call TI
TPIC1310KTS	OBsolete	PFM	KTS	15		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

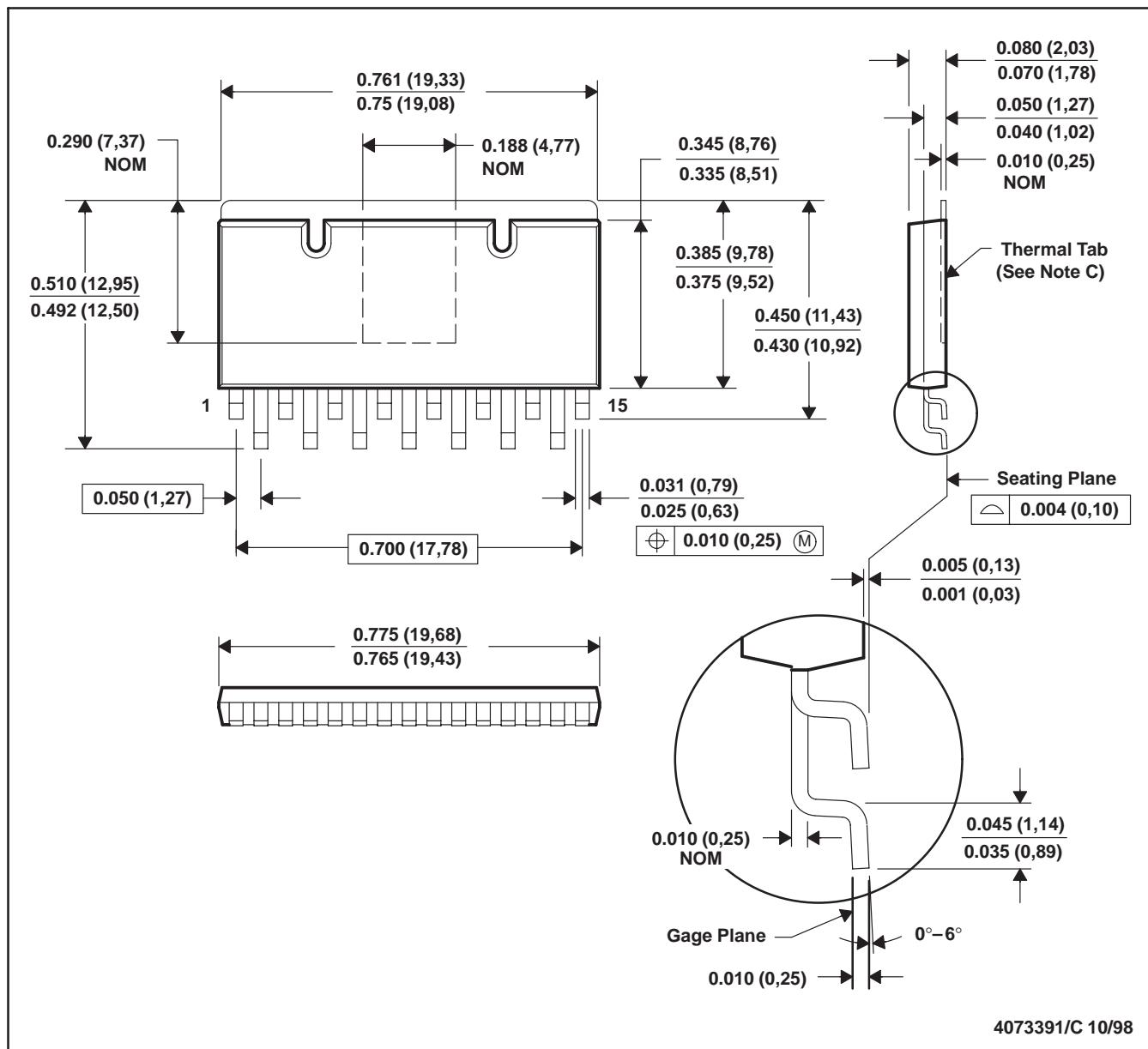
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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KTR (R-PSFM-G15)

PowerFLEX™ PLASTIC FLANGE-MOUNT



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. The heatsink area is approximately 78K sq mils.  
 D. Dimensions do not include mold protrusions, not to exceed 0.006 (0.15).

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