

74LVTH16652

Low Voltage 16-Bit Transceiver/Register with 3-STATE Outputs

General Description

The LVTH16652 consists of sixteen bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function (see Functional Description).

The LVTH16652 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

The transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH16652 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 16652
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device model > 1000V

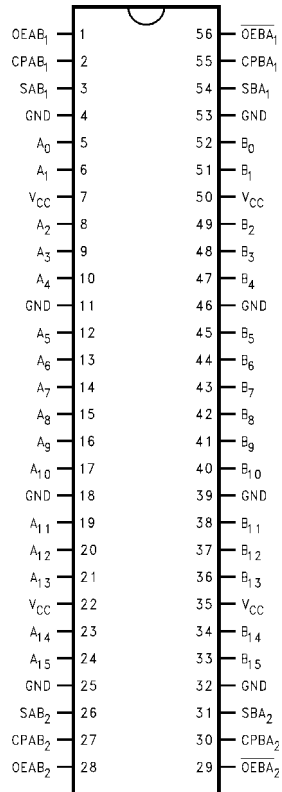
Ordering Code:

| Order Number | Package Number | Package Description |
|----------------|----------------|---|
| 74LVTH16652MEA | MS56A | 56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide |
| 74LVTH16652MTD | MTD56 | 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

74LVTH16652 Low Voltage 16-Bit Transceiver/Register with 3-STATE Outputs

Connection Diagram



Pin Descriptions

| Pin Names | Description |
|---------------------------------------|--|
| A ₀ –A ₁₅ | Data Register A Inputs/ 3-STATE Outputs |
| B ₀ –B ₁₅ | Data Register B Inputs/ 3-STATE Outputs |
| CPAB _n , CPBA _n | Clock Pulse Inputs |
| SAB _n , SBA _n | Select Inputs |
| OEAB _n , OEBA _n | Output Enable Inputs |

Truth Table

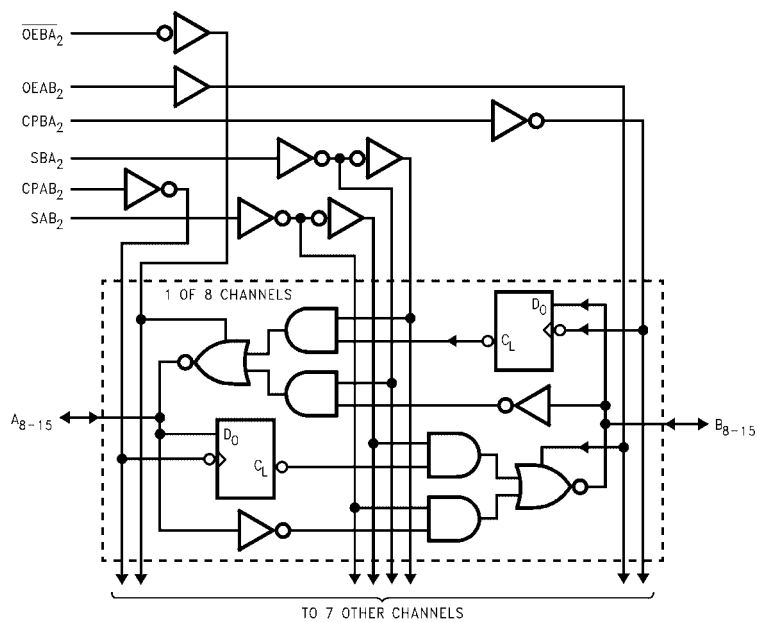
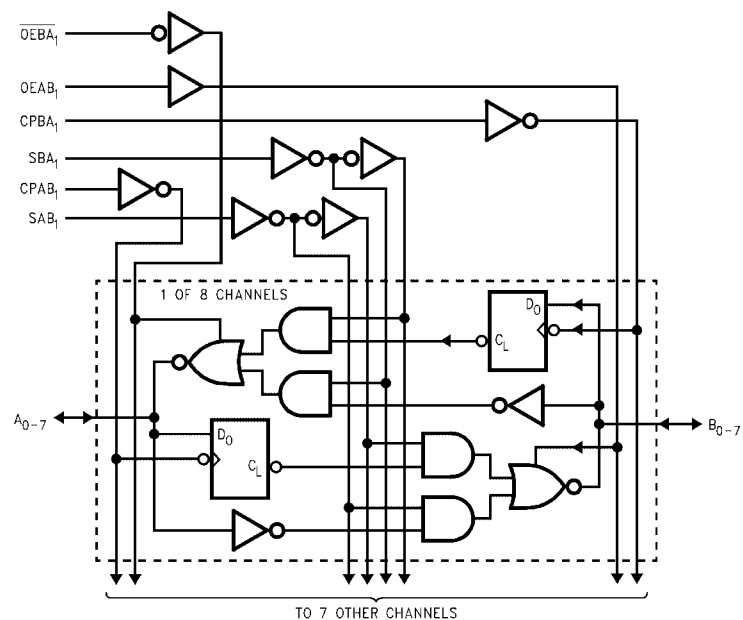
(Note 1)

| Inputs | | | | | | Inputs/Outputs | | Operating Mode |
|-------------------|-------------------|-------------------|-------------------|------------------|------------------|------------------------------------|------------------------------------|--|
| OEAB ₁ | OEBA ₁ | CPAB ₁ | CPBA ₁ | SAB ₁ | SBA ₁ | A ₀ thru A ₇ | B ₀ thru B ₇ | |
| L | H | H or L | H or L | X | X | Input | Input | Isolation |
| L | H | ↗ | ↗ | X | X | | | Store A and B Data |
| X | H | ↗ | H or L | X | X | Input | Not Specified | Store A, Hold B |
| H | H | ↗ | ↗ | X | X | Input | Output | Store A in Both Registers |
| L | X | H or L | ↗ | X | X | Not Specified | Input | Hold A, Store B |
| L | L | ↗ | ↗ | X | X | Output | Input | Store B in Both Registers |
| L | L | X | X | X | L | Output | Input | Real-Time B Data to A Bus |
| L | L | X | H or L | X | H | | | Store B Data to A Bus |
| H | H | X | X | L | X | Input | Output | Real-Time A Data to B Bus |
| H | H | H or L | X | H | X | | | Stored A Data to B Bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored A Data to B Bus and Stored B Data to A Bus |

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial ↗ = LOW-to-HIGH Clock Transition

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs. This also applies to data I/O (A and B: 8–15) and #2 control pins

Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

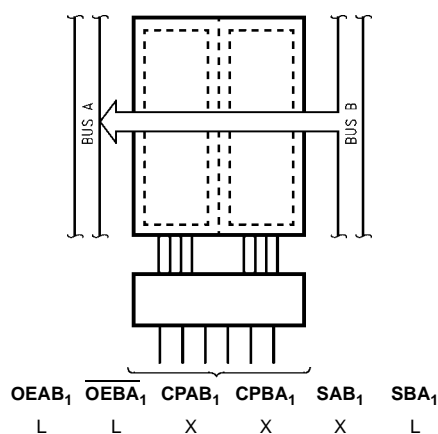
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB_n , SBA_n) controls can multiplex stored and real-time.

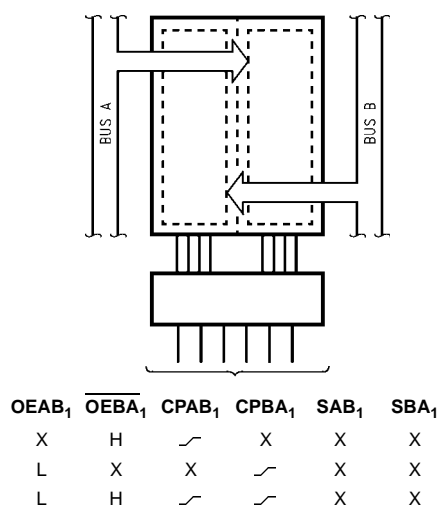
The examples below demonstrate the four fundamental bus-management functions that can be performed with the LVTH16652.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW-to-HIGH transitions at the appropriate Clock Inputs ($CPAB_n$, $CPBA_n$) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling $OEAB_n$ and $OEBA_n$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

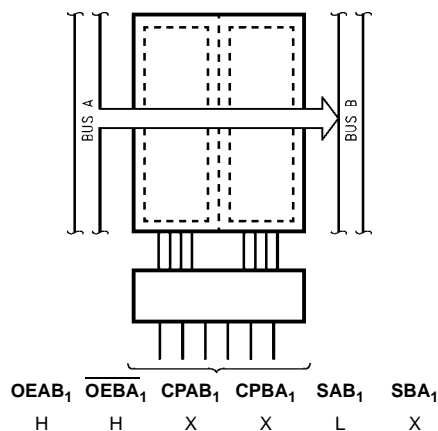
**Real-Time Transfer
Bus B to Bus A**



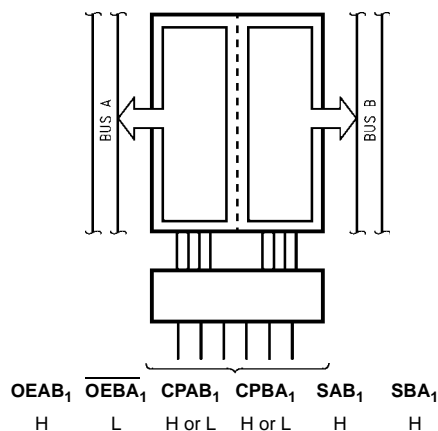
Storage



**Real-Time Transfer
Bus A to Bus B**



**Transfer Storage
Data to A or B**



Absolute Maximum Ratings(Note 2)

| Symbol | Parameter | Value | Conditions | Units |
|-----------|----------------------------------|--------------|--------------------------------------|-------------|
| V_{CC} | Supply Voltage | -0.5 to +4.6 | | V |
| V_I | DC Input Voltage | -0.5 to +7.0 | | V |
| V_O | DC Output Voltage | -0.5 to +7.0 | Output in 3-STATE | V |
| | | -0.5 to +7.0 | Output in HIGH or LOW State (Note 3) | |
| I_{IK} | DC Input Diode Current | -50 | $V_I < GND$ | mA |
| I_{OK} | DC Output Diode Current | -50 | $V_O < GND$ | mA |
| I_O | DC Output Current | 64 | $V_O > V_{CC}$ Output at HIGH State | mA |
| | | 128 | $V_O > V_{CC}$ Output at LOW State | |
| I_{CC} | DC Supply Current per Supply Pin | ± 64 | | mA |
| I_{GND} | DC Ground Current per Ground Pin | ± 128 | | mA |
| T_{STG} | Storage Temperature | -65 to +150 | | $^{\circ}C$ |

Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Units |
|---------------------|---|-----|-----|-------------|
| V_{CC} | Supply Voltage | 2.7 | 3.6 | V |
| V_I | Input Voltage | 0 | 5.5 | V |
| I_{OH} | HIGH-Level Output Current | | -32 | mA |
| I_{OL} | LOW-Level Output Current | | 64 | mA |
| T_A | Free-Air Operating Temperature | -40 | 85 | $^{\circ}C$ |
| $\Delta t/\Delta V$ | Input Edge Rate, $V_{IN} = 0.8V-2.0V$, $V_{CC} = 3.0V$ | 0 | 10 | ns/V |

Note 2: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 3: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) | T _A = -40°C to +85°C | | Units | Conditions |
|----------------------|---|------------------------|---------------------------------|------|-------|---|
| | | | Min | Max | | |
| V _{IK} | Input Clamp Diode Voltage | 2.7 | | -1.2 | V | I _I = -18 mA |
| V _{IH} | Input HIGH Voltage | 2.7-3.6 | 2.0 | | V | V _O ≤ 0.1V or V _O ≥ V _{CC} - 0.1V |
| V _{IL} | Input LOW Voltage | 2.7-3.6 | | 0.8 | | |
| V _{OH} | Output HIGH Voltage | 2.7-3.6 | V _{CC} - 0.2 | | V | I _{OH} = -100 μA |
| | | 2.7 | 2.4 | | | I _{OH} = -8 mA |
| | | 3.0 | 2.0 | | | I _{OH} = -32 mA |
| V _{OL} | Output LOW Voltage | 2.7 | | 0.2 | V | I _{OL} = 100 μA |
| | | 2.7 | | 0.5 | | I _{OL} = 24 mA |
| | | 3.0 | | 0.4 | | I _{OL} = 16 mA |
| | | 3.0 | | 0.5 | | I _{OL} = 32 mA |
| | | 3.0 | | 0.55 | | I _{OL} = 64 mA |
| I _{I(HOLD)} | Bushold Input Minimum Drive | 3.0 | 75 | | μA | V _I = 0.8V |
| | | | -75 | | | V _I = 2.0V |
| I _{I(OD)} | Bushold Input Over-Drive Current to Change State | 3.0 | 500 | | μA | (Note 4) |
| | | | -500 | | | (Note 5) |
| I _I | Input Current | 3.6 | | 10 | μA | V _I = 5.5V |
| | | Control Pins | 3.6 | ±1 | | V _I = 0V or V _{CC} |
| | | Data Pins | 3.6 | -5 | | V _I = 0V |
| I _{OFF} | Power Off Leakage Current | 0 | | ±100 | μA | V _I ≤ V _I or V _O ≤ 5.5V |
| I _{PU/PD} | Power up/down 3-STATE Output Current | 0-1.5V | | ±100 | μA | V _O = 0.5V to 3.0V V _I = GND or V _{CC} |
| I _{OZL} | 3-STATE Output Leakage Current | 3.6 | | -5 | μA | V _O = 0.0V |
| I _{OZH} | 3-STATE Output Leakage Current | 3.6 | | 5 | μA | V _O = 3.6V |
| I _{OZH+} | 3-STATE Output Leakage Current | 3.6 | | 10 | μA | V _{CC} < V _O ≤ 5.5V |
| I _{CCH} | Power Supply Current | 3.6 | | 0.19 | mA | Outputs HIGH |
| I _{CCL} | Power Supply Current | 3.6 | | 5 | mA | Outputs LOW |
| I _{CCZ} | Power Supply Current | 3.6 | | 0.19 | mA | Outputs Disabled |
| I _{CCZ+} | Power Supply Current | 3.6 | | 0.19 | mA | V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled |
| ΔI _{CC} | Increase in Power Supply Current (Note 6) | 3.6 | | 0.2 | mA | One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND |

Note 4: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 6: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 7)

| Symbol | Parameter | V _{CC} (V) | T _A = 25°C | | | Units | Conditions C _L = 50 pF, R _L = 500Ω |
|------------------|--|------------------------|-----------------------|------|-----|-------|---|
| | | | Min | Typ | Max | | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | 3.3 | | 0.8 | | V | (Note 8) |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | 3.3 | | -0.8 | | V | (Note 8) |

Note 7: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 8: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

| Symbol | Parameter | | $T_A = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ $C_L = 50\text{ pF}, R_L = 500\Omega$ | | | | Units |
|------------|--------------------------------|---------------------------------------|---|-----|-----------------|-----|-------|
| | | | $V_{CC} = 3.3V \pm 0.3V$ | | $V_{CC} = 2.7V$ | | |
| | | | Min | Max | Min | Max | |
| f_{MAX} | Maximum Clock Frequency | | 150 | | 150 | | MHz |
| t_{PHL} | Propagation Delay | | 1.3 | 4.8 | 1.3 | 5.4 | ns |
| t_{PLH} | CPAB or CPBA to A or B | | 1.3 | 5.1 | 1.3 | 5.6 | |
| t_{PHL} | Propagation Delay | | 1.0 | 4.5 | 1.0 | 5.1 | ns |
| t_{PLH} | Data to A or B | | 1.0 | 4.4 | 1.0 | 4.7 | |
| t_{PHL} | Propagation Delay | | 1.0 | 4.9 | 1.0 | 5.5 | ns |
| t_{PLH} | SBA or SAB to A or B | | 1.0 | 4.8 | 1.0 | 5.4 | |
| t_{PZL} | Output Enable Time | | 1.0 | 4.9 | 1.0 | 5.8 | ns |
| t_{PZH} | OE to A | | 1.0 | 4.8 | 1.0 | 5.8 | |
| t_{PLZ} | Output Disable Time | | 1.6 | 5.6 | 1.6 | 6.1 | ns |
| t_{PHZ} | OE to A | | 2.0 | 5.4 | 2.0 | 6.1 | |
| t_{PZL} | Output Enable Time | | 1.3 | 5.0 | 1.3 | 5.4 | ns |
| t_{PZH} | OE to B | | 1.3 | 4.8 | 1.3 | 5.4 | |
| t_{PLZ} | Output Disable Time | | 1.3 | 5.5 | 1.3 | 6.2 | ns |
| t_{PHZ} | OE to B | | 1.3 | 5.6 | 1.3 | 6.3 | |
| t_S | Setup Time | A or B before CPAB or CPBA, Data HIGH | 1.2 | | 1.5 | | ns |
| | | A or B before CPAB or CPBA, Data LOW | 2.0 | | 2.8 | | |
| t_H | Hold Time | A or B before CPAB or CPBA, Data HIGH | 0.5 | | 0.0 | | ns |
| | | A or B before CPAB or CPBA, Data LOW | 0.5 | | 0.5 | | |
| t_W | Pulse Width | CPAB or CPBA HIGH or LOW | 3.3 | | 3.3 | | ns |
| t_{OSHL} | Output to Output Skew (Note 9) | | | 1.0 | | 1.0 | ns |
| t_{OSLH} | | | | 1.0 | | 1.0 | |

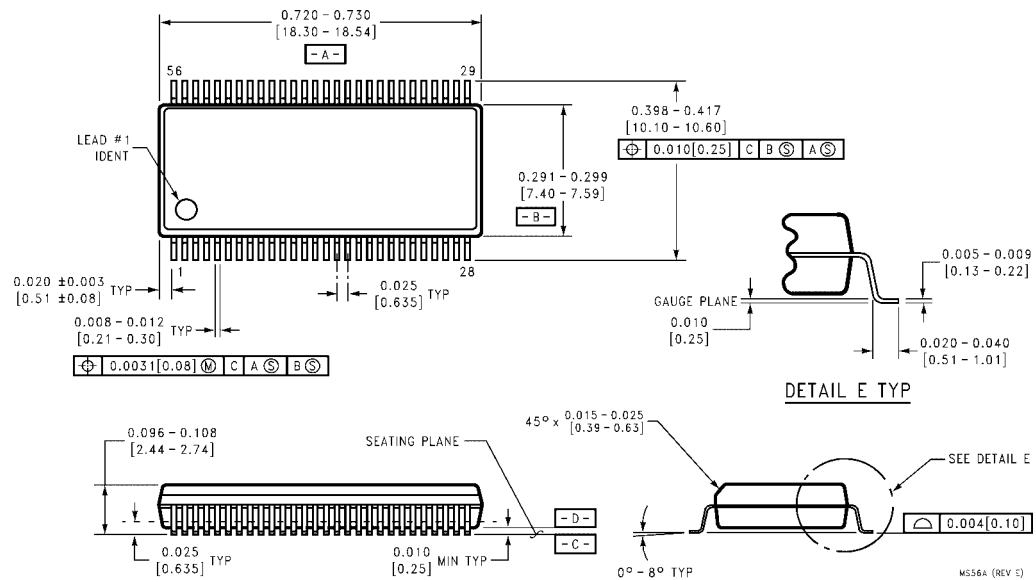
Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 10)

| Symbol | Parameter | Conditions | Typical | Units |
|----------|--------------------------|---|---------|-------|
| C_{IN} | Input Capacitance | $V_{CC} = \text{Open}, V_I = 0V \text{ or } V_{CC}$ | 4 | pF |
| C_{IO} | Input/Output Capacitance | $V_{CC} = 3.0V, V_O = 0V \text{ or } V_{CC}$ | 8 | pF |

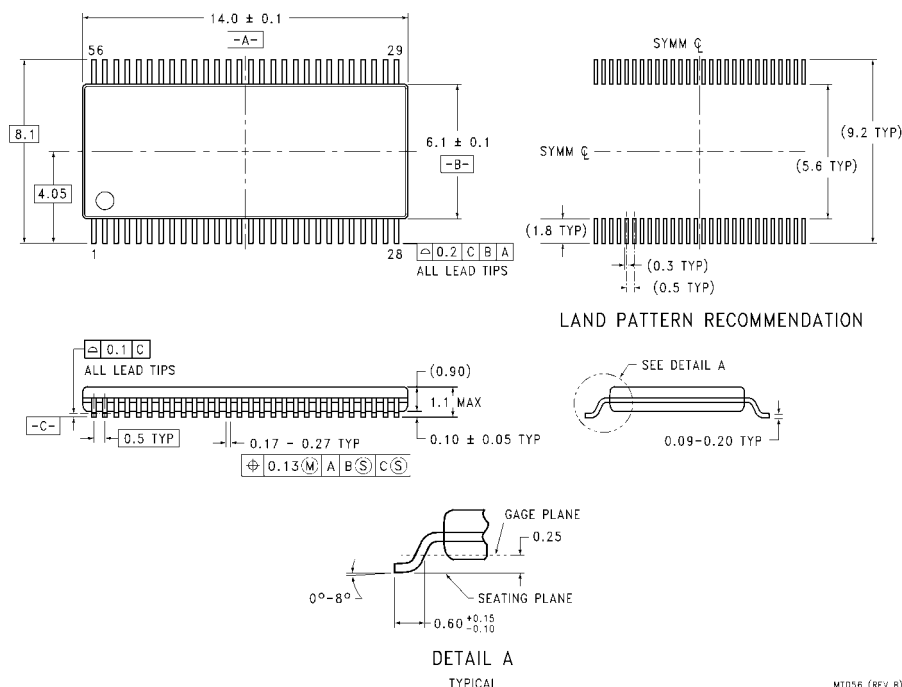
Note 10: Capacitance is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com