

CYPRESS
SEMICONDUCTOR

T-46-23-12

CY7C185A
CY7C186A

8,192 x 8 Static R/W RAM

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
— 20 ns
- Low active power
— 990 mW
- Low standby Power
— 220 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C185A and CY7C186A are high-performance CMOS static RAMs organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. Both devices have an automatic power-down feature ($\overline{CE}_1$), reducing the power consumption by over 75% when deselected. The CY7C185A is in the space saving 300-mil-wide DIP package and leadless chip carrier. The CY7C186A is in the standard 600-mil-wide package.

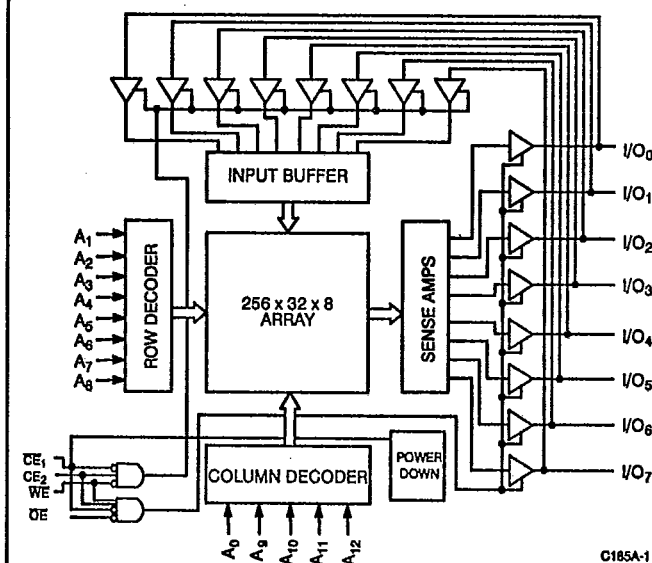
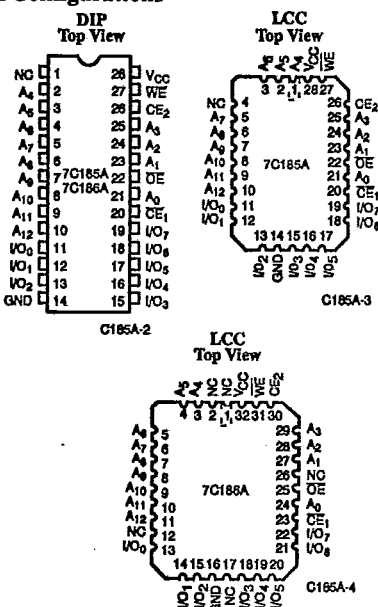
Writing to the device is accomplished when the chip enable one ($\overline{CE}_1$) and write

enable ($\overline{WE}$) inputs are both LOW, and the chip enable two (CE_2) input is HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{12}).

Reading the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW, while taking write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the I/O pins.

The I/O pins remain in high-impedance state when chip enable one ($\overline{CE}_1$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or chip enable two (CE_2) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram**Pin Configurations****Selection Guide^[1]**

		7C185A-12 7C186A-12	7C185A-15 7C186A-15	7C185A-20 7C186A-20	7C185A-25 7C186A-25	7C185A-35 7C186A-35	7C185A-45 7C186A-45	7C185A-55 7C186A-55
Maximum Access Time (ns)		12	15	20	25	35	45	55
Maximum Operating Current (mA)	Military	180	170	135	125	125	125	125
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	40/20	30/20	30/20	30/20

Shaded area contains advanced information.

Notes:

1. For commercial specifications, see the CY7C185/6 datasheet.



T-46-23-12

CY7C185A
CY7C186A**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to +150°C
Ambient Temperature with Power Applied	- 55°C to +125°C
Supply Voltage to Ground Potential (Pin 28 to Pin 14)	- 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	- 0.5V to +7.0V
DC Input Voltage	- 3.0V to +7.0V

Output Current into Outputs (Low)	20 mA
Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Military ^[2]	- 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameters	Description	Test Conditions	7C185A-12 7C186A-12		7C185A-15 7C186A-15		7C185A-20 7C186A-20		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[4]		-0.5	0.8	-0.5	0.8	-3.0	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max. I _{OUT} = 0 mA		180		170		135	mA
I _{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{IH}$, Min. Duty Cycle = 100%		40		40		40	mA
I _{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≥ 0.3V		20		20		20	mA

Shaded area contains advanced information.

Notes:

- ¹ T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- V_{IL} (min.) = -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.



SRAMS



CY7C185A
CY7C186A

T-46-23-12

Electrical Characteristics Over the Operating Range^[3] (continued)

Parameters	Description	Test Conditions	7C185A-25 7C186A-25		7C185A-35, 45, 55 7C186A-35, 45, 55		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[4]		-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		125		125	mA
I _{SB1}	Automatic CE ₁ Power-Down Current	Max. V _{CC} , CE ₁ ≥ V _{IH} , Min. Duty Cycle = 100%		40		30	mA
I _{SB2}	Automatic CE ₁ Power-Down Current	Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≥ 0.3V		20		20	mA

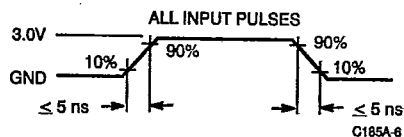
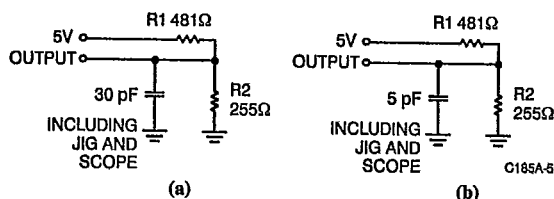
Capacitance^[6]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

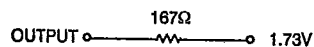
Notes:

6. Tested initially and after may design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT





T-46-23-12

CY7C185A
CY7C186A

Switching Characteristics Over the Operating Range^[2, 7]

Parameters	Description	7C185A–12 7C186A–12		7C185A–15 7C186A–15		7C185A–20 7C186A–20		7C185A–25 7C186A–25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	12		15		20		25		ns
t _{AA}	Address to Data Valid		12		15		20		25	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		ns
t _{ACE1}	$\overline{CE}_1$ LOW to Data Valid		12		15		20		25	ns
t _{ACE2}	CE_2 HIGH to Data Valid		12		15		20		25	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		10		12	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		3		3		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[8]		7		8		8		10	ns
t _{LZCE1}	$\overline{CE}_1$ LOW to Low Z ^[9]	3		3		5		5		ns
t _{LZCE2}	CE_2 HIGH to Low Z	3		3		3		3		ns
t _{HZCE}	$\overline{CE}_1$ HIGH to High Z ^[8, 9] CE_2 LOW to High Z		7		8		8		10	ns
t _{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		ns
t _{PD}	$\overline{CE}_1$ HIGH to Power-Down		12		15		20		20	ns
WRITE CYCLE ^[10]										
t _{WC}	Write Cycle Time	12		15		20		20		ns
t _{SCE1}	$\overline{CE}_1$ LOW to Write End	8		10		15		20		ns
t _{SCE2}	CE_2 HIGH to Write End	8		10		15		20		ns
t _{AW}	Address Set-Up to Write End	9		10		15		20		ns
t _{HA}	Address Hold from Write End	0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	8		10		15		15		ns
t _{SD}	Data Set-Up to Write End	6		7		10		10		ns
t _{HD}	Data Hold from Write End	0		0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[8]		6		7		7		7	ns

Shaded area contains advanced information.

- Notes:
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
 - t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
 - At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
 - Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$. $CE_2 = V_{IH}$.



SRAMs



T-46-23-12

CY7C185A
CY7C186A
Switching Characteristics Over the Operating Range^{1, 7} (continued)

Parameters	Description	7C185A-35 7C186A-35		7C185A-45 7C186A-45		7C185A-55 7C186A-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	35		45		55		ns
t _{AA}	Address to Data Valid		35		45		55	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE1}	$\overline{CE}_1$ LOW to Data Valid		35		45		55	ns
t _{ACE2}	CE ₂ HIGH to Data Valid		25		30		40	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[8]		12		15		20	ns
t _{LZCE1}	$\overline{CE}_1$ LOW to Low Z ^[9]	5		5		5		ns
t _{LZCE2}	CE ₂ HIGH to Low Z	3		3		3		ns
t _{HZCE}	$\overline{CE}_1$ HIGH to High Z ^[8, 9] CE ₂ LOW to High Z		15		15		20	ns
t _{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		ns
t _{PD}	$\overline{CE}_1$ HIGH to Power-Down		20		25		25	ns
WRITE CYCLE ^[10]								
t _{WC}	Write Cycle Time	25		40		50		ns
t _{SCE1}	$\overline{CE}_1$ LOW to Write End	25		30		40		ns
t _{SCE2}	CE ₂ HIGH to Write End	20		25		30		ns
t _{AW}	Address Set-Up to Write End	25		30		40		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	20		20		25		ns
t _{SD}	Data Set-Up to Write End	15		15		25		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[8]		10		15		20	ns

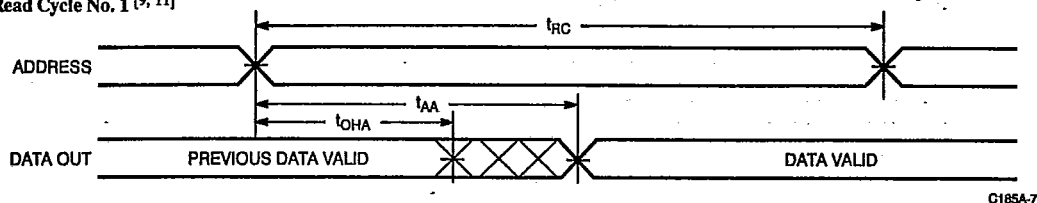


CY7C185A
CY7C186A

T-46-23-12

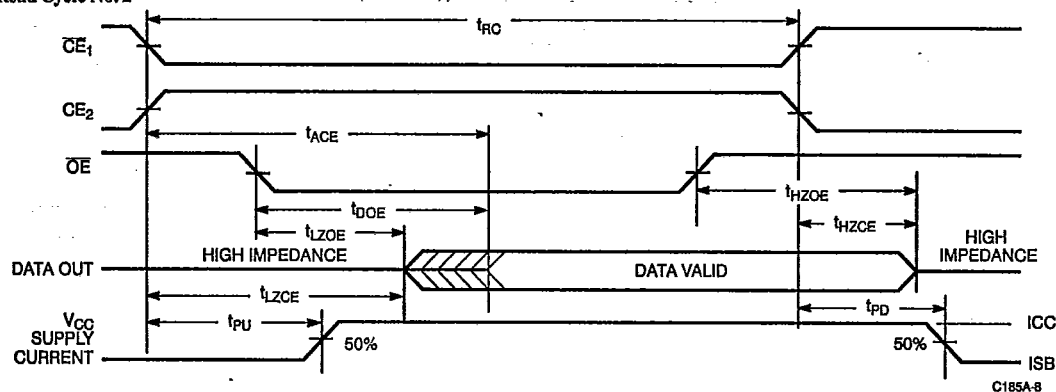
Switching Waveforms

Read Cycle No. 1 [9, 11]



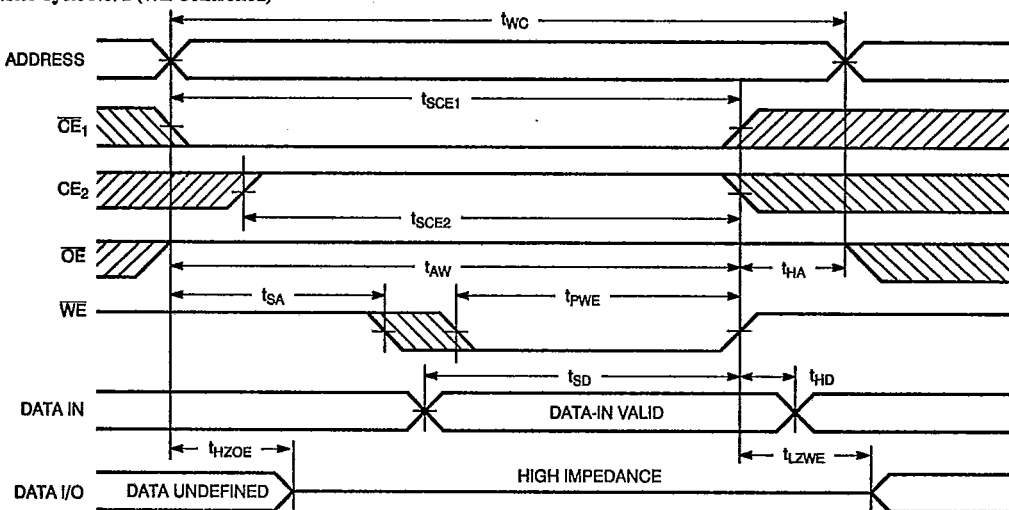
C185A-7

Read Cycle No. 2 [11, 12]



C185A-8

Write Cycle No. 1 (WE Controlled) [13, 14]



C185A-9

Notes:

11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.12. $\overline{WE}$ is HIGH for read cycle.13. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ HIGH, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.14. Data I/O is high impedance if $OE = V_{IH}$.

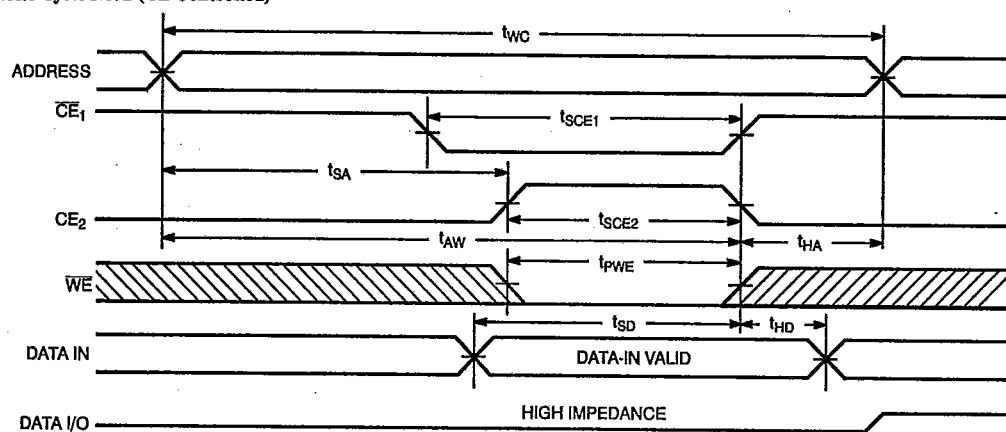
2
SRAMS



T-46-23-12

CY7C185A
CY7C186A

Switching Waveforms (continued)

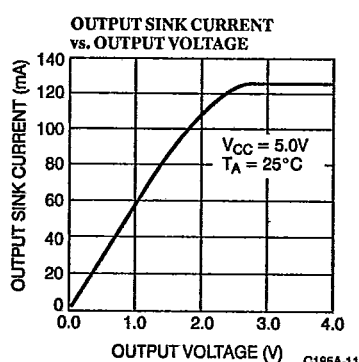
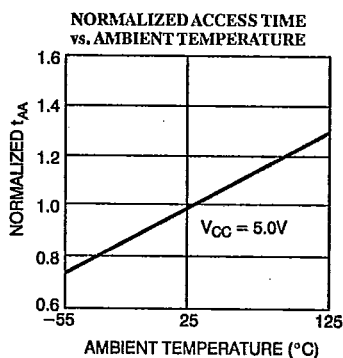
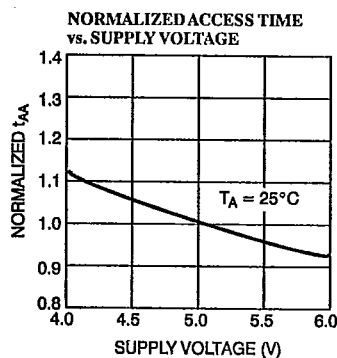
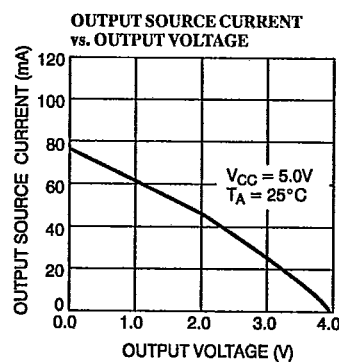
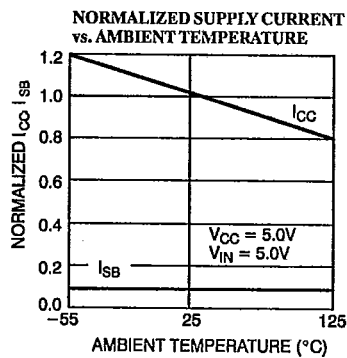
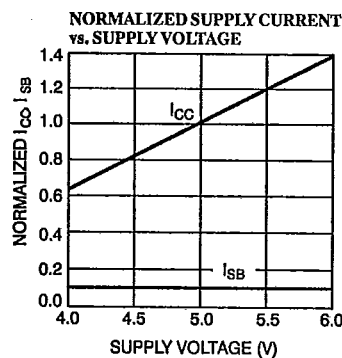
Write Cycle No. 2 ($\overline{CE}$ Controlled) [13, 14, 15]

C185A-10

Notes:

15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics



C185A-11

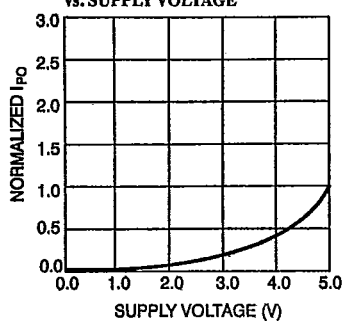
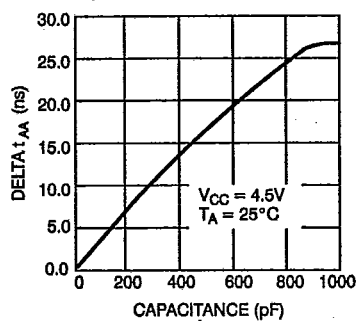
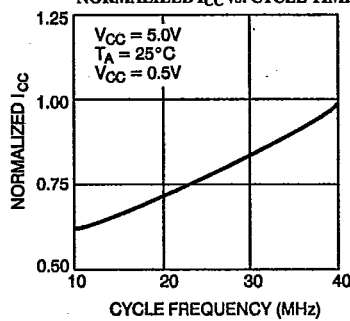
CYPRESS
SEMICONDUCTOR

T-46-23-12

CY7C185A

CY7C186A

Typical DC and AC Characteristics (continued)

TYPICAL POWER-ON CURRENT
vs. SUPPLY VOLTAGETYPICAL ACCESS TIME CHANGE
vs. OUTPUT LOADINGNORMALIZED I_{CC} vs. CYCLE TIME

C185A-12



SRAMs

Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24



T-46-23-12

CY7C185A
CY7C186A

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C185A-12DMB	D22	Military
	CY7C185A-12KMB	K74	
	CY7C185A-12LMB	L54	
15	CY7C185A-15DMB	D22	Military
	CY7C185A-15KMB	K74	
	CY7C185A-15LMB	L54	
20	CY7C185A-20DMB	D22	Military
	CY7C185A-20KMB	K74	
	CY7C185A-20LMB	L54	
25	CY7C185A-25DMB	D22	Military
	CY7C185A-25KMB	K74	
	CY7C185A-25LMB	L54	
35	CY7C185A-35DMB	D22	Military
	CY7C185A-35KMB	K74	
	CY7C185A-35LMB	L54	
45	CY7C185A-45DMB	D22	Military
	CY7C185A-45KMB	K74	
	CY7C185A-45LMB	L54	
55	CY7C185A-55DMB	D22	Military
	CY7C185A-55KMB	K74	
	CY7C185A-55LMB	L54	

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C186A-12DMB	D16	Military
	CY7C186A-12LMB	L55	
15	CY7C186A-15DMB	D16	Military
	CY7C186A-15LMB	L55	
20	CY7C186A-20DMB	D16	Military
	CY7C186A-20LMB	L55	
25	CY7C186A-25DMB	D16	Military
	CY7C186A-25LMB	L55	
35	CY7C186A-35DMB	D16	Military
	CY7C186A-35LMB	L55	
45	CY7C186A-45DMB	D16	Military
	CY7C186A-45LMB	L55	
55	CY7C186A-55DMB	D16	Military
	CY7C186A-55LMB	L55	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{TX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{OS}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE1}	7, 8, 9, 10, 11
t _{ACE2}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE1}	7, 8, 9, 10, 11
t _{SCE2}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Document #: 38-00114-A