NEC®

9 GHz DIVIDE-BY-2 DYNAMIC PRESCALER

UPG504B UPG504P

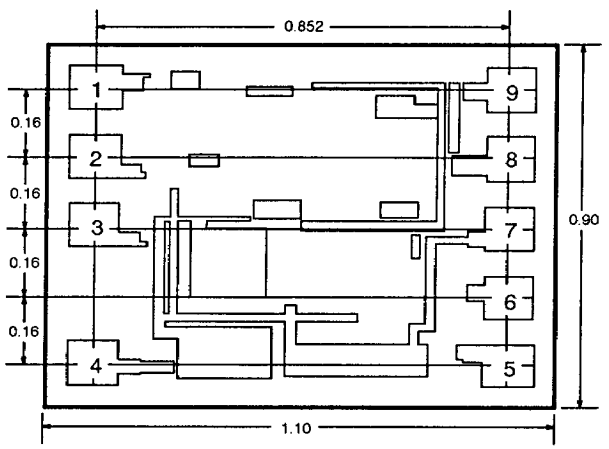
FEATURES

- **WIDE OPERATING FREQUENCY RANGE:** f_{IN} = 2.0 to 9.0 GHz (T_A = 25°C)
- **LOW POWER DISSIPATION**
- **DIVISION RATIO OF 2**
- **GUARANTEED OPERATING TEMPERATURE OVER AN AMBIENT RANGE OF -25°C TO +75°C**

DESCRIPTION AND APPLICATIONS

The UPG504B/P is a GaAs divide-by-2 prescaler that is capable of operating up to 9 GHz. It is designed as the prescaler in the frequency synthesizers of microwave communication systems and measurement equipment. The UPG504B/P is a dynamic divider. This device employs buffered FET logic (BFL). It is housed in a hermetic 8-lead ceramic flat package that is easy to install and reliable under harsh environments.

UPG504B (CHIP)
t = 0.14



1. IN	4. V_{SS2}	7. V_{SS1}
2. GND	5 GND	8. V_{DD}
3. V_{GG}	6. OUT	9. GND

RECOMMENDED CHIP ASSEMBLY CONDITIONS

Die Attachment
- Atmosphere: N_2 gas
- Temperature: 320 ± 3°C
- AuSn Preform: UPG504P 0.5 x 0.5 x 0.05t (mm), 1 piece

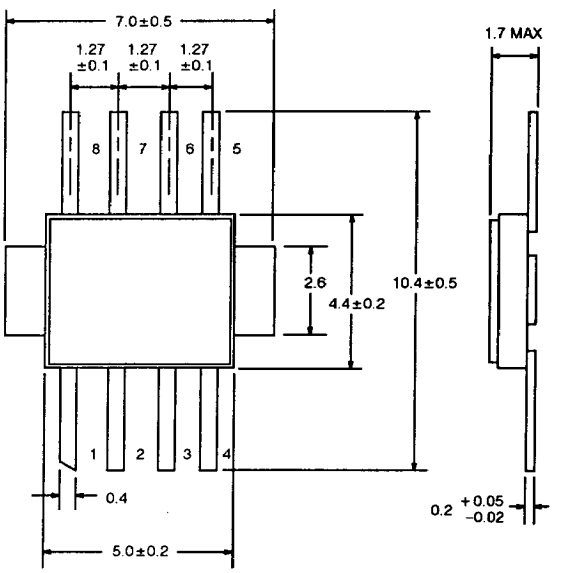
The hard solder such as AuSi or AuGe which has a higher melting point than AuSn should not be used.

Base material: CuW, Cu, KV
Epoxy Die Attach is not recommended.

Bonding:
- Machine: TCB
- Wire: 30 µm diameter Au wire
- Temperature: 260 ± 10°C
- Strength: 44 ± 5g
- Atmosphere: N_2 gas

OUTLINE DIMENSIONS (Units in mm)

OUTLINE BF08



PIN CONNECTIONS
1. Output
2. V_{SS1}
3. NC*
4. V_{DD}
5. Input
6. NC
7. V_{GG}**
8. V_{SS2}

FLANGE : GND

*Non Connection
**Normally open. This Terminal can be used to suppress self-oscillation.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DD}	Supply Voltage	V	+5
V_{SS2}	Supply Voltage	V	-5
P_{IN}	Input Power Level	dBm	+13
P_T	Total Power Dissipation	W	1.5
T_{STG}	Storage Temperature	°C	-65 to +175
T_C	Case Temperature	°C	-65 to +125

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PART NUMBER PACKAGE OUTLINE			UPG504B, UPG504P BF08		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I_{DD}	Supply Current at V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V	mA	38	55	78
I_{SS1}	Supply Current at V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V	mA	18	20	24
I_{SS2}	Supply Current at V_{DD} = 3.8 V, V_{SSI} = 0 V, V_{SS2} = -2.2 V	mA	20	35	54
$f_{IN(U)}$	Upper Limit of Input Frequency at V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V, P_{IN} = +9 to +10 dBm	GHz	8.6	9	
$f_{IN(L)}$	Lower Limit of Input Frequency at V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V, P_{IN} = +9 to +10 dBm	GHz		2	2.2
P_{IN}	Input Power at V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V, f_{IN} = 2.2 to 8.6 GHz f_{IN} = 5.0 to 7.4 GHz	 dBm dBm	 +9 +3		 +10 +10
P_{OUT}	Output Power at V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V, f_{IN} = 8.0 GHz, P_{IN} = +10 dBm f_{IN} = 2.2 GHz, P_{IN} = +10 dBm	 dBm dBm	 -3 0	 +2	

ELECTRICAL CHARACTERISTICS (T_A = -25 to +75°C)

PART NUMBER PACKAGE OUTLINE			UPG504B, UPG504P BF08		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I_{DD}	Supply Current at V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V	mA		55	
I_{SS1}	Supply Current at V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V	mA		20	
I_{SS2}	Supply Current at V_{DD} = 3.8 V, V_{SSI} = 0 V, V_{SS2} = -2.2 V	mA		35	
$f_{IN(U)}$	Upper Limit of Input Frequency at V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V, P_{IN} = +9 to +10 dBm	GHz	8.0	8.4	
$f_{IN(L)}$	Lower Limit of Input Frequency at V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V, P_{IN} = +9 to +10 dBm	GHz		2.3	2.5
P_{IN}	Input Power at V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V, f_{IN} = 2.5 to 8.0 GHz f_{IN} = 5.0 to 7.0 GHz	 dBm dBm	 +9 +4		 +10 +10
P_{OUT}	Output Power at V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V, f_{IN} = 8.0 GHz, P_{IN} = +10 dBm f_{IN} = 2.5 GHz, P_{IN} = +10 dBm	 dBm dBm	 -4 -1	 -1 +1	

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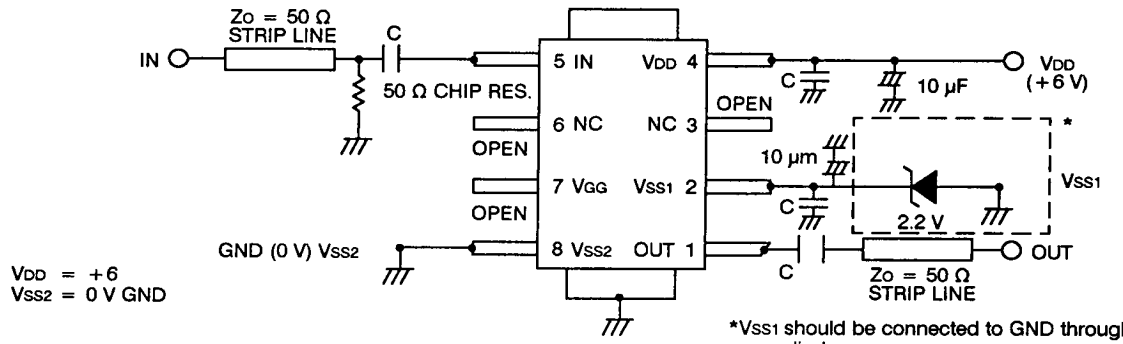
POWER SUPPLY CONFIGURATIONS (V_{GG1} and V_{GG2} are normally open)

C: 1000-5000 pF CHIP CAPACITOR

CONFIGURATION 1



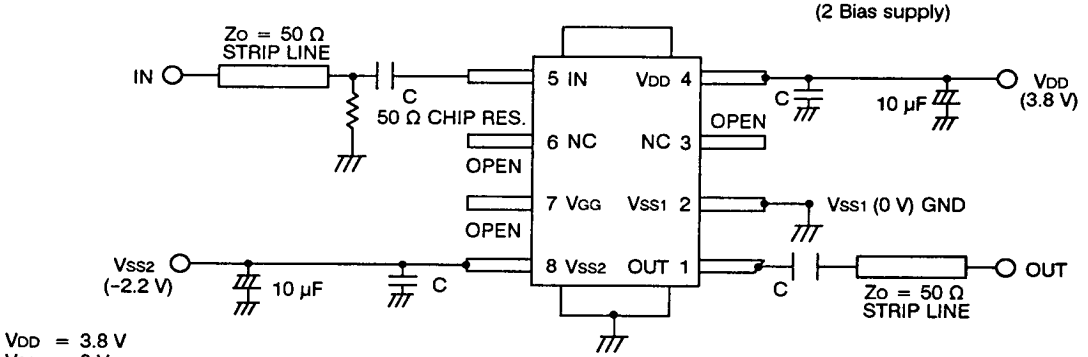
V_{DD} = +6
V_{SS2} = 0 V GND

*V_{SS1} should be connected to GND through a 2.2 V zener diode.

C: 1000-5000 pF CHIP CAPACITOR

CONFIGURATION 2

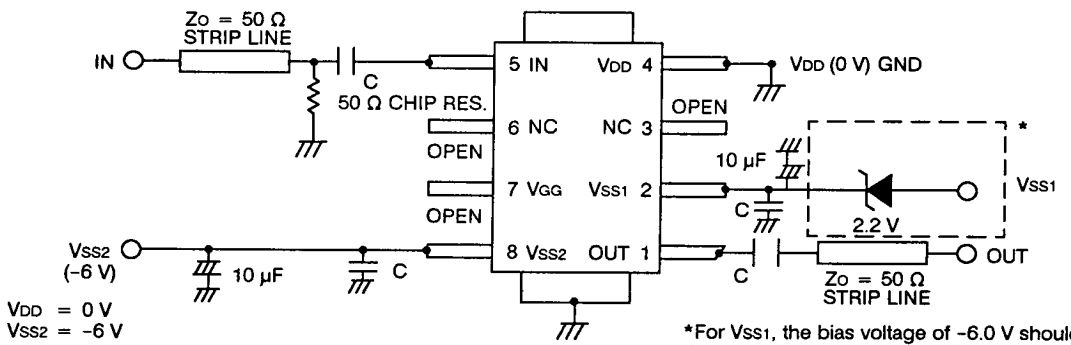
(2 Bias supply)



V_{DD} = 3.8 V
V_{SS1} = 0 V
V_{SS2} = -2.2 V

C: 1000-5000 pF CHIP CAPACITOR

CONFIGURATION 3



V_{DD} = 0 V
V_{SS2} = -6 V

*For V_{SS1}, the bias voltage of -6.0 V should be applied through a 2.2 V zener diode.

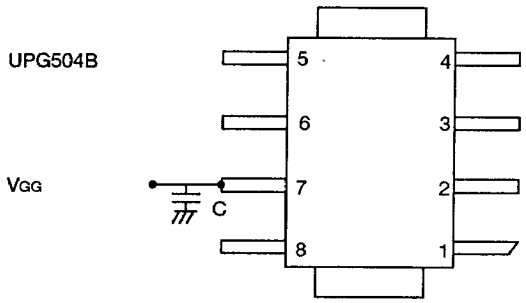
POWER SUPPLY CONFIGURATIONS

SELF OSCILLATION

1. To prevent self oscillation of UPG504B, V_{GG} is used. When you apply -9 V to V_{GG} self oscillation of UPG504B will stop.
   (V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V).
   Also a chip capacitor should be used. Please refer to the figure below.

C: 1000-5000 pF CHIP CAPACITOR

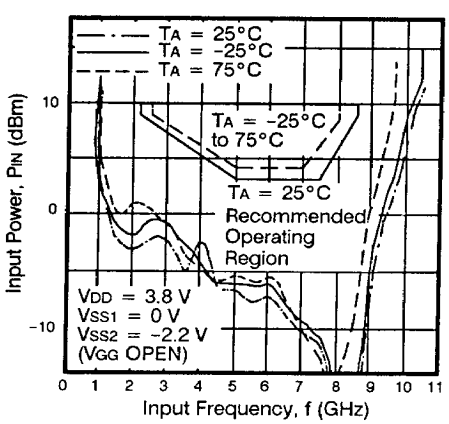
CONFIGURATION 4



When used in a PLL synthesizer application use the 50 Ω chip resistor and 10 μF capacitor shown in configurations, 1, 2 and 3. These resistors and capacitors may not be required if only used for counter applications.

TYPICAL INPUT SENSITIVITY CURVE (T_A = 25°C)

INPUT POWER AND OUTPUT POWER vs. FREQUENCY



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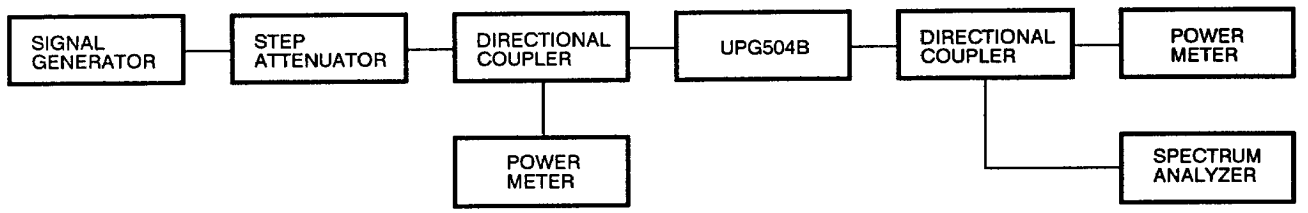
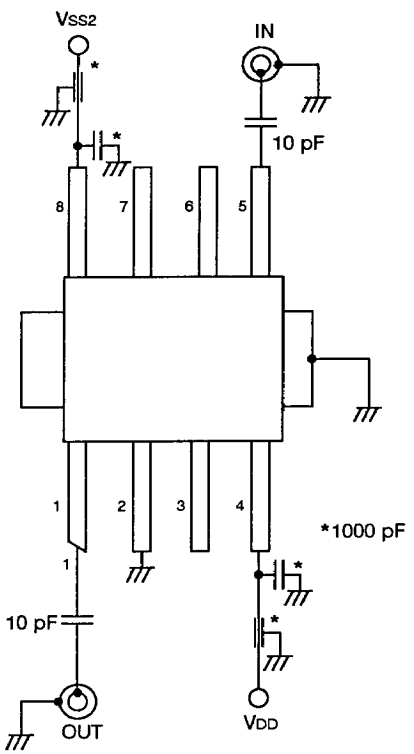
TEST CIRCUIT BLOCK DIAGRAM



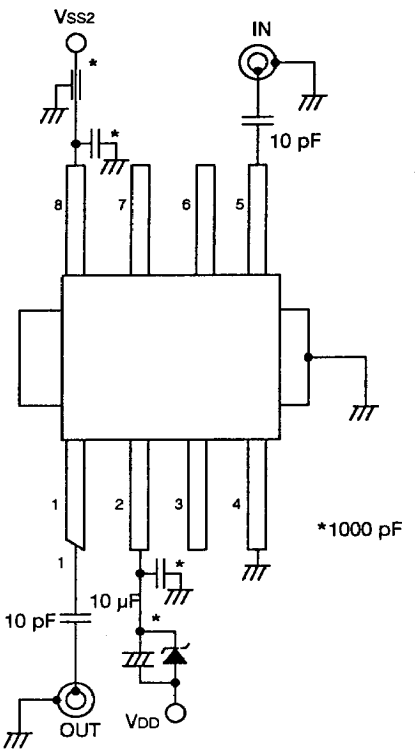
TEST CIRCUIT

2 Bias Supply



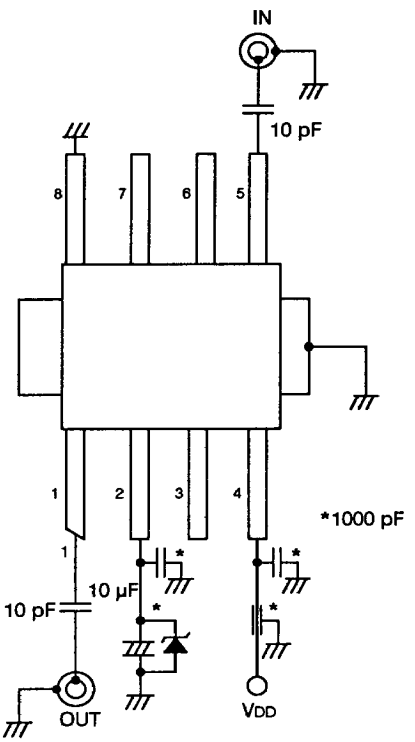
VDD = +3.8 V
VSS1 = GND
VSS2 = -2.2 V

Single Bias Supply



VDD = GND
VSS2 = -6.0 V

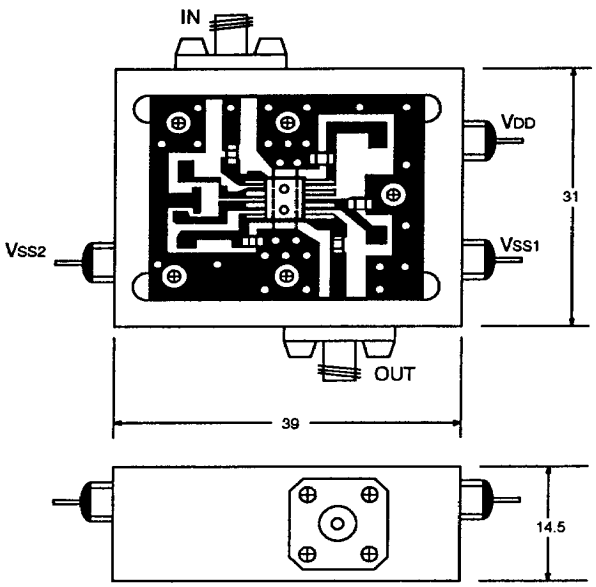
For VSS1, the bias voltage of -6.0 V should be applied through 2.2 V zener diode.



VDD = +6.0 V
VSS2 = GND

VSS1 should be connected to GND through 2.2 V zener diode.

TEST JIG DRAWING (Units in mm)



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