Quad, 15 V, 256-Position, Digital Potentiometer with Pin Selectable SPI/I²C

AD5263

FEATURES

256-position, 4-channel
End-to-end resistance 20 kΩ, 50 kΩ, 200 kΩ
Pin selectable SPI® or I²C® compatible interface
Power-on preset to midscale
Two package address decode pins AD0 and AD1
Rheostat mode temperature coefficient 30 ppm/°C
Voltage divider temperature coefficient 5 ppm/°C
Wide operating temperature range –40°C to +125°C
5 V to 15 V single supply; ±5 V dual supply

APPLICATIONS

Mechanical potentiometer replacement
Optical network adjustment
Instrumentation: gain, offset adjustment
Stereo channel audio level control
Automotive electronics adjustment
Programmable power supply
Programmable filters, delays, time constants
Line impedance matching
Low resolution DAC/trimmer replacement
Base station power amp biasing
Sensor calibration

GENERAL DESCRIPTION

The AD5263 is the industry's first quad-channel, 256-position, digital potentiometer[1] with a selectable digital interface. This device performs the same electronic adjustment function as mechanical potentiometers or variable resistors, with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

Each channel of the AD5263 offers a completely programmable value of resistance between the A terminal and the wiper, or between the B terminal and the wiper. The fixed A-to-B terminal resistance of 20 kΩ, 50 kΩ, or 200 kΩ has a nominal temperature coefficient of ±30 ppm/°C and a ±1% channel-to-channel matching tolerance. Another key feature of this part is the ability to operate from +4.5 V to +15 V, or at ±5 V.

Wiper position programming presets to midscale upon power-on. Once powered, the VR wiper position is programmed by either the 3-wire SPI or 2-wire I²C compatible interface. In the I²C mode, additional programmable logic outputs enable users to drive digital loads, logic gates, and analog switches in their systems.

The AD5263 is available in a narrow body TSSOP-24. All parts are guaranteed to operate over the automotive temperature range of –40°C to +125°C.

For single- or dual-channel applications, refer to the AD5260/AD5280 or AD5262/AD5282.

FUNCTIONAL BLOCK DIAGRAM

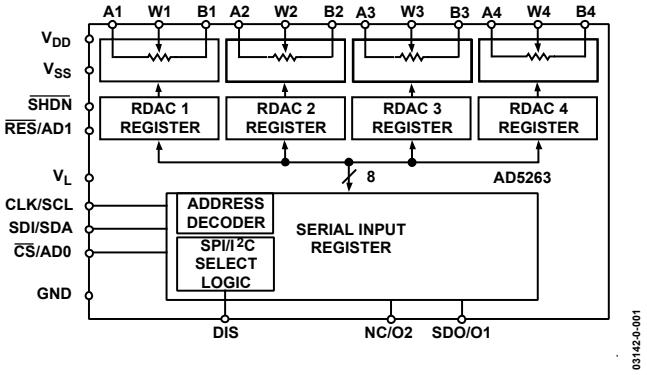

Figure 1.

[1] The terms *digital potentiometer*, *VR*, and *RDAC* are used interchangeably.

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS—20 kΩ, 50 kΩ, 200 kΩ VERSIONS

(V_{DD} = +5 V, V_{SS} = −5 V, V_L = +5 V, V_A = +V_{DD}, V_B = 0 V, −40°C < T_A < +125°C, unless otherwise noted.)

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE (Specifications apply to all VRs.)						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A=NC	−1	±1/4	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A=NC	−1	±1/2	+1	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−30		30	%
Resistance Mode Temperature Coefficient	$\Delta R_{WB}/\Delta T$			30		ppm/°C
	$\Delta R_{WA}/\Delta T$			30		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R_{AB}		60	150	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs.)						
Resolution	N				8	Bits
Differential Nonlinearity[4]	DNL		−1	±1/4	+1	LSB
Integral Nonlinearity[4]	INL		−1	±1/2	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x80		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−2	−1	+0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	+1	+2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		V_{SS}		V_{DD}	V
Capacitance[6] Ax, Bx	$C_{A,B}$	f = 1 MHz, measured to GND, Code = 0x80		25		pF
Capacitance[6] Wx	C_W	f = 1 MHz, measured to GND, Code = 0x80		55		pF
Common-Mode Leakage	I_{CM}	V_A = V_B = V_{DD}/2		1		nA
Shutdown Current[7]	I_{SHDN}			0.02	5	µA
DIGITAL INPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High (SDA and SCL)	V_{IH}	V_{SS} = 0 V	0.7 × V_L		V_L + 0.5	V
Input Logic Low (SDA and SCL)	V_{IL}	V_{SS} = 0 V	−0.5		0.3 × V_L	V
Input Current	I_{IL}	V_{IN} = 0 V or +5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
DIGITAL OUTPUTS						
SDA	V_{OL}	I_{SINK} = 3 mA			0.4	V
	V_{OL}	I_{SINK} = 6 mA			0.6	V
O1, O2	V_{OH}	I_{SOURCE} = 40 µA	4			V
O1, O2	V_{OL}	I_{SINK} = 1.6 mA			0.4	V
SDO	V_{OH}	R_L = 2.2 kΩ to V_{DD}	V_{DD} − 0.1			V
SDO	V_{OL}	I_{SINK} = 3 mA			0.4	V
Three-State Leakage Current	I_{OZ}	V_{IN} = 0 V or +5 V			±1	µA
Output Capacitance[6]	C_{OZ}			3	8	pF
POWER SUPPLIES						
Logic Supply[8]	V_L		2.7		5.5	V
Power Single-Supply Range	$V_{DD\ RANGE}$	V_{SS} = 0 V	V_L		16.5	V
Power Dual-Supply Range	$V_{DD/SS\ RANGE}$		±4.5		±7.5	V
Logic Supply Current[9]	I_L	V_L = +5 V		25	60	µA
Positive Supply Current	I_{DD}	V_{IH} = +5 V or V_{IL} = 0 V			1	µA
Negative Supply Current	I_{SS}	V_{SS} = −5 V			1	µA
Power Dissipation[10]	P_{DISS}	V_{IH} = +5 V or V_{IL} = 0 V, V_{DD} = +5 V, V_{SS} = −5 V			0.6	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%		0.002	0.01	%/%
DYNAMIC CHARACTERISTICS[6, 11]						
Bandwidth (3 dB)	BW	R_{AB} = 20 kΩ/50 kΩ/200 kΩ		300/150/35		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 20 kΩ		0.05		%
V_W Settling Time[12]	t_S	V_A = 10 V, V_B = 0 V, ±1 LSB error band		2		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 10 kΩ, f = 1 kHz, RS = 0		9		nV/√Hz

TIMING CHARACTERISTICS—20 kΩ, 50 kΩ, 200 kΩ VERSIONS

(V_{DD} = +5 V, V_{SS} = −5 V, V_L = +5 V, V_A = $+V_{DD}$, V_B = 0 V, −40°C < T_A < +125°C unless otherwise noted.)

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
SPI INTERFACE TIMING CHARACTERISTICS (Specifications Apply to All Parts[6, 13])						
Clock Frequency	f_{CLK}				25	MHz
Input Clock Pulsewidth	t_{CH},t_{CL}	Clock level high or low	20			ns
Data Setup Time	t_{DS}		10			ns
Data Hold Time	t_{DH}		10			ns
$\overline{CS}$ Setup Time	t_{CSS}		15			ns
$\overline{CS}$ High Pulsewidth	t_{CSW}		20			ns
CLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		0			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns
Reset Pulsewidth	t_{RS}		5			ns
I²C INTERFACE TIMING CHARACTERISTICS (Specifications Apply to All Parts[6, 13])						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time between STOP and START	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated START)	t_2	After this period, the first clock pulse is generated.	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU;STA}$ Setup Time for START Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU;STO}$ Setup Time for STOP Condition	t_{10}		0.6			µs

NOTES

[1] Typicals represent average readings at 25°C and V_{DD} = +5 V, V_{SS} = −5 V.

[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. $I_W = V_{DD}/R$ for both V_{DD} = +5 V and V_{SS} = −5 V.

[3] $V_{AB} = V_{DD}$, Wiper (V_W) = no connect.

[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

[5] Resistor Terminals A, B, and W have no limitations on polarity with respect to each other.

[6] Guaranteed by design and not subject to production test.

[7] Measured at the Ax terminals. All Ax terminals are open circuited in shutdown mode.

[8] V_L is limited to V_{DD} or 5.5 V, whichever is less.

[9] Worst-case supply current consumed when all logic-input levels set at 2.4 V, standard characteristic of CMOS logic.

[10] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.

[11] All dynamic characteristics use V_{DD} = +5 V, V_{SS} = −5 V, V_L = +5 V.

[12] Settling time depends on value of V_{DD}, R_L, and C_L.

[13] See timing diagrams for location of measured values. All input control voltages are specified with $t_R = t_F$ = 2 ns (10% to 90% of +3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using V_L = +5 V.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

Table 3.

Parameter	Value
V_{DD} to GND	−0.3 V to +16.5 V
V_{SS} to GND	0 V to +7.5 V
V_{DD} to V_{SS}	+16.5 V
V_L to GND	−0.3 V to +6.5 V
V_A, V_B, V_W to GND	V_{SS} to V_{DD}
Terminal Current, Ax-Bx, Ax-Wx, Bx-Wx	
Pulsed[1]	±20 mA
Continuous	±3 mA
Digital Inputs and Output Voltage to GND	0 V to +7 V
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature ($T_{J\,MAX}$)	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Thermal Resistance[2] θ_{JA}	
TSSOP-24	143°C/W

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation: $(T_{JMAX} - T_A)/\theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

(R_{AB} = 20 kΩ unless otherwise noted.)

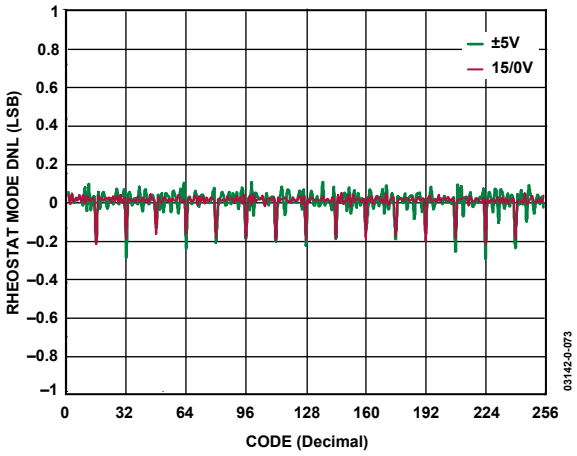

Figure 2. R-DNL vs. Code vs. Supply Voltage

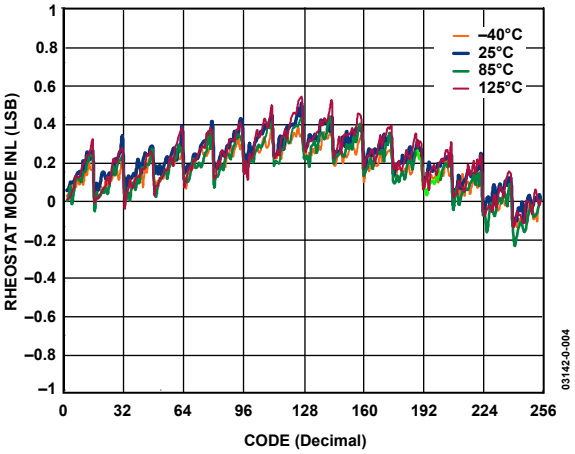

Figure 5. R-INL vs. Code; V_{DD} = ±5 V

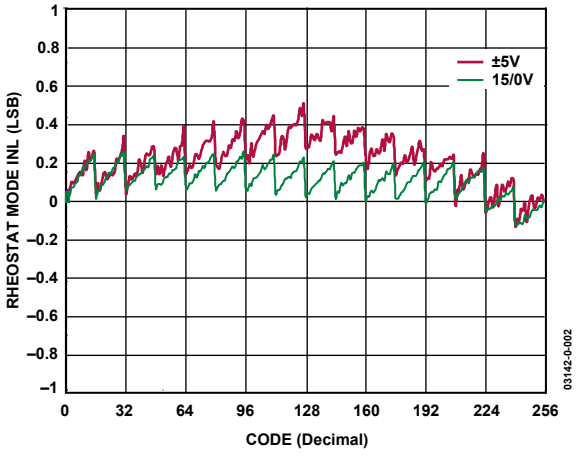

Figure 3. R-INL vs. Code vs. Supply Voltage

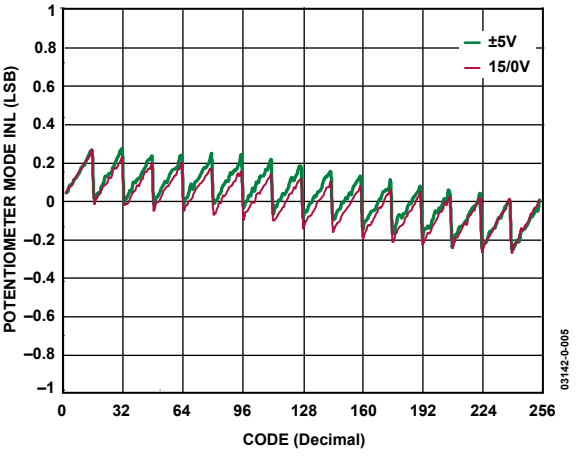

Figure 6. INL vs. Code vs. Supply Voltage

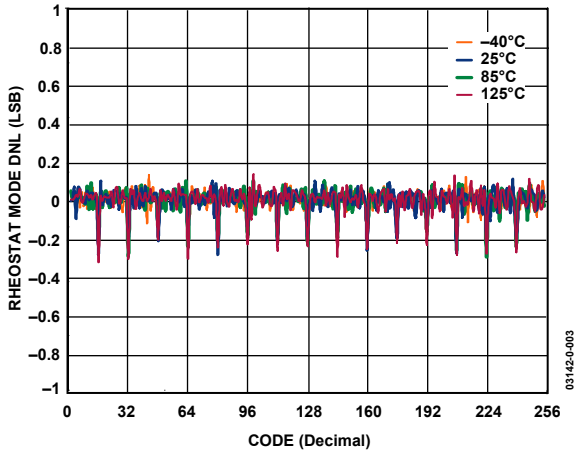

Figure 4. R-DNL vs. Code; V_{DD} = ±5 V

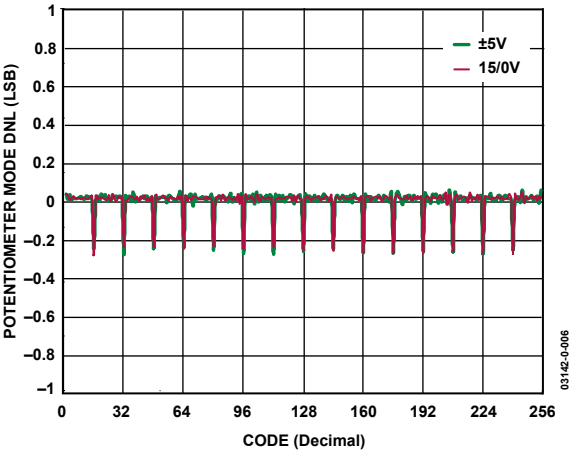

Figure 7. DNL vs. Code vs. Supply Voltage

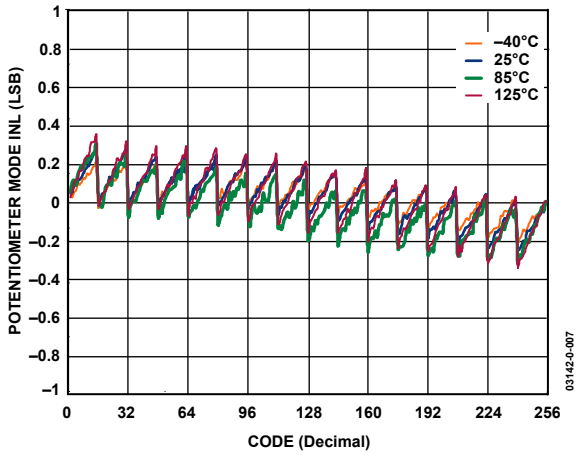

Figure 8. INL vs. Code; V_{DD} = ±5 V

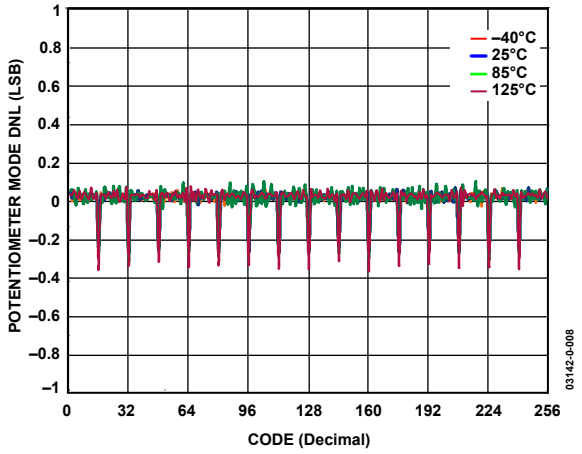

Figure 9. DNL vs. Code; V_{DD} = ±5 V

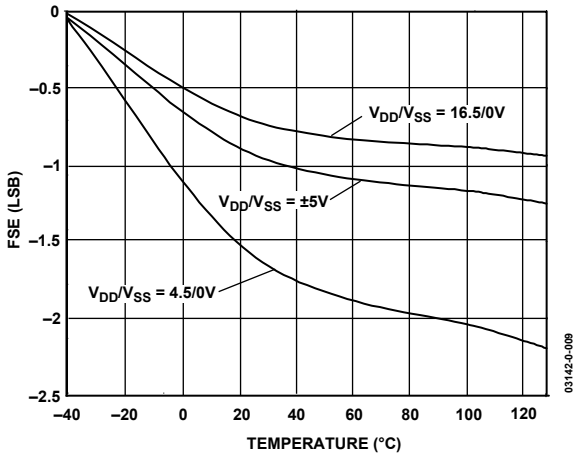

Figure 10. Full-Scale Error vs. Temperature

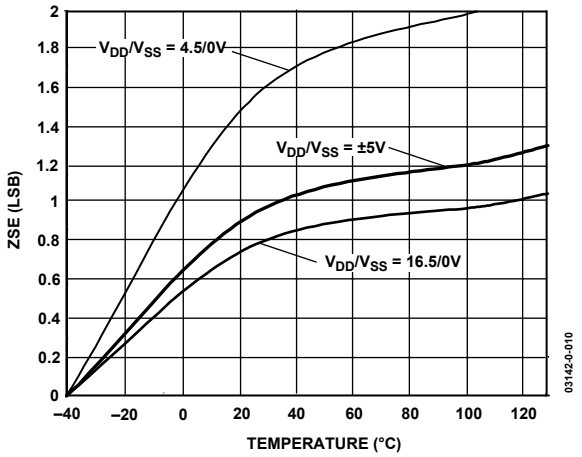

Figure 11. Zero-Scale Error vs. Temperature

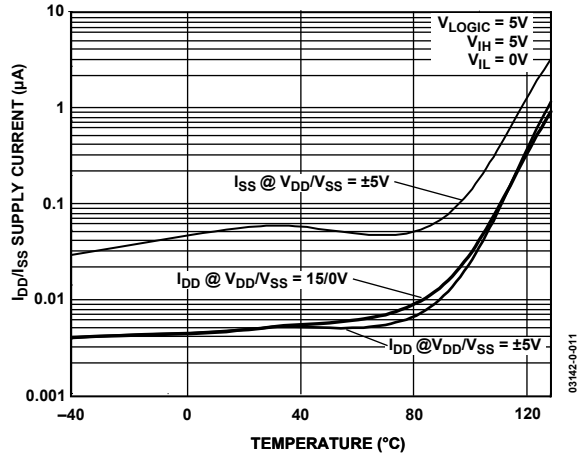

Figure 12. Supply Current vs. Temperature

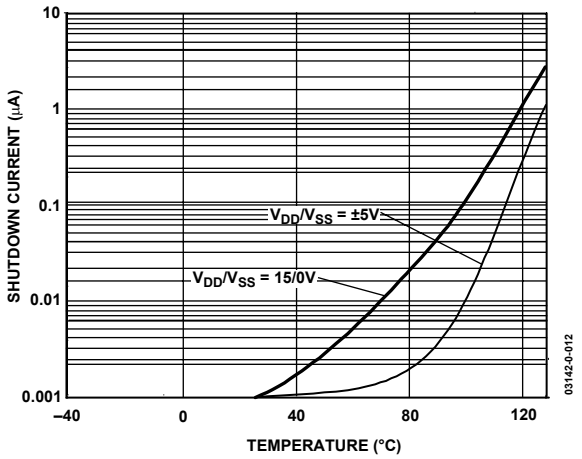

Figure 13. Shutdown Current vs. Temperature

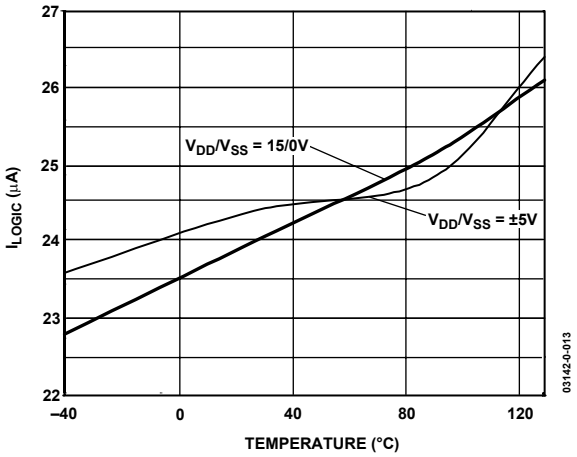

Figure 14. I_{LOGIC} vs. Temperature

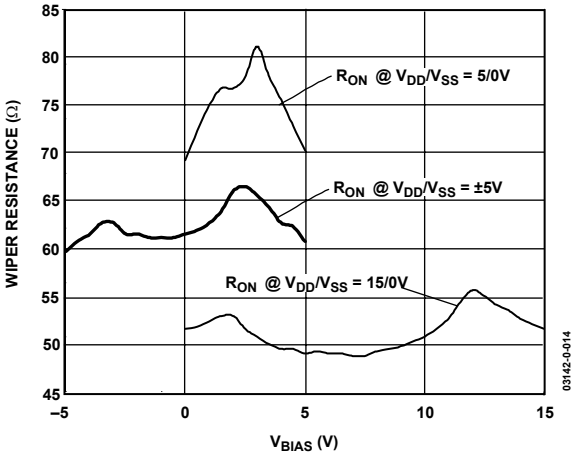

Figure 15. Wiper ON Resistance vs. Bias Voltage

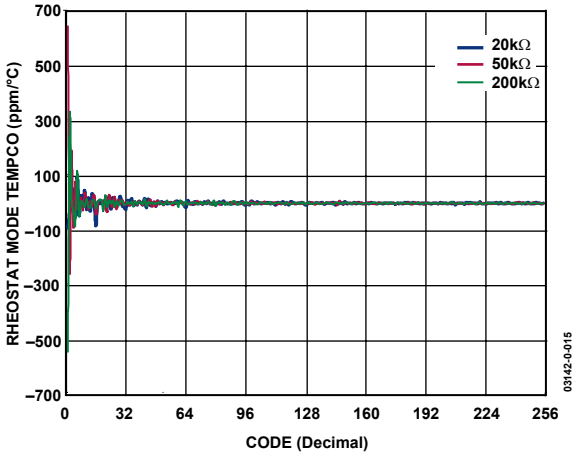

Figure 16. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

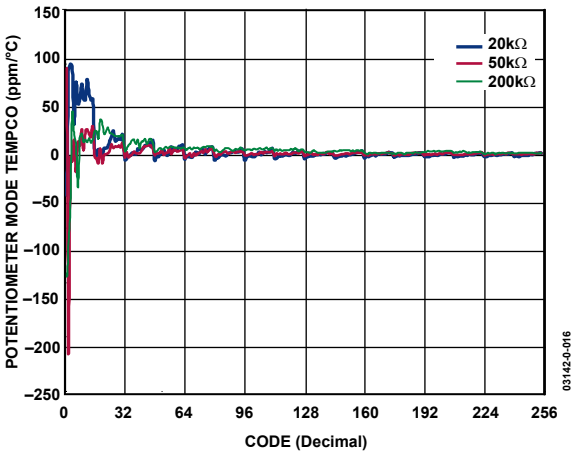

Figure 17. Potentiometer Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

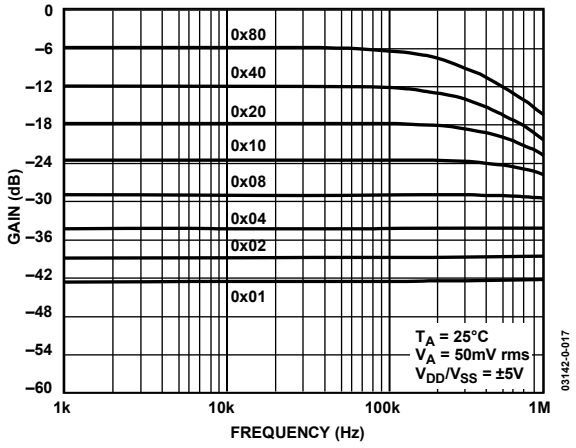

Figure 18. Gain vs. Frequency vs. Code; R_{AB} = 20 kΩ

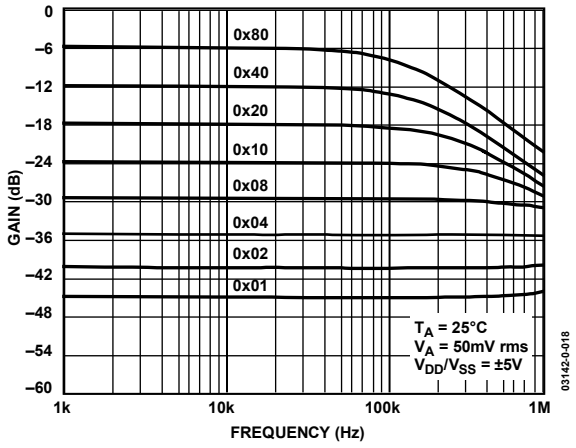

Figure 19. Gain vs. Frequency vs. Code; R_{AB} = 50 kΩ

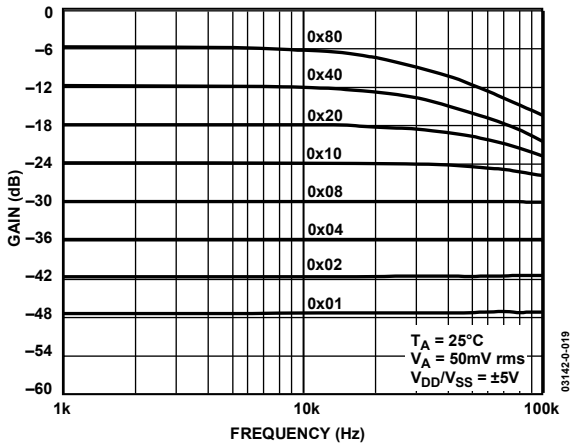

Figure 20. Gain vs. Frequency vs. Code; R_{AB} = 200 kΩ

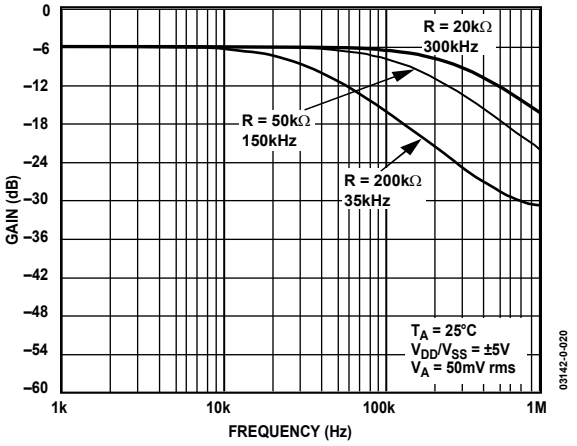

Figure 21. –3 db Bandwidth

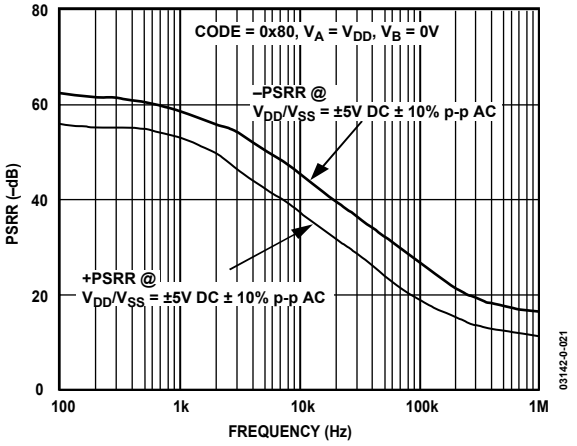

Figure 22. PSRR vs. Frequency

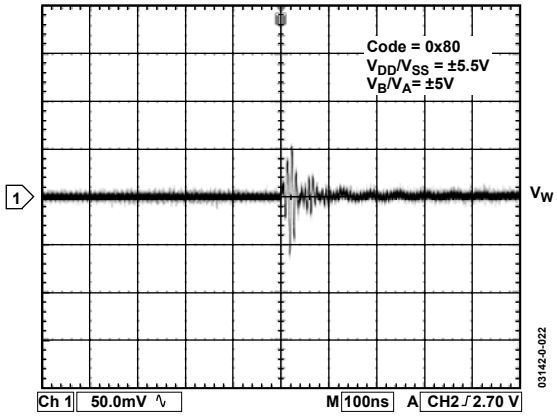

Figure 23. Digital Feedthrough

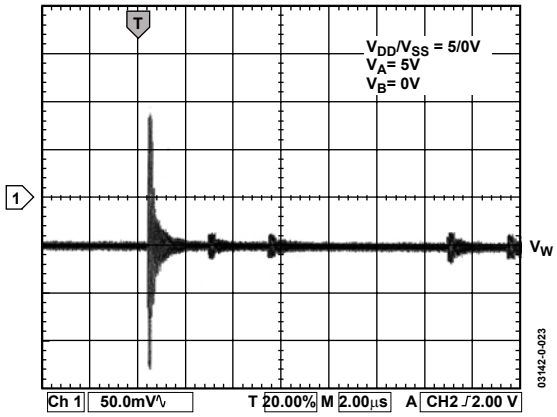

Figure 24. Midscale Glitch; Code 0x80–ox7F
(4.7 nF Capacitor Used from Wiper to Ground)

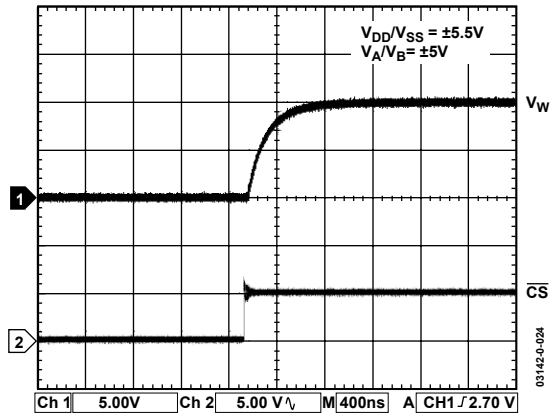

Figure 25. Large Signal Settling Time; Code 0x00–0xFF

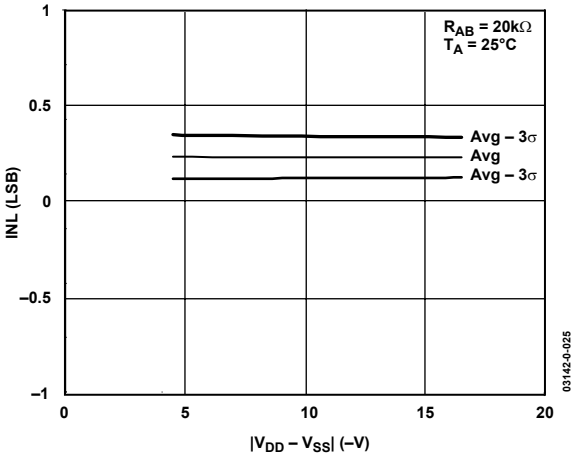

Figure 26. INL vs. Supply Voltage

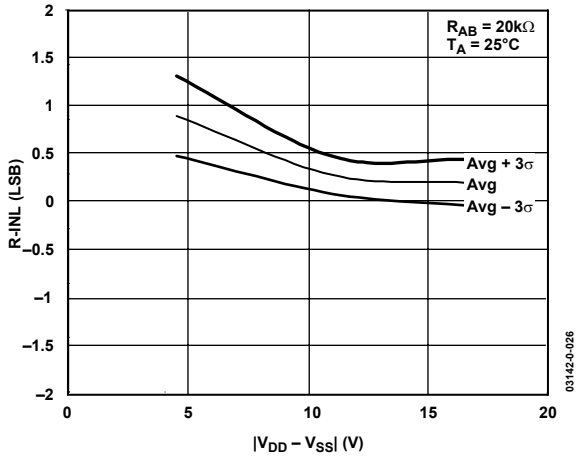

Figure 27. R-INL vs. Supply Voltage

TEST CIRCUITS

Figure 28 to Figure 38 define the test conditions used in the product specification table.

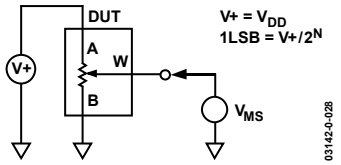

Figure 28. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

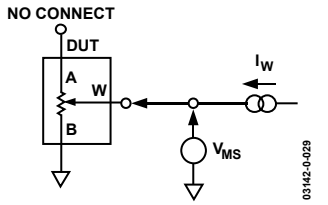

Figure 29. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

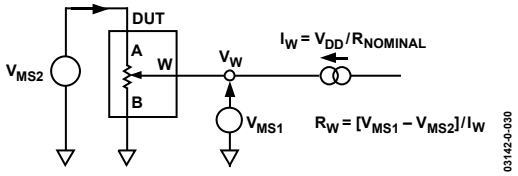

Figure 30. Test Circuit for Wiper Resistance

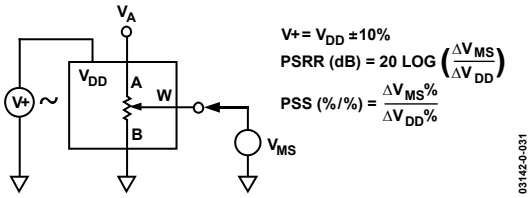

Figure 31. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

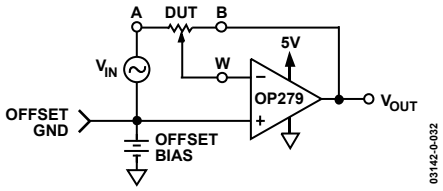

Figure 32. Test Circuit for Inverting Gain

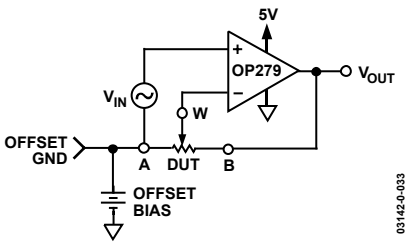

Figure 33. Test Circuit for Noninverting Gain

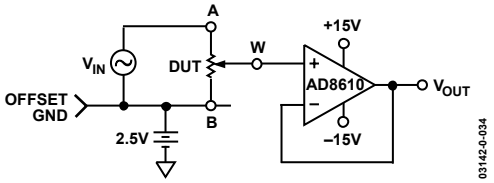

Figure 34. Test Circuit for Gain vs Frequency

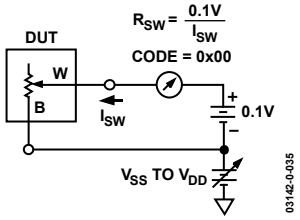

Figure 35. Test Circuit for Incremental ON Resistance

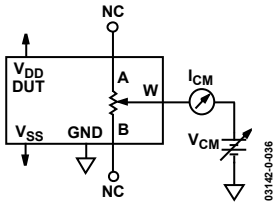

Figure 36. Test Circuit for Common Mode Leakage Current

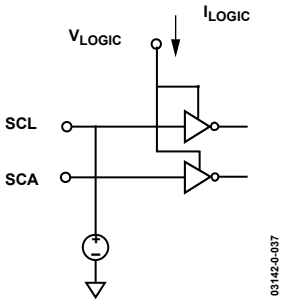

Figure 37. Test Circuit for V_{LOGIC} Current vs. Digital Input Voltage

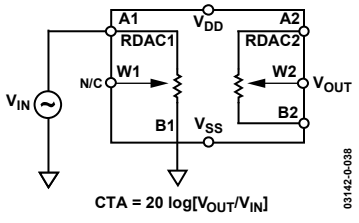

Figure 38. Test Circuit for Analog Crosstalk

SPI COMPATIBLE DIGITAL INTERFACE (DIS = 0)

Table 4. AD5263 Serial Data-Word Format

Addr		Data							
B9	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
		MSB							LSB
2^9		2^7							2^0

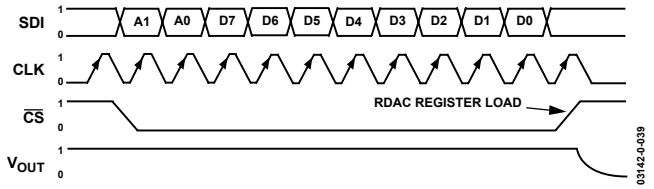

Figure 39. AD5263 Timing Diagram (V_A = 5 V, V_B = 0 V, $V_W = V_{OUT}$)

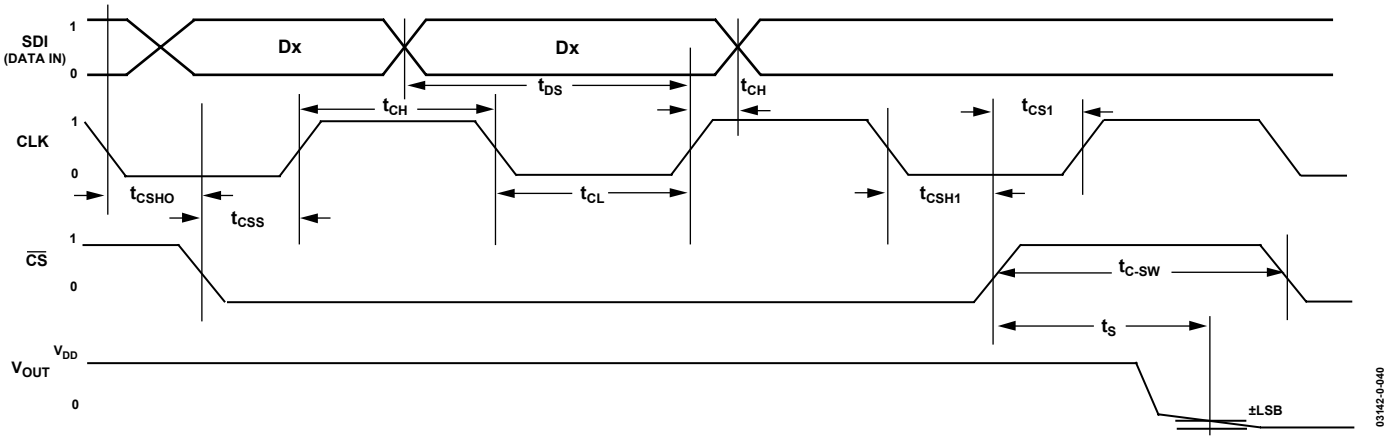

Figure 40. Detailed SPI Timing Diagram (V_A = 5 V, V_B = 0 V, $V_W = V_{OUT}$)

I²C COMPATIBLE DIGITAL INTERFACE (DIS = 1)

Table 5. I²C Write Mode Data-Word Format

S	0	1	0	1	1	AD1	AD0	$\overline{W}$	A	X	A1	A0	RS	SD	O1	O2	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

Table 6. I²C Read Mode Data-Word Format

S	0	1	0	1	1	AD1	AD0	R	A	D7	D8	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									

S = Start condition.
P = Stop condition.
A = Acknowledge.

AD1, AD0 = I²C device address bits. Must match with the logic states at pins AD1, AD0. Refer to Figure 48.

A1, A0 = RDAC channel select.

RS = Software reset wiper (A1, A0) to midscale position.

SD = Shutdown active high; ties wiper (A1, A0) to Terminal A, opens Terminal B, RDAC register contents are not disturbed. To exit shutdown, the command SD = 0 must be executed for each RDAC (A1, A0).

O1, O2 = Data to digital output pins O1, O2 in I²C mode, used to drive external logic. The logic high level is determined by V_L and the logic low level is GND.

$\overline{\mathbf{W}}$ = Write = 0.
R = Read = 1.

D7, D6, D5, D4, D3, D2, D1, D0 = Data Bits.

X = Don't Care.

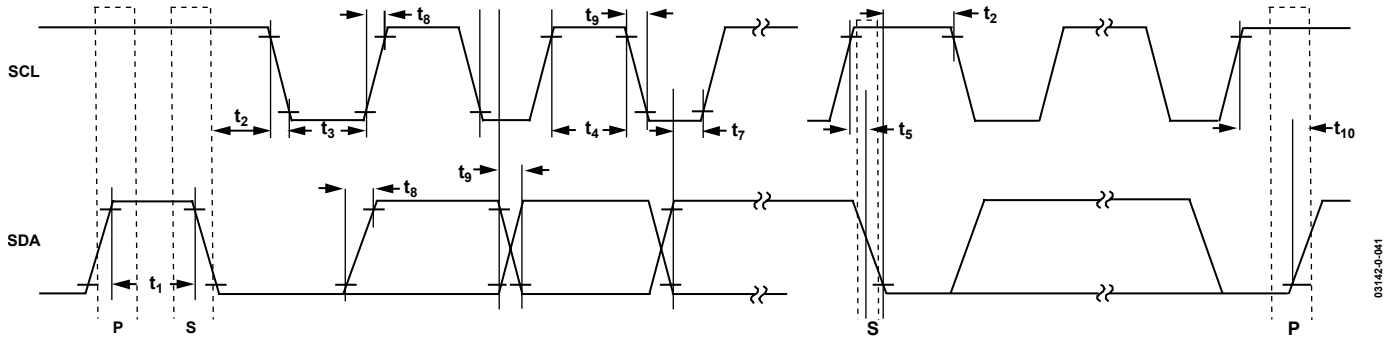

Figure 41. Detailed I²C Timing Diagram

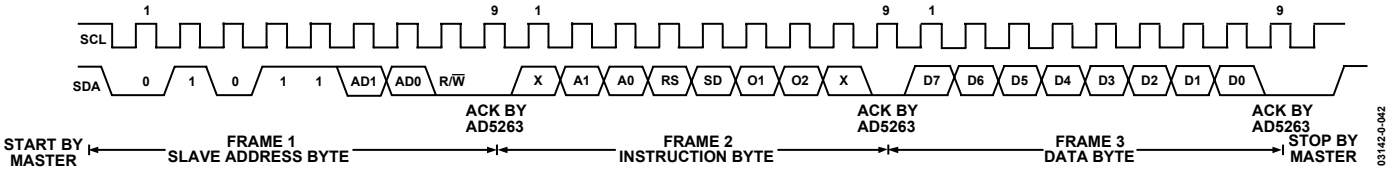

Figure 42. Writing to the RDAC Register

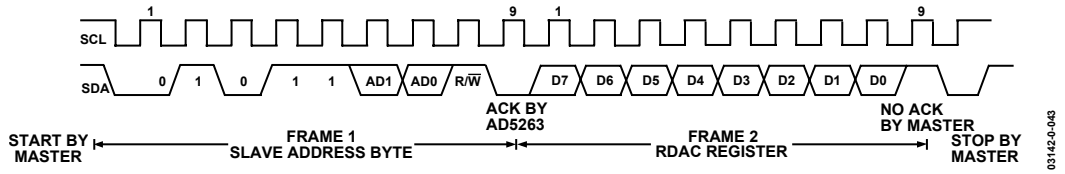

Figure 43. Reading Data from a Previously Selected RDAC Register in Write Mode

OPERATION

The AD5263 is a quad-channel, 256-position, digitally controlled, variable resistor (VR) device.

To program the VR settings, refer to the interface sections of the previous pages. The part has an internal power-on preset that places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up. In addition, the shutdown $\overline{SHDN}$ pin of AD5263 places the RDAC in an almost zero power consumption state where Terminal A is open circuited and the wiper W is connected to Terminal B, resulting in only leakage current consumption in the VR structure. During shutdown, the VR latch settings are maintained or new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting will be applied to the RDAC.

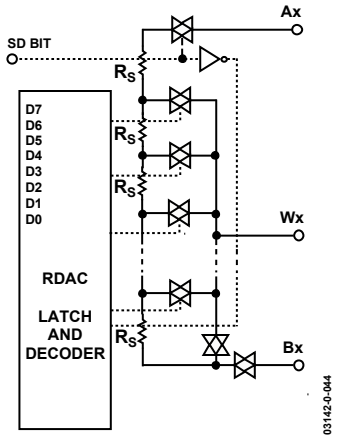

Figure 44. AD5263 Equivalent RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between Terminals A and B is available in 20 kΩ, 50 kΩ, and 200 kΩ. The final two or three digits of the part number determine the nominal resistance value, e.g., 20 kΩ = 20; 50 kΩ = 50; 200 kΩ = 200. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assuming a 20 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Since there is a 60 Ω wiper contact resistance, such a connection yields a minimum of 2 × 60 Ω resistance between Terminals W and B. The second connection is the first tap point, and corresponds to 198 Ω ($R_{WB} = R_{AB}/256 + R_W$ = 78 Ω + 2 × 60 Ω) for data 0x01. The third connection is the next tap point representing 216 Ω (R_{WB} = 78 Ω × 2 + 2 × 60 Ω) for data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 19,982 Ω (R_{AB} – 1 LSB + 2 × R_W). Figure 44 shows a simplified diagram of the equivalent RDAC circuit, where the last resistor string will not be accessed; therefore, there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

The general equation determining the digitally programmed output resistance between Terminals W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \quad (1)$$

where:

D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.

R_{AB} is the end-to-end resistance.

R_W is the wiper resistance contributed by the ON resistance of one internal switch.

In summary, if R_{AB} = 20 kΩ and the A terminal is open-circuited, the following RDAC latch codes result in the corresponding output resistance, R_{WB}.

Table 7. Codes and Corresponding R_{WB} Resistances

D (dec)	R_{WB} (Ω)	Output State
255	19,982	Full-Scale (R_{AB} – 1 LSB + R_W)
128	10,120	Midscale
1	198	1 LSB
0	120	Zero-Scale (Wiper Contact Resistance)

Note that in the zero-scale condition a finite wiper resistance of 120 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + 2 \times R_W \quad (2)$$

For R_{AB} = 20 kΩ and the B terminal open-circuited, the following RDAC latch codes result in the corresponding output resistance R_{WA}:

Table 8. Codes and Corresponding R_{WA} Resistances

D (dec)	R_{WA} (Ω)	Output State
255	198	Full-Scale
128	10,120	Midscale
1	19,982	1 LSB
0	20,060	Zero-Scale

The typical distribution of the end-to-end resistance R_{AB} from channel to channel matches within ±1%. Device to device matching is process lot dependent and is possible to have ±30% variation. Since the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a very low temperature coefficient of 30 ppm/°C.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage from Terminals A to B. Unlike the polarity from V_{DD} to V_{SS}, which must be positive, the voltage across A-B, W-A, and W-B can be at either polarity, provided that V_{SS} is powered by a negative supply.

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage from the wiper to B starting at 0 V up to 1 LSB below 5 V. Each LSB step of voltage is equal to the voltage applied across Terminals A-B divided by the 256 positions of the potentiometer divider. Since the AD5263 can be powered by dual supplies, the general equation defining the output voltage V_W with respect to ground for any valid input voltages applied to Terminals A and B is

$$V_W(D) = \frac{D}{256} V_A + \frac{256 - D}{256} V_B \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, V_W can be found as

$$V_W(D) = \frac{R_{WB}(D)}{256} V_A + \frac{R_{WA}(D)}{256} V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistances R_{WA} and R_{WB}, and not their absolute values; therefore, the temperature drift reduces to 5 ppm/°C.

PIN SELECTABLE DIGITAL INTERFACE

The AD5263 provides the flexibility of a selectable interface. When the digital interface select (DIS) pin is tied low, the SPI mode is engaged. When the DIS pin is tied high to the V_L supply, the I^2C mode is engaged.

SPI COMPATIBLE 3-WIRE SERIAL BUS (DIS = 0)

The AD5263 contains a 3-wire SPI compatible digital interface (SDI, $\overline{CS}$, and CLK). The 10-bit serial word must be loaded with address bits A1 and A0, followed by the data byte, MSB first. The format of the word is shown in Table 4.

The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or other suitable means. When $\overline{CS}$ is low, the clock loads data into the serial register on each positive clock edge (see Figure 39).

Table 9. AD5263 Address Decode Table

A1	A0	Latch Loaded
0	0	RDAC 1
0	1	RDAC 2
1	0	RDAC 3
1	1	RDAC 4

The data setup and data hold times in the specification table determine the valid timing requirements. The AD5263 uses a 10-bit serial input data register word that is transferred to the internal RDAC register when the $\overline{CS}$ line returns to logic high. Note that only the last 10-bits that are clocked into the register are latched into the decoder. As $\overline{CS}$ goes high, it activates the address decoder and updates the corresponding channel according to Table 9.

During shutdown ($\overline{SHDN}$), the serial data output (SDO) pin is forced to logic high in order to avoid power dissipation in the external pull-up resistor. For an equivalent SDO output circuit schematic, see Figure 45.

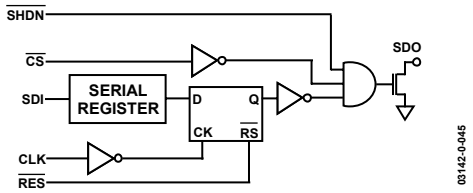

Figure 45. Detailed SDO Output Schematic of the AD5263

During reset ($\overline{RES}$), the wiper is set to midscale. Note that unlike $\overline{SHDN}$, when the part is taken out of reset, the wiper will remain at midscale and will not revert to its pre-reset setting.

Daisy-Chain Operation

The serial data output (SDO) pin contains an open drain N-channel FET. This output requires a pull-up resistor in order to transfer data to the next package's SDI pin. This allows for daisy chaining several RDACs from a single processor serial data line. The pull-up resistor termination voltage can be greater than the V_{DD} supply voltage. It is recommended to increase the clock period when using a pull-up resistor to the SDI pin of the following device because capacitive loading at the daisy-chain node (SDO-SDI) between devices may induce time delay to subsequent devices. Users should be aware of this potential problem to achieve data transfer successfully (see

Figure 46). If two AD5263s are daisy-chained, a total of 20 bits of data is required. The first 10 bits, complying with the format shown in Table 4, go to U2 and the second 10 bits, with the same format, go to U1. $\overline{CS}$ should be kept low until all 20 bits are clocked into their respective serial registers. After this, $\overline{CS}$ is pulled high to complete the operation and load the RDAC latch. Note that data appears on SDO on the negative edge of the clock, thus making it available to the input of the daisy-chained device on the rising edge of the next clock.

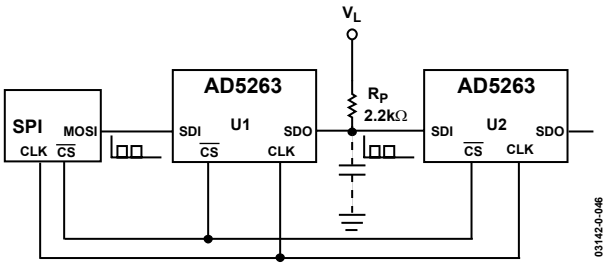

Figure 46. Daisy-Chain Configuration

I²C COMPATIBLE 2-WIRE SERIAL BUS (DIS = 1)

In the I²C compatible mode, the RDACs are connected to the bus as slave devices.

Referring to Table 5 and Table 6, the first byte of the AD5263 is a slave address byte, consisting of a 7-bit slave address and a R/$\overline{W}$ bit. The five MSBs are 01011 and the following two bits are determined by the state of the AD0 and AD1 pins of the device. AD0 and AD1 allow the user to place up to four of the I²C compatible devices on one bus.

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 42). The following byte is the slave address byte, which consists of the 7-bit slave address followed by an R/$\overline{W}$ bit. This R/$\overline{W}$ bit determines whether data will be read from or written to the slave device.

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master will read from the slave device. If the R/$\overline{W}$ bit is low, the master will write to the slave device.

2. In the write mode, the second byte is the instruction byte. The first bit (MSB) of the instruction byte is a don't care. The following two bits, labeled A1 and A0, are the RDAC subaddress select bits.

   The fourth MSB (RS) is the midscale reset. A logic high on this bit moves the wiper of the selected channel to the center tap where $R_{WA} = R_{WB}$. This feature effectively writes over the contents of the register, so that when taken out of reset mode, the RDAC will remain at midscale.

   The fifth MSB (SD) is the shutdown bit. A logic high causes the selected channel to open circuit at Terminal A while shorting the wiper to Terminal B. This operation yields almost 0 Ω in rheostat mode or 0 V in potentiometer mode. This SD bit serves the same function as the $\overline{SHDN}$ pin except that the $\overline{SHDN}$ pin reacts to active low. Also, the $\overline{SHDN}$ pin affects all channels, as opposed to the SD bit, which affects only the channel being written to. It is important to note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting will be applied to the RDAC.

   The next two bits are O2 and O1. They are extra programmable logic outputs that can be used to drive other digital loads, logic gates, LED drivers, analog switches, etc.

   The LSB is a don't care (see Table 5).

   After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 42).

3. In the read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference with the write mode, where there are eight data bits followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 43).

   Note that the channel of interest is the one that was previously selected in the write mode. In the case where users need to read the RDAC values of both channels, they need to program the first channel in the write mode and then change to the read mode to read the first channel value. After that, they need to change back to the write mode with the second channel selected and read the second channel value in the read mode again. It is not necessary for users to issue the Frame 3 data byte in the write mode for subsequent readback operation. Refer to Figure 43 for the programming format.

4. After all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master will pull the SDA line high during the tenth clock pulse to establish a STOP condition (see Figure 42). In read mode, the master will issue a no acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the tenth clock pulse, which goes high to establish a STOP condition (see Figure 43).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in the write mode, the RDAC output will update on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

ADDITIONAL PROGRAMMABLE LOGIC OUTPUT

The AD5263 features additional programmable logic outputs, O1 and O2, which can be used to drive a digital load, analog switches, and logic gates. O1 and O2 default to Logic 0. The voltage level can swing from GND to V_L. The logic states of O1 and O2 can be programmed in Frame 2 under write mode (see Figure 42). These logic outputs have adequate current driving capability to sink/source milliamperes of load.

Users can also activate O1 and O2 in three different ways without affecting the wiper settings. They may do the following:

1. START, slave address byte, acknowledge, instruction byte with O1 and O2 specified, acknowledge, STOP.

2. Complete the write cycle with STOP, then START, slave address byte, acknowledge, instruction byte with O1 and O2 specified, acknowledge, STOP.

3. Do not complete the write cycle by not issuing the STOP, then START, slave address byte, acknowledge, instruction byte with O1 and O2 specified, acknowledge, STOP.

SELF-CONTAINED SHUTDOWN FUNCTION

Shutdown can be activated by strobing the $\overline{\text{SHDN}}$ pin or programming the SD bit in the write mode instruction byte. In addition, shutdown can even be implemented with the device's digital output as shown in Figure 47. In this configuration, the device will be shut down during power-up, but users are allowed to program the device. Thus, when O1 is programmed high, the device will exit from the shutdown mode and respond to the new setting. This self-contained shutdown function allows absolute shutdown during power-up, which is crucial in hazardous environments, without adding extra components.

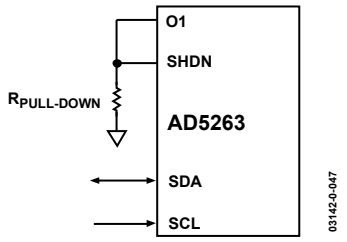

Figure 47. Shutdown by Internal Logic Output

MULTIPLE DEVICES ON ONE BUS

Figure 48 shows four AD5263 devices on the same serial bus. Each has a different slave address since the states of their AD0 and AD1 pins are different. This allows each RDAC within each device to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I^2C compatible interface.

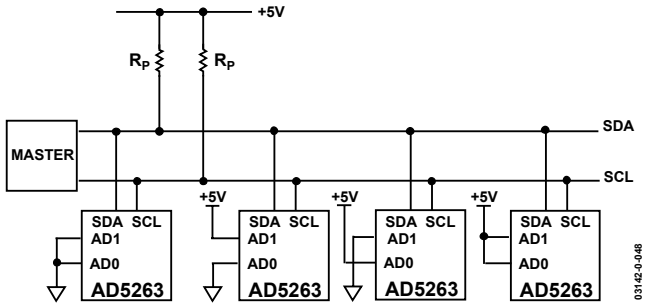

Figure 48. Multiple AD5263 Devices on One I^2C Bus

LEVEL SHIFT FOR NEGATIVE VOLTAGE OPERATION

The digital potentiometer is popular in laser diode driver and certain telecommunication equipment level-setting applications. These applications are sometimes operated between ground and some negative supply voltage so that the systems can be biased at ground to avoid large bypass capacitors that may significantly impede the ac performance. Like most digital potentiometers, the AD5263 can be configured with a negative supply (see Figure 49).

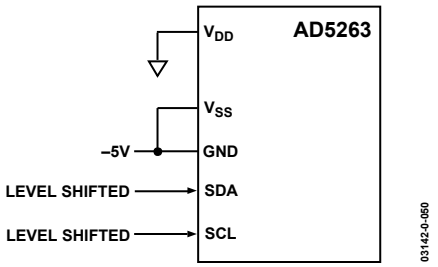

Figure 49. Biased at Negative Voltage

However, the digital inputs must also be level shifted to allow proper operation since the ground is now referenced to the negative potential. As a result, Figure 50 shows one implementation with a couple transistors and a few resistors.

When V_{IN} is high, Q1 is turned on and its emitter is clamped at one threshold above ground. This threshold appears at the base of Q2, which causes Q2 to turn off. In this state, V_{OUT} approaches −5 V. When V_{IN} is low, Q1 is turned off and the base of Q2 is pulled low, which in turn causes Q2 to turn on. In this state, V_{OUT} approaches 0 V. Beware that proper time shifting is also needed for successful communication with the device.

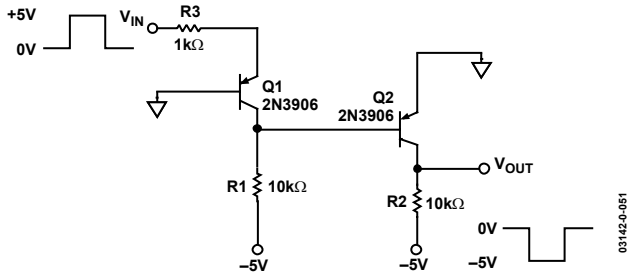

Figure 50. Level Shift for Bipolar Potential Operation

ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures shown in Figure 51 and Figure 52. This protection applies to digital input pins SDI/SDA, CLK/SCL, $\overline{CS}$/AD0, $\overline{RES}$/AD1, and $\overline{SHDN}$.

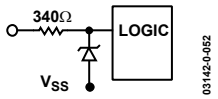

Figure 51. ESD Protection of Digital Pins

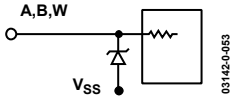

Figure 52. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5263 positive V_{DD} and negative V_{SS} power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminals A, B, and W that exceed V_{DD} or V_{SS} will be clamped by the internal forward biased diodes shown in Figure 53.

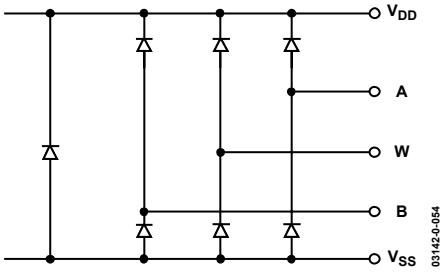

Figure 53. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

POWER-UP SEQUENCE

Since the ESD protection diodes limit the voltage compliance at Terminals A, B, and W (see Figure 53), it is important to power V_{DD} and V_{SS} before applying any voltage to Terminals A, B, and W; otherwise, the diodes will be forward biased such that V_{DD} and V_{SS} will be powered unintentionally and may affect the rest of the circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, V_{SS}, V_L, digital inputs, and $V_{A/B/W}$. The relative order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD} and V_{SS}.

V_{LOGIC} POWER SUPPLY

The AD5263 is capable of operating at high voltages beyond the internal logic levels, which are limited to operation at 5 V. As a result, V_L always needs to be tied to a separate 2.7 V to 5.5 V source to ensure proper digital signal levels. Logic levels must be limited to V_L, regardless of V_{DD}. In addition, V_L should always be less than or equal to V_{DD}.

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum-lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF to 0.1 µF ceramic disc or chip capacitors. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 54). Notice the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

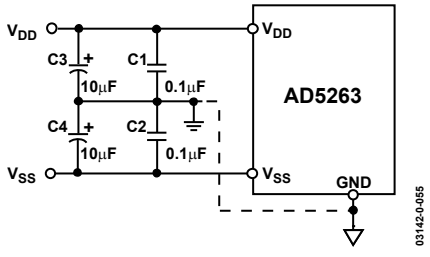

Figure 54. Power Supply Bypassing

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the RDACs. Configured as a potentiometer divider, the –3 dB bandwidth of the AD5263 (20 kΩ resistor) measures 300 kHz at half scale. Figure 21 provides the large signal BODE plot characteristics of the three available resistor versions: 20 kΩ, 50 kΩ, and 200 kΩ. A parasitic simulation model is shown in Figure 55. The following code provides a macro model net list for the 20 kΩ RDAC.

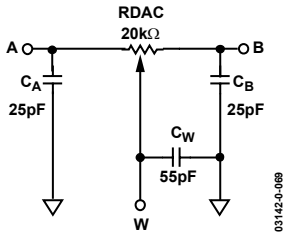

Figure 55. RDAC Circuit Simulation Model for RDAC = 20 kΩ

Listing 1. Macro Model Net List for RDAC

```
.PARAM D=256, RDAC=20E3
*
.SUBCKT DPOT (A,W,B)
*
CA      A       0       25E-12
RWA     A       W       {(1-D/256)*RDAC+60}
CW      W       0       55E-12
RWB     W       B       {D/256*RDAC+60}
CB      B       0       25E-12
*
.ENDS DPOT
```

APPLICATIONS

BIPOLAR DC OR AC OPERATION FROM DUAL SUPPLIES

The AD5263 can be operated from dual supplies, enabling control of ground referenced ac signals or bipolar operation. The ac signal, as high as V_{DD}/V_{SS}, can be applied directly across Terminals A-B with the output taken from Terminal W. See Figure 56 for a typical circuit connection.

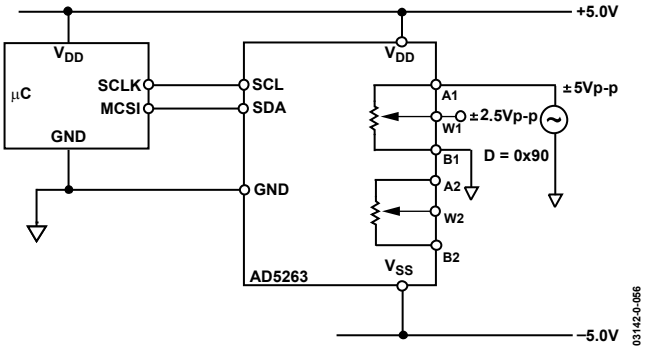

Figure 56. Bipolar Operation from Dual Supplies

GAIN CONTROL COMPENSATION

The digital potentiometer is commonly used in gain control such as the noninverting gain amplifier shown in Figure 57.

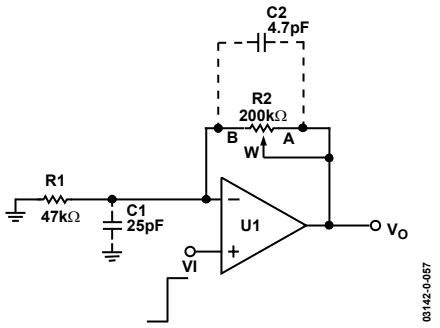

Figure 57. Typical Noninverting Gain Amplifier

Notice the RDAC B terminal parasitic capacitance is connected to the op amp noninverting node. It introduces a zero for the $1/\beta_o$ term with +20 dB/dec, whereas a typical op amp GBP has –20 dB/dec characteristics. A large R2 and finite C1 can cause this zero's frequency to fall well below the crossover frequency. Thus, the rate of closure becomes 40 dB/dec and the system has 0° phase margin at the crossover frequency. The output may ring or oscillate if the input is a rectangular pulse or step function. Similarly, it is also likely to ring when switching between two gain values, because this is equivalent to a step change at the input.

Depending on the op amp GBP, reducing the feedback resistor may extend the zero's frequency far enough to overcome the problem. A better approach is to include a compensation capacitor C2 to cancel the effect caused by C1. Optimum compensation occurs when R1 × C1 = R2 × C2 . This is not an option, because of the variation of R2. As a result, one may use the relationship above and scale C2 as if R2 is at its maximum value. Doing so may overcompensate and compromise the performance slightly when R2 is set at low values. However, it will avoid the gain peaking, ringing, or oscillation in the worst case. For critical applications, C2 should be found empirically to suit the need. In general, C2 in the range of few pF to no more than a few tenths of pF is usually adequate for the compensation.

Similarly, there are W and A terminal capacitances connected to the output (not shown); fortunately their effect at this node is less significant and the compensation can be disregarded in most cases.

PROGRAMMABLE VOLTAGE REFERENCE

For voltage divider mode operation (Figure 58), it is common to buffer the output of the digital potentiometer unless the load is much larger than R_{WB}. Not only does the buffer serve the purpose of impedance conversion, but also allows a heavier load to be driven.

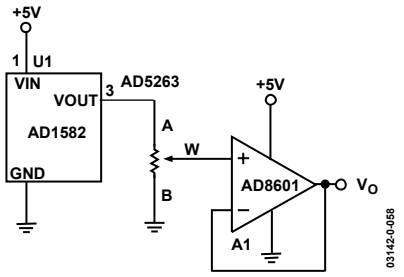

Figure 58. Programmable Voltage Reference

8-BIT BIPOLAR DAC

Figure 59 shows a low cost, 8-bit, bipolar DAC. It offers the same number of adjustable steps but not the precision as compared to conventional DACs. The linearity and temperature coefficient, especially at low values codes, are skewed by the effects of the digital potentiometer wiper resistance. The output of this circuit is

$$V_O = \left(\frac{2D}{256} - 1\right) \times V_{REF} \quad (5)$$

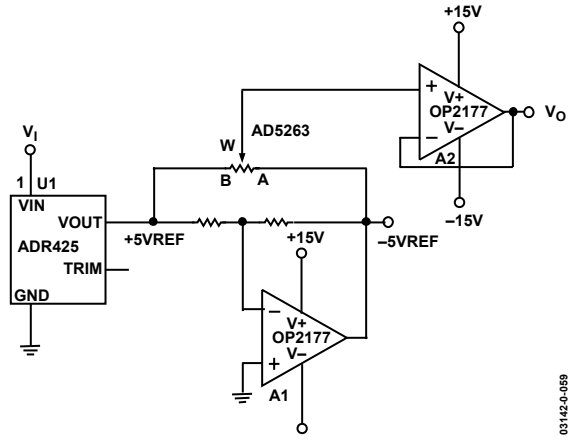

Figure 59. 8-Bit Bipolar DAC

BIPOLAR PROGRAMMABLE GAIN AMPLIFIER

For applications requiring bipolar gain, Figure 60 shows one implementation similar to the previous circuit. The digital potentiometer U1 sets the adjustment range. The wiper voltage at W2 can therefore be programmed between V_I and $-KV_I$ at a given U2 setting. Configuring A2 in the noninverting mode allows linear gain and attenuation. The transfer function is

$$\frac{V_O}{V_I} = \left(1 + \frac{R2}{R1}\right) \times \left(\frac{D2}{256} \times (1 + K) - K\right) \quad (6)$$

where K is the ratio of R_{WB1}/R_{WA1} set by U1.

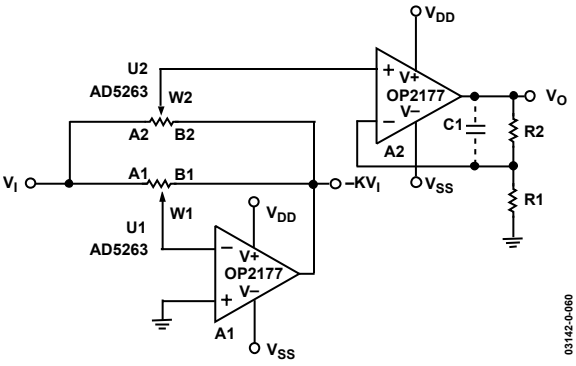

Figure 60. Bipolar Programmable Gain Amplifier

Similar to the previous example, in the simpler (and much more usual) case where $K = 1$, a single channel is used and U1 is replaced by a matched pair of resistors to apply V_I and $-V_I$ at the ends of the digital potentiometer. The relationship becomes

$$V_O = \left(1 + \frac{R2}{R1}\right) \times \left(\frac{2 \times D2}{256} - 1\right) \times V_I \quad (7)$$

If $R2$ is large, a compensation capacitor of a few pF may be needed to avoid any gain peaking.

Table 10 shows the result of adjusting D, with A2 configured with unity gain, gain of 2, and gain of 10. The result is a bipolar amplifier with linearly programmable gain and 256-step resolution.

Table 10. Result of Bipolar Gain Amplifier

D	R1 = ∞, R2 = 0	R1 = R2	R2 = 9 × R1
0	–1	–2	–10
64	–0.5	–1	–5
128	0	0	0
192	0.5	1	5
255	0.968	1.937	9.680

PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT

For applications that require high current adjustment, such as a laser diode driver or tunable laser, a boosted voltage source can be considered. See Figure 61.

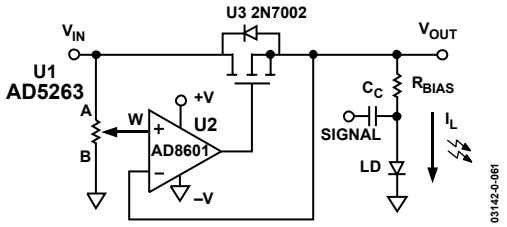

Figure 61. Programmable Booster Voltage Source

In this circuit, the inverting input of the op amp forces the V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-channel FET N1. N1 power handling must be adequate to dissipate power equal to $(V_{IN} - V_{OUT}) \times I_L$. This circuit can source a maximum of 100 mA with a 5 V supply. For precision applications, a voltage reference such as ADR421, ADR03, or ADR370 can be applied at the A terminal of the digital potentiometer.

PROGRAMMABLE 4–20 mA CURRENT SOURCE

A programmable 4–20 mA current source can be implemented with the circuit shown in Figure 62. The REF191 is a unique low supply headroom and high current handling precision reference that can deliver 20 mA at +2.048 V. The load current is simply the voltage across Terminals B-W of the digital potentiometer divided by R_S:

$$I_L = \frac{V_{REF} \times D}{R_S \times 2^N} \quad (8)$$

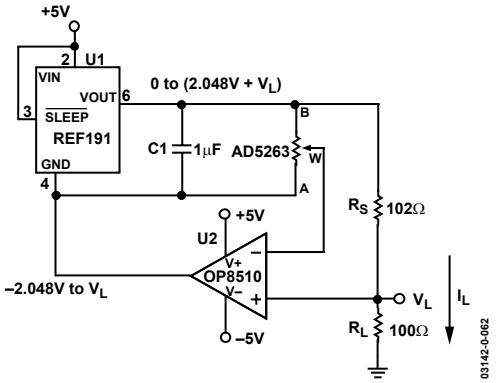

Figure 62. Programmable 4–20 mA Current Source

The circuit is simple, but beware of two things. First, dual-supply op amps are ideal because the ground potential of the REF191 can swing from –2.048 V at zero scale to V_L at full scale of the potentiometer setting. Although the circuit works with a single supply, the programmable resolution of the system will be reduced.

For applications that demand higher current capabilities, a few changes to the circuit in Figure 62 will produce an adjustable current in the range of hundreds of mA. First, the voltage reference needs to be replaced with a high current, low dropout regulator, such as the ADP3333, and the op amp needs to be swapped with a high current, dual-supply model, such as the AD8532. Depending on the desired range of current, an appropriate value for R_S must be calculated. Because of the high current flowing to the load, the user must pay attention to the load impedance so as not to drive the op amp past the positive rail.

PROGRAMMABLE BIDIRECTIONAL CURRENT SOURCE

For applications that require bidirectional current control or higher voltage compliance, a Howland current pump can be a solution (see Figure 63). If the resistors are matched, the load current is

$$I_L = \frac{(R2A + R2B)/R1}{R2B} \times V_W \quad (9)$$

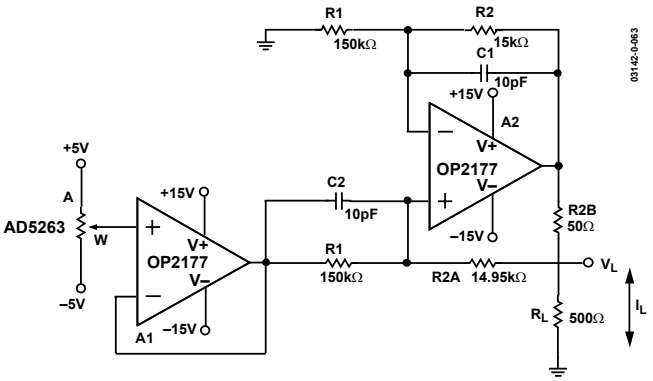

Figure 63. Programmable Bidirectional Current Source

R2B, in theory, can be made as small as needed to achieve the current needed within A2's output current driving capability. In this circuit, OP2177 can deliver ±5 mA in either direction, and the voltage compliance approaches +15 V. It can be shown that the output impedance is

$$Z_o = \frac{R1' \times R2B(R1 + R2A)}{R1 \times R2' - R1'(R2A + R2B)} \quad (10)$$

This output impedance can be infinite if resistors R1′ and R2′ match precisely with R1 and R2A+R2B, respectively. On the other hand, it can be negative if the resistors are not matched. As a result, C1 in the range of 1 pF to 10 pF is needed to prevent oscillation.

PROGRAMMABLE LOW-PASS FILTER

In A/D conversion applications, it is common to include an antialiasing filter to band-limit the sampling signal. Dual-channel digital potentiometers can be used to construct a second order Sallen-Key low-pass filter (see Figure 64). The design equations are

$$\frac{V_O}{V_I} = \frac{\omega_O{}^2}{S^2 + \frac{\omega_O}{Q} S + \omega_O{}^2} \quad (11)$$

$$\omega_O = \sqrt{\frac{1}{R1 \times R2 \times C1 \times C2}} \quad (12)$$

$$Q = \frac{1}{R1 \times C1} + \frac{1}{R2 \times C2} \quad (13)$$

Users can first select some convenient values for the capacitors. To achieve maximally flat bandwidth where Q = 0.707, let C1 be twice the size of C2, and let R1 = R2. As a result, the user can adjust R1 and R2 to the same settings to achieve the desired bandwidth.

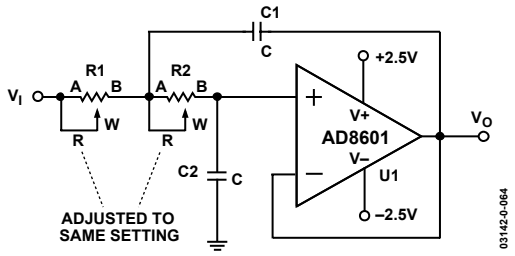

Figure 64. Sallen-Key Low-Pass Filter

PROGRAMMABLE OSCILLATOR

In a classic Wien-bridge oscillator (Figure 65), the Wien network (R, R′, C, C′) provides positive feedback, while R1 and R2 provide negative feedback. At the resonant frequency, f_O, the overall phase shift is zero, and the positive feedback causes the circuit to oscillate.

With R = R′, C = C′, and R2 = R2A||(R2B + R_{DIODE}), the oscillation frequency is

$$\omega_O = \frac{1}{RC}, \text{ or } f_O = \frac{1}{2\pi RC} \quad (14)$$

where R is equal to R_{WA}, such that

$$R = \frac{256 - D}{256} R_{AB} \quad (15)$$

At resonance, setting

$$\frac{R2}{R1} = 2 \quad (16)$$

balances the bridge. In practice, $R2/R1$ should be set slightly greater than 2 to ensure that the oscillation can start. On the other hand, the alternating turn-on of the diodes D1 and D2 ensures that $R2/R1$ is momentarily less than 2, thereby stabilizing the oscillation.

Once the frequency is set, the oscillation amplitude can be tuned by $R2B$, since

$$\frac{2}{3} V_O = I_D \times R2B + V_D \quad (17)$$

V_O, I_D, and V_D are interdependent variables. With proper selection of $R2B$, an equilibrium will be reached such that V_O converges. $R2B$ can be in series with a discrete resistor to increase the amplitude, but the total resistance should not be so large that it saturates the output.

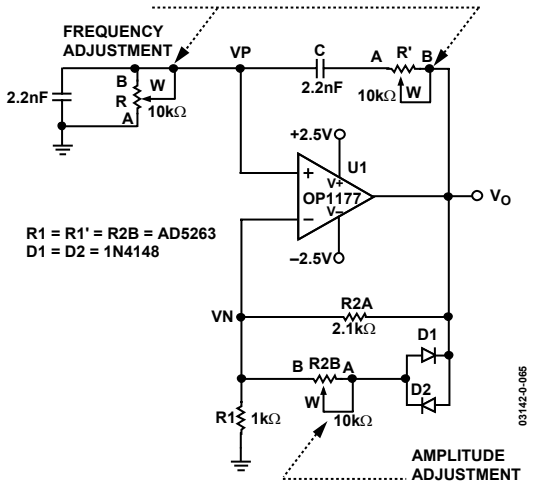

Figure 65. Programmable Oscillator with Amplitude Control

RESISTANCE SCALING

The AD5263 offers 20kΩ, 50kΩ, and 200kΩ nominal resistances. Users who need a lower resistance and the same number of step adjustments can place multiple devices in parallel. For example, Figure 66 shows a simple scheme of using two channels in parallel. To adjust half of the resistance linearly per step, users need to program both channels to the same settings.

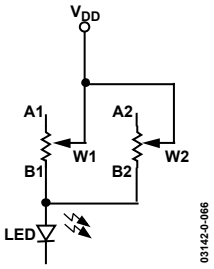

Figure 66. Reduce Resistance by Half with Linear Adjustment Characteristics

Applicable only to the voltage divider mode, by connecting a discrete resistor in parallel as shown in Figure 67, a proportionately lower voltage appears at Terminal A. This translates into a finer degree of precision because the step size at Terminal W will be smaller. The voltage can be found as

$$V_W(D) = \frac{D}{256} \times \left(\frac{V_{DD}}{R2 + (R_{AB} \,||\, R1)} \right) \times (R_{AB} \,||\, R1) \qquad (18)$$

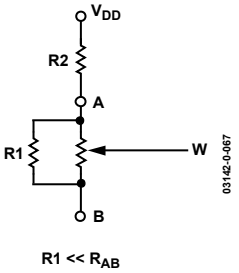

Figure 67. Decreasing Step Size by Lowering the Nominal Resistance

Figure 66 and Figure 67 show applications in which the digital potentiometers change steps linearly. On the other hand, log taper adjustment is usually preferred in applications such as volume control. Figure 68 shows another method of resistance scaling which produces a pseudo-log taper output. In this circuit, the smaller the value of R2 with respect to R_{AB}, the more the output approaches log type behavior.

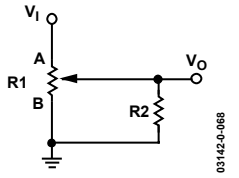

Figure 68. Resistor Scaling with Log Adjustment Characteristics

RESISTANCE TOLERANCE, DRIFT, AND TEMPERATURE COEFFICIENT MISMATCH CONSIDERATIONS

In the rheostat mode operation, such as the gain control circuit of Figure 69, the tolerance mismatch between the digital potentiometer and the discrete resistor can cause repeatability issues among various systems. Because of the inherent matching of the silicon process, it is practical to apply the multichannel device in this type of application. As such, R1 should be replaced by one of the channels of the digital potentiometer. R1 should be programmed to a specific value while R2 can be used for the adjustable gain. Although it adds cost, this approach minimizes the tolerance and temperature coefficient mismatch between R1 and R2. In addition, this approach also tracks the resistance drift over time. As a result, these non-ideal parameters become less sensitive to system variations.

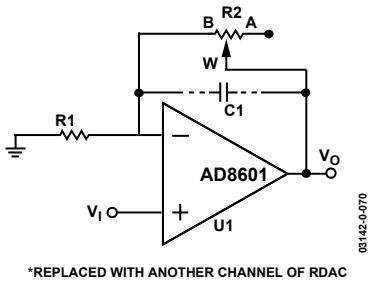

Figure 69. Linear Gain Control with Tracking Resistance Tolerance and Drift

Notice that the circuit in Figure 70 can also be used to track the tolerance, temperature coefficient, and drift in this particular application. However, the characteristics of the transfer function change from a linear to a pseudo-logarithmic gain function.

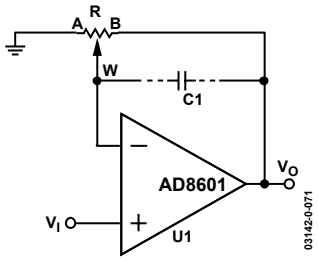

Figure 70. Nonlinear Gain Control with Tracking Resistance Tolerance and Drift

PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

PIN CONFIGURATION

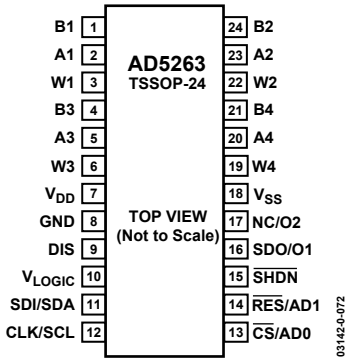

Figure 71. 24-Lead TSSOP

PIN FUNCTION DESCRIPTIONS

Table 11.

Pin	Name	Description
1	B1	Resistor Terminal B1
2	A1	Resistor Terminal A1 (ADDR = 00)
3	W1	Wiper Terminal W1
4	B3	Resistor Terminal B3
5	A3	Resistor Terminal A3
6	W3	Wiper Terminal W3 (ADDR = 10)
7	V_{DD}	Positive Power Supply, specified for +5 V to +15 V operation.
8	GND	Ground
9	DIS	Digital Interface Select (SPI/I²C Select). SPI when DIS = 0, I²C when DIS = 1
10	V_{LOGIC}	2.7 V to 5.5 V Logic Supply Voltage. The logic supply voltage should always be less than or equal to V_{DD}. In addition, logic levels must be limited to the logic supply voltage regardless of V_{DD}.
11	SDI/SDA	SDI = 3-Wire Serial Data Input. SDA = 2-Wire Serial Data Input/Output.
12	CLK/SCL	Serial Clock Input
13	$\overline{CS}$/AD0	Chip Select in SPI Mode. Device Address Bit 0 in I²C Mode.
14	$\overline{RES}$/AD1	RESET in SPI Mode. Device Address Bit 1 in I²C Mode.
15	$\overline{SHDN}$	Shutdown. Shorts wiper to Terminal B, opens Terminal A. Tie to +5 V supply if not used. Do not tie to V_{DD} if V_{DD} > 5 V.
16	SDO/O1	Serial Data Output in SPI Mode, open-drain transistor requires pull-up resistor. Digital Output O1 in I²C Mode, can be used to drive external logic.
17	NC/O2	No Connection in SPI Mode. Digital Output O2 in I²C Mode, can be used to drive external logic.
18	V_{SS}	Negative Power Supply, specified for operation from 0 V to –5 V.
19	W4	Wiper Terminal W4 (ADDR = 11)
20	A4	Resistor Terminal A4
21	B4	Resistor Terminal B4
22	W2	Wiper Terminal W2 (ADDR = 01)
23	A2	Resistor Terminal A2
24	B2	Resistor Terminal B2

OUTLINE DIMENSIONS

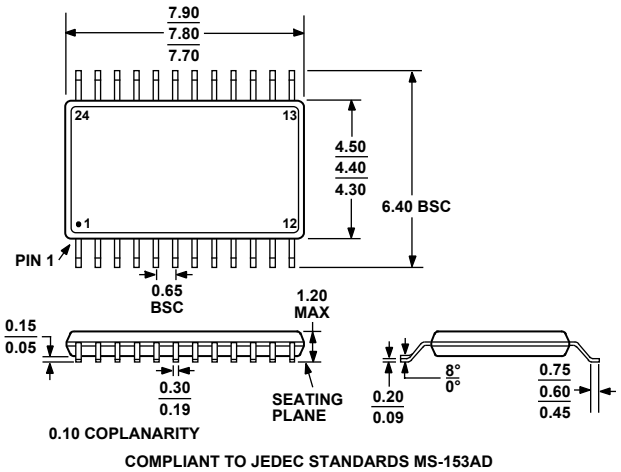

Figure 72. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Table 12. Ordering Guide

Model[1]	R_{AB} (kΩ)	Temperature	Package Description	Package Option	Parts per Container
AD5263BRU20	20	–40°C to +125°C	TSSOP-24	RU-24	62
AD5263BRU20-REEL7	20	–40°C to +125°C	TSSOP-24	RU-24	1,000
AD5263BRU50	50	–40°C to +125°C	TSSOP-24	RU-24	62
AD5263BRU50-REEL7	50	–40°C to +125°C	TSSOP-24	RU-24	1,000
AD5263BRU200	200	–40°C to +125°C	TSSOP-24	RU-24	62
AD5263BRU200-REEL7	200	–40°C to +125°C	TSSOP-24	RU-24	1,000
AD5263EVAL	See Note 2		Evaluation Board		

[1]Package branding: Line 1 contains the model number, Line 2 contains the end-to-end resistance, and Line 3 contains the date code YYWW.
[2]The evaluation board is shipped with the 20 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

The AD5263 contains 5,184 transistors. Die size: 108 mil × 198 mil = 21,384 sq. mil.

NOTES

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