FAIRCHILD SEMICONDUCTOR®

June 2011

FAN4852
9MHz Low-Power Dual CMOS Amplifier

Features

- 0.8mA Supply Current
- 9 MHz Bandwidth
- Output Swing to within 10mV of Either Rail
- Input Voltage Range Exceeds the Rails
- 6V/µs Slew Rate
- 11nV/√Hz Input Voltage Noise
- Fully Specified at +3.3V and +5V Supplies

Applications

- Piezoelectric Sensors
- PCMCIA, USB
- Mobile Communications / Battery-Powered Devices
- Notebooks and PDAs
- Active Filters
- Signal Conditioning
- Portable Test Instruments

Description

The FAN4852 is a dual, rail-to-rail output, low-power, CMOS amplifier that consumes only 800µA of supply current, while providing ±50mA of output short-circuit current. This amplifier is designed to operate supplies from 2.5V to 5V.

Additionally, the FAN4852 is EMI hardened, which minimizes EMI interference. It has a maximum input offset voltage of 1mV and an input common-mode range that includes ground.

The FAN4852 is designed on a CMOS process and provides 9MHz of bandwidth and 6V/µs of slew rate. The combination of low-power, low-voltage operation and a small package make this amplifier well suited for general-purpose and battery-powered applications.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN4852IMU8X	-40 to +85°C	8-Lead MSOP Package	3000 on Tape and Reel

Pin Configuration

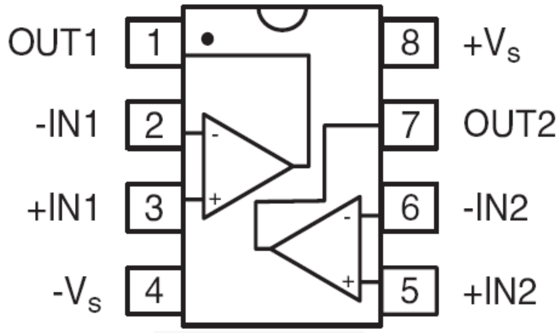

Figure 1. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	OUT1	Output, Channel 1
2	-IN1	Negative Input, Channel 1
3	+IN1	Positive Input, Channel 1
4	-Vs	Negative Supply
5	+IN2	Positive Input, Channel 2
6	-IN2	Negative Input, Channel 2
7	OUT2	Output, Channel 2
8	+Vs	Positive Supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if operating conditions are not exceeded.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	0	6	V
V_{IN}	Input Voltage Range	$-V_S-0.5$	$+V_S+0.5$	V
T_J	Junction Temperature		+150	°C
T_{STG}	Storage Temperature	-65	+150	°C
T_L	Lead Soldering, 10 Seconds		+260	°C
Θ_{JA}	Thermal Resistance(1)		206	°C/W

Note:
1. Package thermal resistance JEDEC standard, multi-layer test boards, still air.

ESD Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
ESD	Human Body Model, JESD22-A114		8		kV
	Charged Device Model, JESD22-C101		2		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		+85	°C
Vs	Supply Voltage Range	2.5	3.3	5.0	V

Electrical Specifications at +3.3V

$+V_S$=+3.3V, -Vs = 0V, V_{CM} = $+V_s/2$, and R_L = 10KΩ to $+V_s/2$, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_S	Supply Current(2)	T_A=25˚C		0.8	1.0	mA
		Full Temperature Range			1.1	
I_{SC}	Short-Circuit Output Current(2)	Sourcing V_O=V_{CM}, V_{IN}=100mV, T_A=25˚C	25	50		mA
		Sourcing V_O=V_{CM}, V_{IN}=100mV, Full Temperature Range	20			
		Sinking V_O=V_{CM}, V_{IN}=-100mV, T_A=25˚C	28	46		
		Sinking V_O=V_{CM}, V_{IN}=-100mV, Full Temperature Range	20			
EMIRR	EMI Rejection Ratio, +IN and -IN(4)	V_{RFpeak}=100mVp, (-20dBVp) f=400MHz		75		dB
		V_{RFpeak}=100mVp, (-20dBVp) f=900MHz		78		
		V_{RFpeak}=100mVp, (-20dBVp) f=1800MHz		87		
PSRR	Power Supply Rejection Ratio(2)	2.7V≤V+≤3.3V, V_O=1V, T_A=25˚C	75	95		dB
		2.7V≤V+≤3.3V, V_O=1V, Full Temperature Range	74			
CMRR	Common Mode Rejection Ratio(2)	-0.2V<V_{CM} <V+-1.2V, T_A=25˚C	76	117		dB
		-0.2V<V_{CM} <V+-1.2V, Full Temperature Range	75			
CMIR	Input Common Mode Voltage Range(2)	CMRR≥76dB	-0.2		2.1	V
V_{OS}	Input Offset Voltage(2)	T_A=25˚C		±0.3	±1.0	mV
		Full Temperature Range			±1.2	
dV_{IO}	Average Drift(3)			±0.4	±2.0	μV/°C
I_{OS}	Input Offset Current			1		pA
		T_A=				
I_{bn_Char}	Input Bias Current(3)	T_A=25˚C		0.1	10.0	pA
		Full Temperature Range			500	
e_n	Input-Referred Voltage Noise	f=1kHz		11		nV/√Hz
		f=10kHz		10		
i_N	Input-Referred Current Noise	f=1kHz		0.005		pA/√Hz

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Electrical Specifications at +3.3V

$+V_S$=+3.3V, -Vs = 0V, V_{CM} = $+V_s/2$, and R_L = 10KΩ to $+V_s/2$, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_O	Output Voltage Swing High(2) $V_O = (+V_S) - V_{OUT}$	R_L=2kΩ to V+/2, T_A=25˚C		21	35	mV
		R_L=2kΩ to V+/2, Full Temperature Range			43	
		R_L=10kΩ to V+/2, T_A=25˚C		4	10	
		R_L=10kΩ to V+/2, Full Temperature Range			12	
	Output Voltage Swing Low(2) $V_O = V_{OUT} + (-V_S)$	R_L=2kΩ to V+/2, T_A=25˚C		20	32	mV
		R_L=2kΩ to V+/2, Full Temperature Range			43	
		R_L=10kΩ to V+/2, T_A=25˚C		3	11	
		R_L=10kΩ to V+/2, Full Temperature Range			14	
GBW	Gain Bandwidth Product			9		MHz
A_{VOL}	Large Signal Voltage Gain(3)	R_L=2kΩ, V_O=0.15 to 1.65V, V_O=3.15 to 1.65V, T_A=25˚C	100	114		dB
		R_L=2kΩ, V_O=0.15 to 1.65V, V_O=3.15 to 1.65V, Full Temperature Range	97			
		R_L=10kΩ, V_O=0.1 to 1.65V, V_O=3.2 to 1.65V, T_A=25˚C	100	115		
		R_L=10kΩ, V_O=0.1 to 1.65V, V_O=3.2 to 1.65V, Full Temperature Range	97			
R_{OUT}	Closed-Loop Impedance	f=6MHz		6		Ω
R_{IN}	Input Resistance			10		GΩ
C_{IN}	Input Capacitance	Common Mode		11		pF
		Differential Mode		6		
$Φ_M$	Phase Margin			86		˚
SR	Slew Rate	Av=+1, V_O=1V_{pp} 10%-90%		6.1		V/µs
THD+N	Total Harmonic Distortion + Noise	f=1kHz, Av=1, BW=>500kHz		0.006		%

Notes:
2. 100% tested at T_A=25°C.
3. Guaranteed by characterization.
4. EMI rejection ratio is defined as EMIRR – 20log (V_{RFpeak} / $ΔV_{OS}$).

Electrical Specifications at +5V

$+V_S$=+5V, $-V_S$ = 0V, V_{CM} = $+V_S/2$, and R_L = 10KΩ to $+V_S/2$, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_S	Supply Current(5)	T_A=25˚C		0.9	1.1	mA
		Full Temperature Range			1.2	
I_{SC}	Short-Circuit Output Current(5)	Sourcing V_O=V_{CM}, V_{IN}=100mV, T_A=25˚C	60	90		mA
		Sourcing V_O=V_{CM}, V_{IN}=100mV, Full Temperature Range	48			
		Sinking V_O=V_{CM}, V_{IN}=-100mV, T_A=25˚C	58	90		
		Sinking V_O=V_{CM}, V_{IN}=-100mV, Full Temperature Range	44			
EMIRR	EMI Rejection Ratio, +IN and -IN(7)	V_{RFpeak}=100mVp, (-20dBVp) f=400MHz		75		dB
		V_{RFpeak}=100mVp, (-20dBVp) f=900MHz		78		
		V_{RFpeak}=100mVp, (-20dBVp) f=1800MHz		87		
PSRR	Power Supply Rejection Ratio(5)	2.7V≤V+≤5.5V, Vo=1V, T_A=25˚C	75	105		dB
		2.7V≤V+≤5.5V, Vo=1V, Full Temperature Range	74			
CMRR	Common Mode Rejection Ratio(5)	-0.2V≤V_{CM}≤V+-1.2V	77	122		dB
CMIR	Input Common Mode Voltage Range(5)	CMRR≥77dB	-0.2		3.8	V
V_{OS}	Input Offset Voltage(5)	T_A=25˚C		±0.3	±1.0	mV
		Full Temperature Range			±1.2	
dV_{IO}	Average Drift(6)			±0.4	±2.0	μV/°C
I_{OS}	Input Offset Current			1		pA
		T_A=				
I_{bn_Char}	Input Bias Current(6)	T_A=25˚C		0.1	10.0	pA
		Full Temperature Range			500	
e_n	Input-Referred Voltage Noise	f=1kHz		11		nV/√Hz
		f=10kHz		10		nV/√Hz
i_N	Input-Referred Current Noise	f=1kHz		0.005		pA/√Hz

Continued on the following page…

Electrical Specifications at +5V

$+V_S$=+5V, $-V_S$ = 0V, V_{CM} = $+V_S/2$, and R_L = 10KΩ to $+V_S/2$, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_O	Output Voltage Swing High(5)	R_L=2kΩ to V+/2, T_A=25˚C		25	39	mV
		R_L=2kΩ to V+/2, Full Temperature Range			47	
		R_L=10kΩ to V+/2, T_A=25˚C		4	11	
		R_L=10kΩ to V+/2, Full Temperature Range			13	
	Output Voltage Swing Low(5)	R_L=2kΩ to V+/2, T_A=25˚C		24	38	mV
		R_L=2kΩ to V+/2, Full Temperature Range			50	
		R_L=10kΩ to V+/2, T_A=25˚C		3	15	
		R_L=10kΩ to V+/2, Full Temperature Range			1	
GBW	Gain Bandwidth Product			9		MHz
A_{VOL}	Large Signal Voltage Gain(6)	R_L=2kΩ, V_O=0.15 to 2.5V, V_O=4.85 to 2.5V, T_A=25˚C	105	118		dB
		R_L=2kΩ, V_O=0.15 to 2.5V, V_O=4.85 to 2.5V, Full Temperature Range	102			
		R_L=10kΩ, V_O=0.1 to 2.5V, V_O=4.9 to 2.5V, T_A=25˚C	105	120		
		R_L=10kΩ, V_O=0.1 to 2.5V, V_O=4.9 to 2.5V, Full Temperature Range	102			
R_{OUT}	Closed-Loop Impedance	f=6MHz		6		Ω
R_{IN}	Input Resistance			10		GΩ
C_{IN}	Input Capacitance	Common Mode		11		pF
		Differential Mode		6		
$Φ_M$	Phase Margin			94		˚
SR	Slew Rate	Av=+1, V_O=1V_{pp} 10%-90%		6.2		V/µs
THD+N	Total Harmonic Distortion + Noise	f=1kHz, Av=1, BW=>500kHz		0.006		%

Notes:
5. 100% tested at T_A=25°C.
6. Guaranteed by characterization.
7. EMI rejection ratio is defined as EMIRR – 20log (V_{RFpeak} / $ΔV_{OS}$).

Typical Performance Characteristics

$+V_S=+3.3V$, $-V_S = 0V$, $V_{CM} = +V_S/2$, and $R_L = 10K\Omega$ to $+V_S/2$, unless otherwise noted.

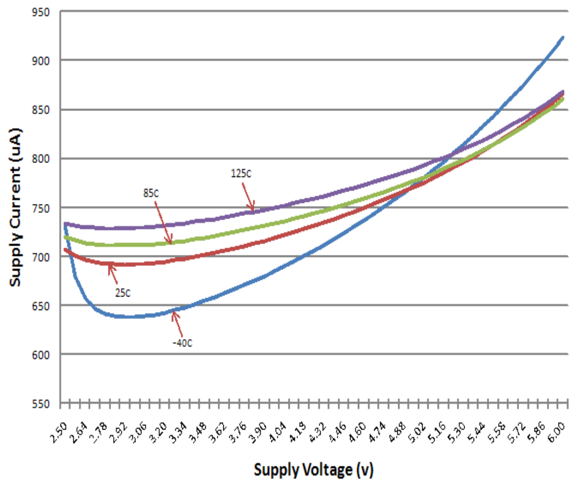

Figure 2. Supply Current vs. Supply Voltage

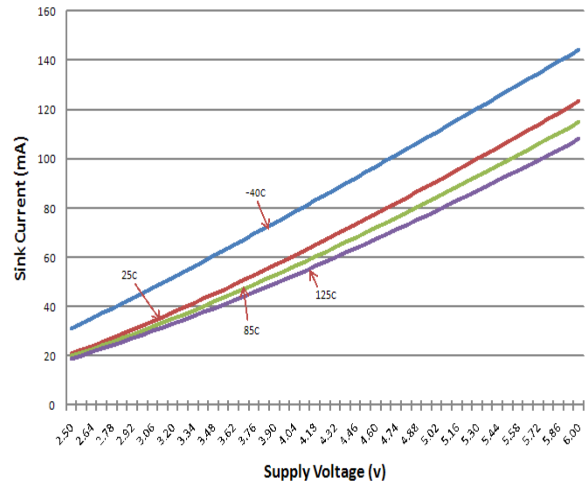

Figure 3. Sink Current vs. Supply Voltage

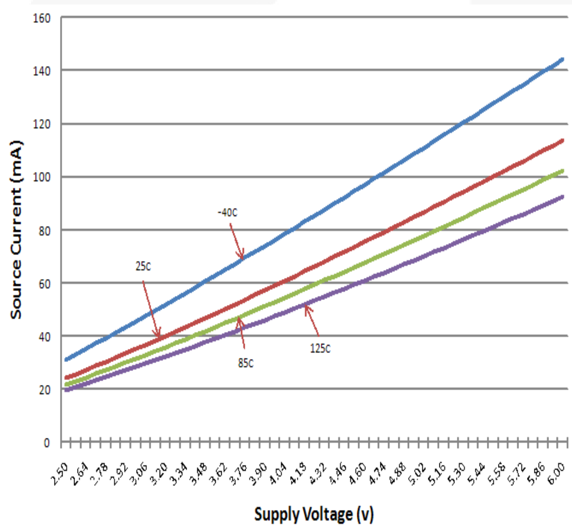

Figure 4. Source Current vs. Supply Voltage

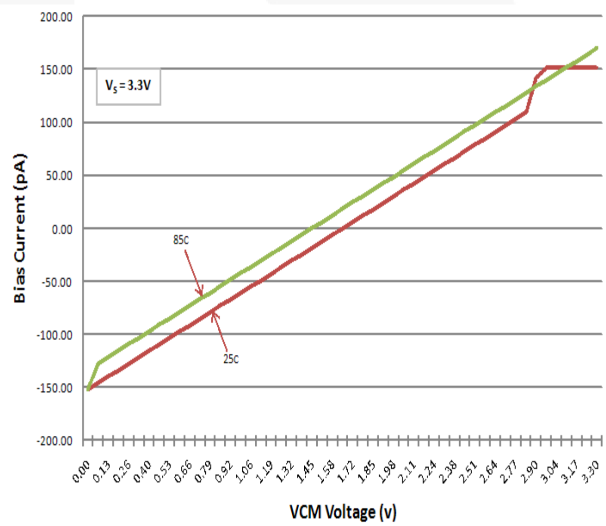

Figure 5. Input Bias Current vs. V_{CM} (3.3V)

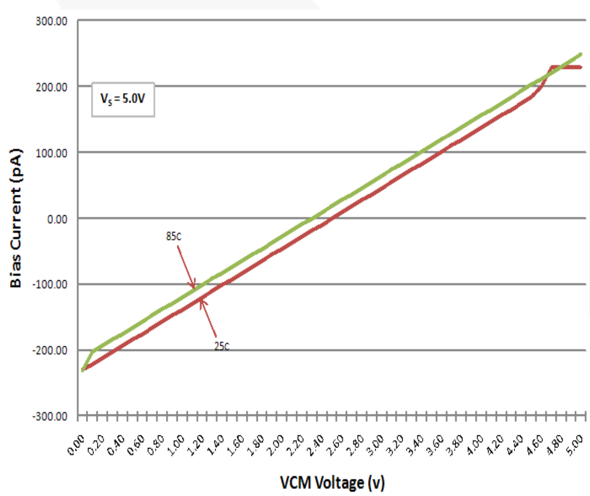

Figure 6. Input Bias Current vs. V_{CM} (5.0V)

Typical Performance Characteristics

$+V_S$=+3.3V, $-V_S$ = 0V, V_{CM} = $+V_S/2$, and R_L = 10KΩ to $+V_S/2$, unless otherwise noted.

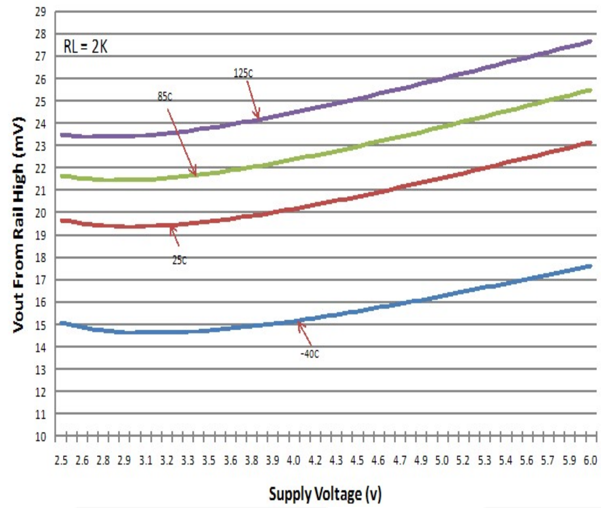

Figure 7. Output Swing High vs. Supply Voltage

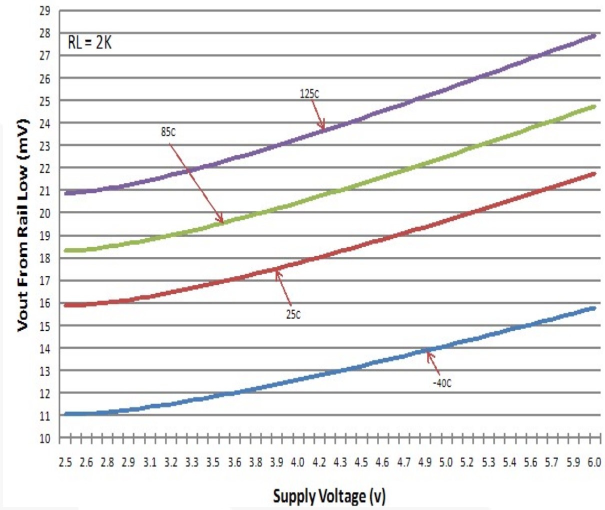

Figure 8. Output Swing Low vs. Supply Voltage

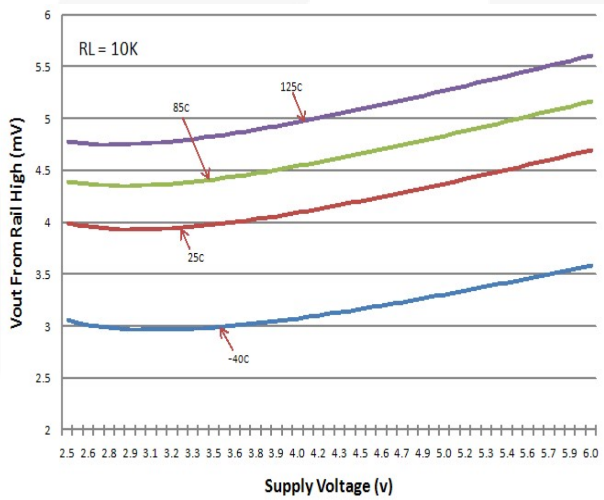

Figure 9. Output Swing High vs. Supply Voltage

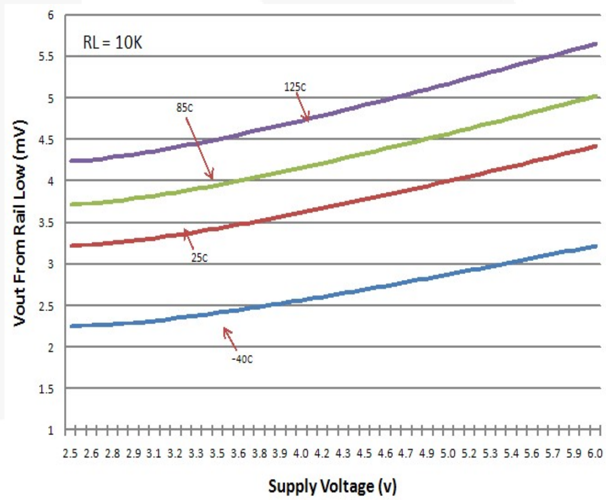

Figure 10. Output Swing Low vs. Supply Voltage

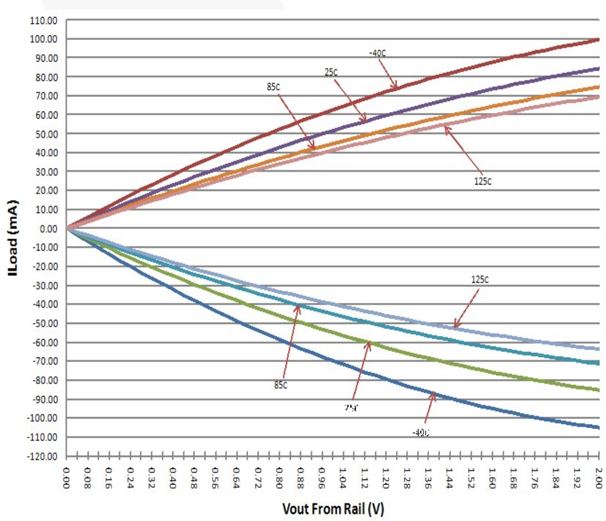

Figure 11. Output Voltage Swing vs. Load Current at 5.0V

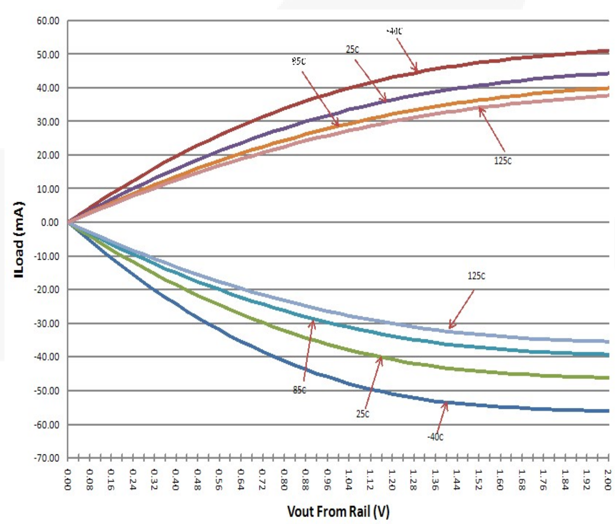

Figure 12. Output Voltage Swing vs. Load Current at 3.3V

Typical Performance Characteristics

$+V_S$=+3.3V, $-V_S$ = 0V, V_{CM} = $+V_S/2$, and R_L = 10KΩ to $+V_S/2$, unless otherwise noted.

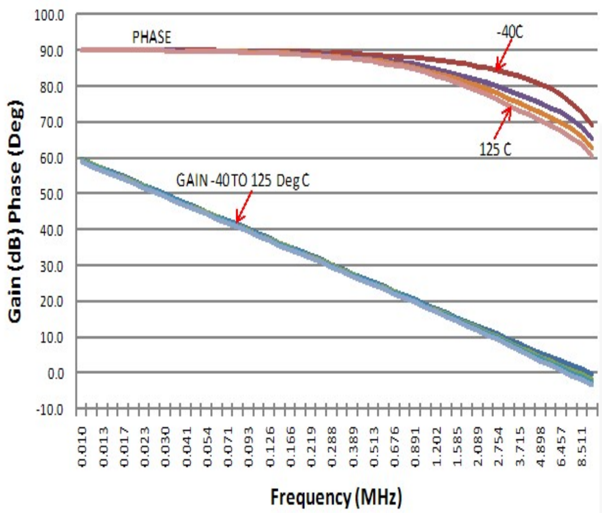

Figure 13. Open-Loop Gain/Phase vs. Temperature

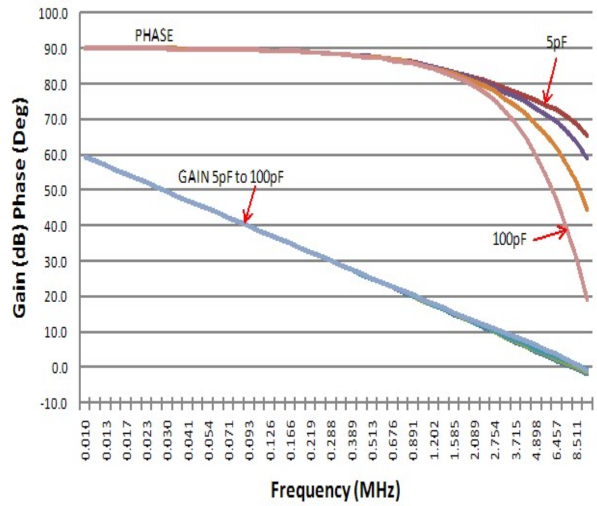

Figure 14. Open-Loop Gain/Phase vs. Load

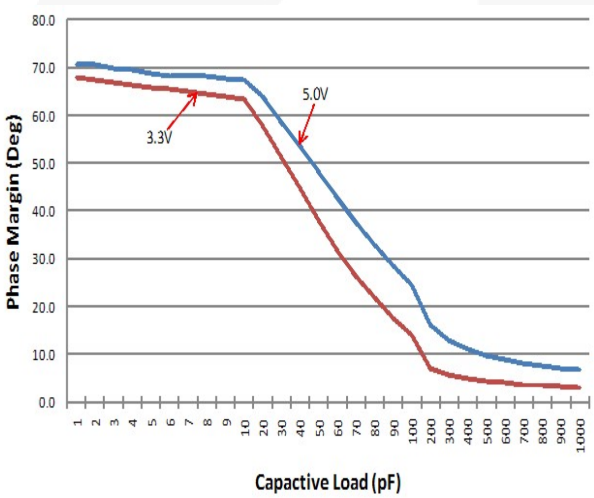

Figure 15. Phase Margin vs. Capacitive Load

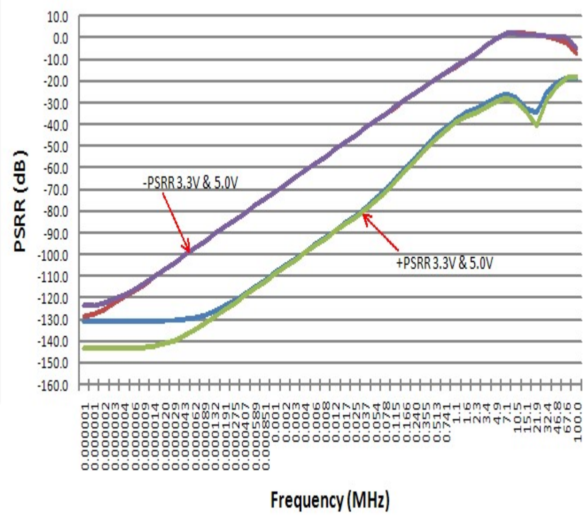

Figure 16. PSRR vs. Frequency

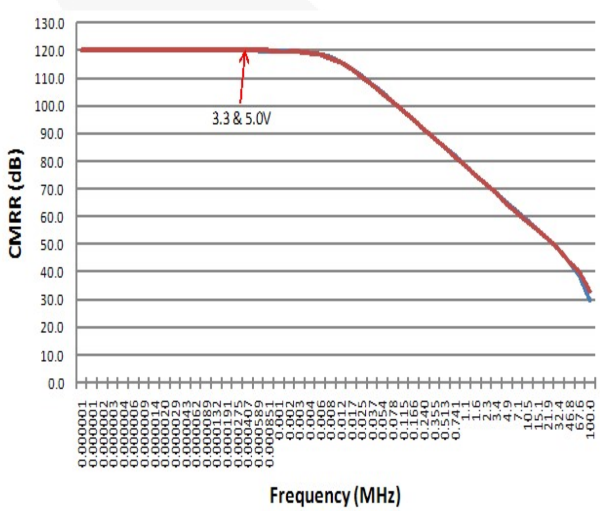

Figure 17. CMRR vs. Frequency

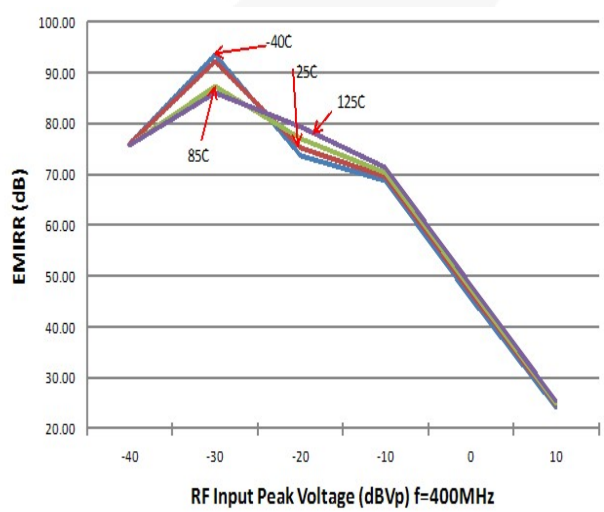

Figure 18. EMIRR vs. Power at 400MHz

Typical Performance Characteristics

+V_S=+3.3V, -V_S = 0V, V_{CM} = +V_S/2, and R_L = 10KΩ to +V_S/2, unless otherwise noted.

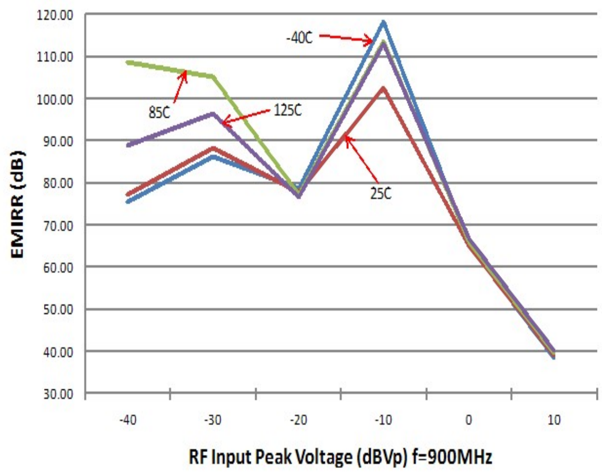

Figure 19. EMIRR vs. Power at 900MHz

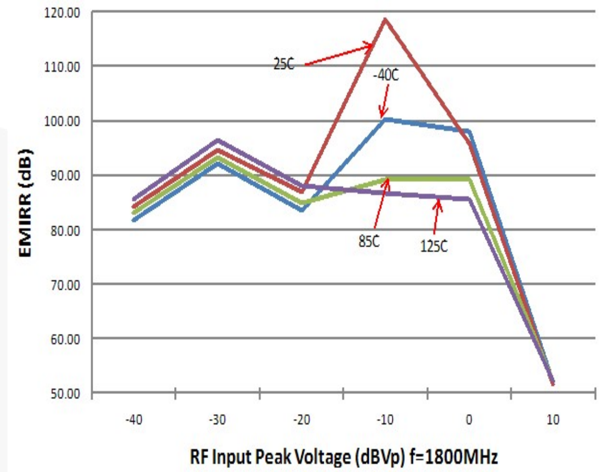

Figure 20. EMIRR vs. Power at 1800MHz

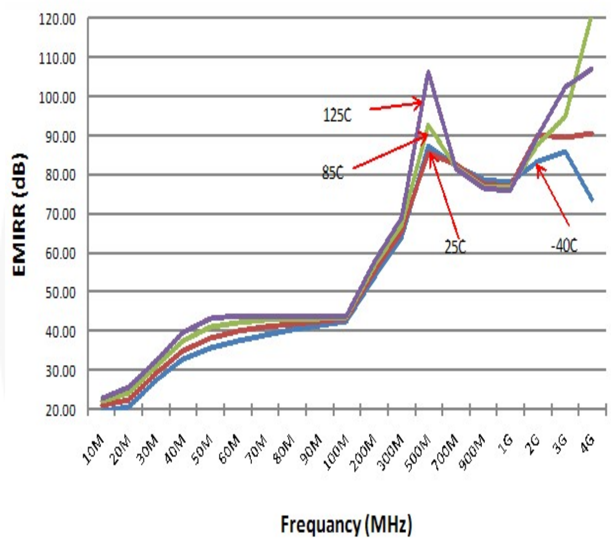

Figure 21. EMIRR vs. Frequency at 5.0V

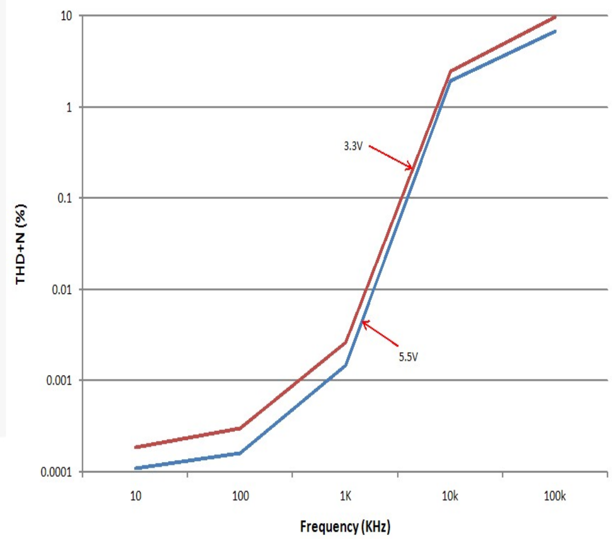

Figure 22. THD+N vs. Frequency

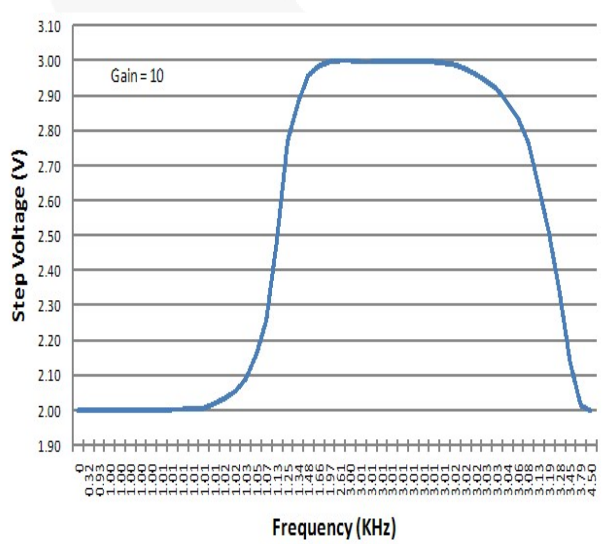

Figure 23. Large Signal Step Response

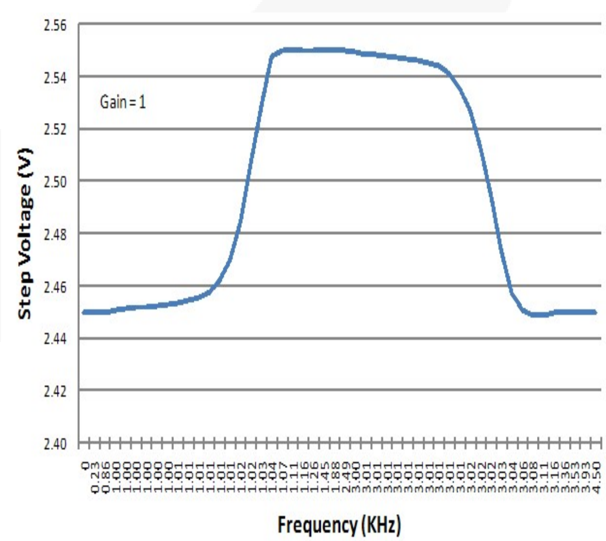

Figure 24. Small Signal Step Response

Typical Performance Characteristics

$+V_S$=+3.3V, $-V_S$ = 0V, V_{CM} = $+V_S/2$, and R_L = 10KΩ to $+V_S/2$, unless otherwise noted.

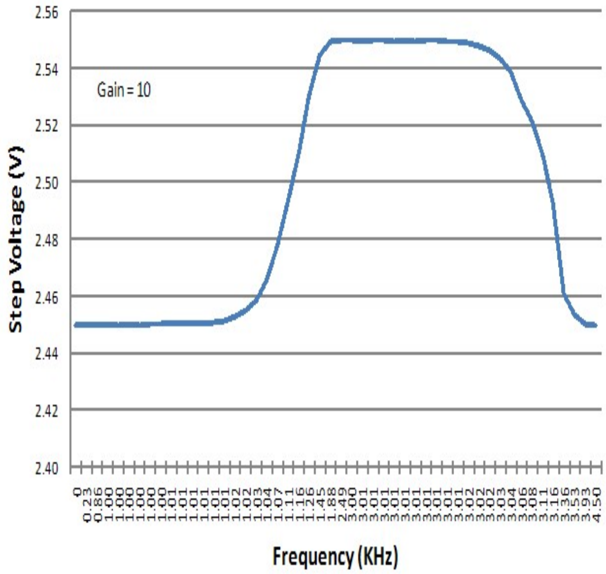

Figure 25. Small Signal Step Response

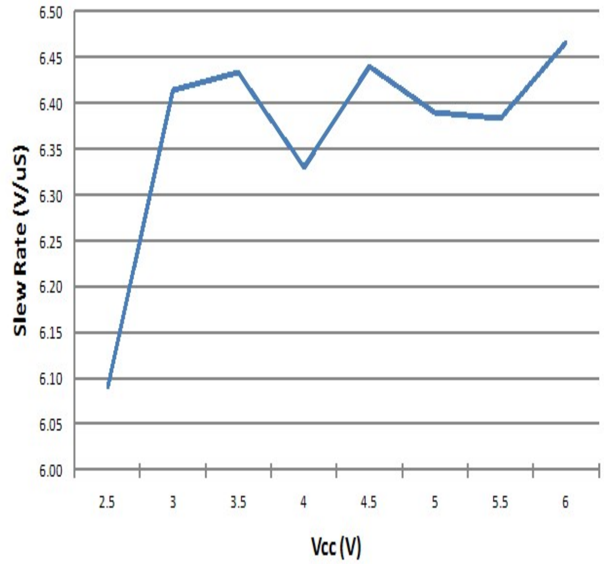

Figure 26. Slew Rate vs. Supply Voltage

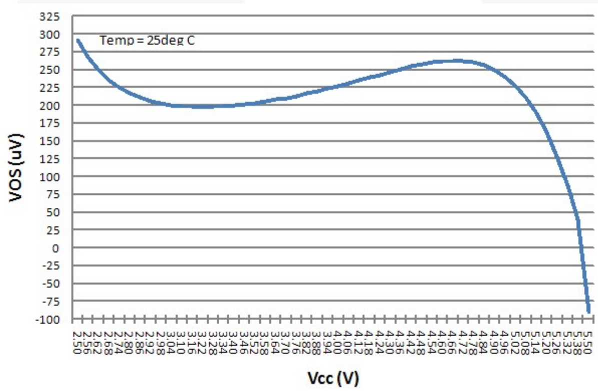

Figure 27. V_{OS} vs. Supply Voltage

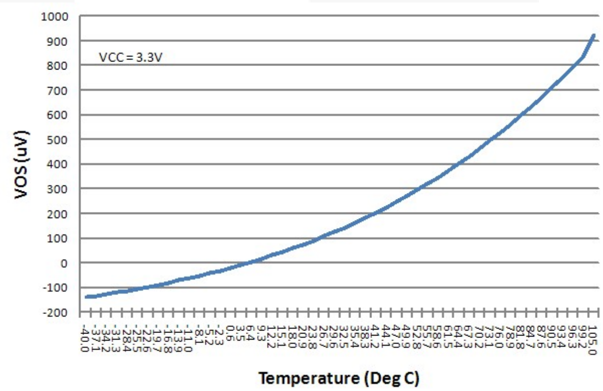

Figure 28. V_{OS} vs. Temperature

Application Information

General Description

The FAN4852 amplifier includes single-supply, general-purpose amplifiers, fabricated on a CMOS process. The input and output are rail-to-rail and the part is unity gain stable. The typical non-inverting circuit schematic is shown in Figure 29.

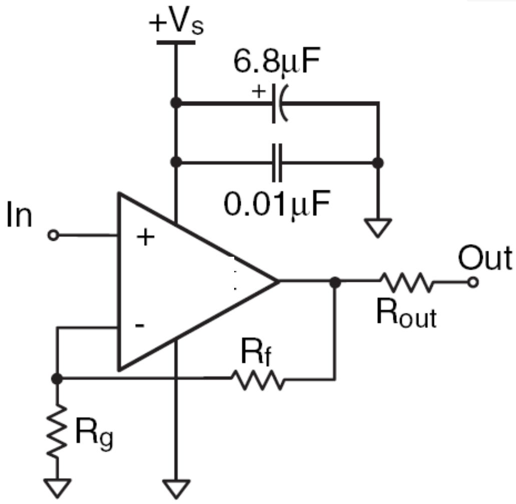

Figure 29. Typical Non-Inverting Configuration

Input Common Mode Voltage

The common mode input range includes ground. CMRR does not degrade when input levels are kept 1.2V below the rail. For the best CMRR when using a V_S of 5V, the maximum input voltage should 3.8V.

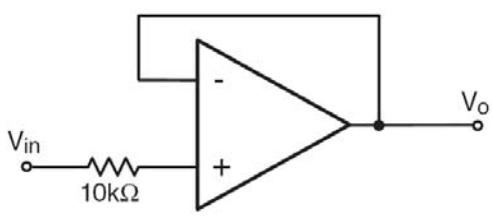

Figure 30. Circuit for Input Current Protection

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C, performance degradation occurs. If the maximum junction temperature exceeds 150°C for an extended time, device failure may occur.

Overdrive Recovery

Overdrive of an amplifier occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the range is exceeded. The FAN4852 typically recovers in less than 500ns from an overdrive condition. Figure 31 shows the FAN4852 amplifier in an overdriven condition.

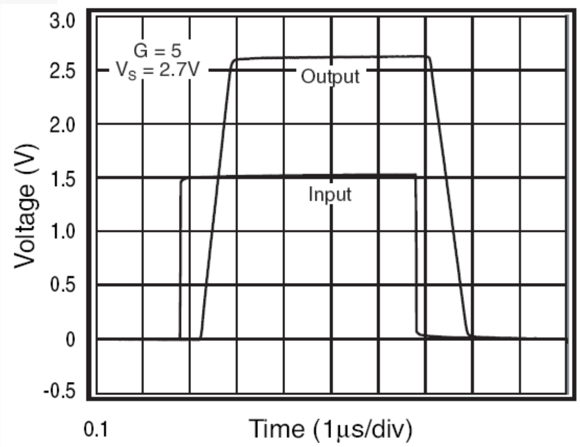

Figure 31. Overdrive Recovery

Driving Capacitive Loads

Figure 31 illustrates the response of the amplifier. A small series resistance (R_S) at the output, illustrated in Figure 32, improves stability and settling performance. R_S values provided achieve maximum bandwidth with less than 2dB of peaking. For maximum flatness, use a larger R_S. Capacitive loads larger than 500pF require the use of R_S.

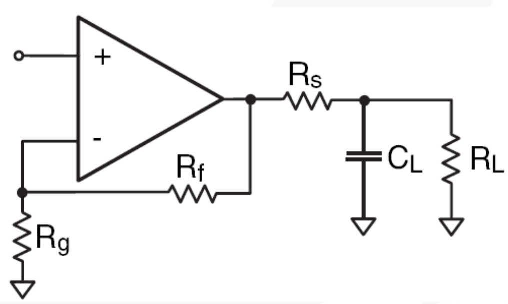

Figure 32. Typical Topology for Driving a Capacitive Load

Driving a capacitive load introduces phase-lag into the output signal, which reduces phase margin in the amplifier. The unity gain follower is the most sensitive configuration. In a unity gain follower configuration, the amplifier requires a 300Ω series resistor to drive a 100pF load.

Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance. Fairchild evaluation boards help guide high-frequency layout and aid in device testing and characterization. Follow the steps below as a basis for high-frequency layout:

1. Include 6.8µF and 0.01µF ceramic capacitors.
2. Place the 6.8µF capacitor within 0.75 inches of the power pin.
3. Place the 0.01µF capacitor within 0.1 inches of the power pin.
4. Remove the ground plane under and around the part, especially near the input and output pins, to reduce parasitic capacitance.

Minimize all trace lengths to reduce series inductances.

Refer to the evaluation board layouts shown in Figure 33 for more information.

When evaluating only one channel, complete the following on the unused channel:

1. Ground the non-inverting input.
2. Short the output to the inverting input.

Evaluation Board	Description
FAN4852-010	Single Channel, Dual Supply

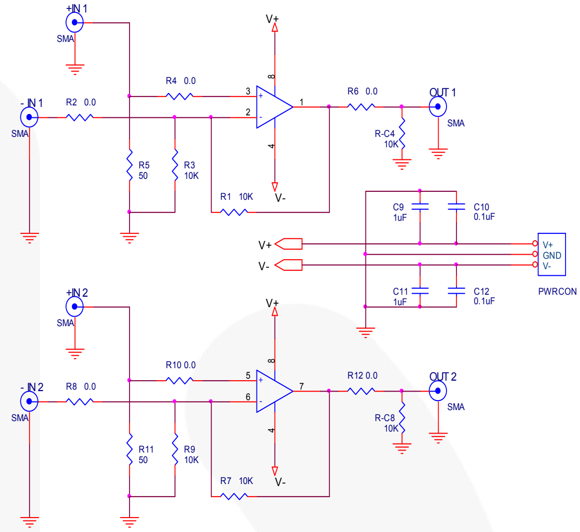

Figure 33. Evaluation Board Schematic

Physical Dimensions

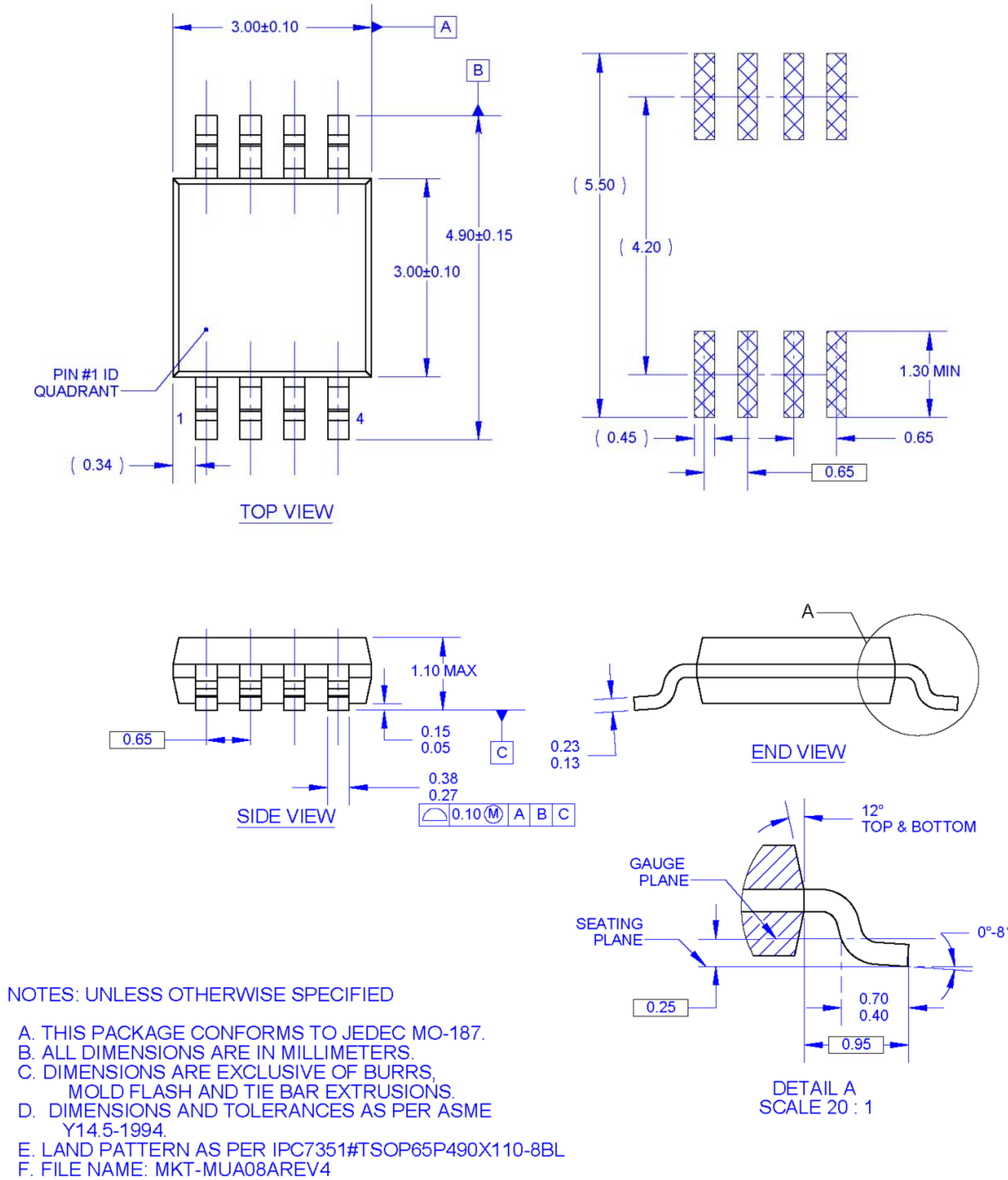

Figure 34. 8-Lead, Molded Small-Outline Package (MSOP)

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