

LMV431x Low-Voltage (1.24-V) Adjustable Precision Shunt Regulators

1 Features

- Low-Voltage Operation/Wide Adjust Range (1.24 V/30 V)
- 0.5% Initial Tolerance (LMV431B)
- Temperature Compensated for Industrial Temperature Range (39 PPM/°C for the LMV431A)
- Low Operation Current (55 μ A)
- Low Output Impedance (0.25 Ω)
- Fast Turn-On Response
- Low Cost

2 Applications

- Shunt Regulator
- Series Regulator
- Current Source or Sink
- Voltage Monitor
- Error Amplifier
- 3-V Off-Line Switching Regulator
- Low Dropout N-Channel Series Regulator

3 Description

The LMV431, LMV431A and LMV431B are precision 1.24 V shunt regulators capable of adjustment to 30 V. Negative feedback from the cathode to the adjust pin controls the cathode voltage, much like a non-inverting op amp configuration (Refer to [Symbol and Functional Diagrams](#)). A two-resistor voltage divider terminated at the adjust pin controls the gain of a 1.24 V band-gap reference. Shorting the cathode to the adjust pin (voltage follower) provides a cathode voltage of a 1.24 V.

The LMV431, LMV431A and LMV431B have respective initial tolerances of 1.5%, 1%, and 0.5%, and functionally lend themselves to several applications that require zener diode type performance at low voltages. Applications include a 3 V to 2.7 V low drop-out regulator, an error amplifier in a 3 V off-line switching regulator and even as a voltage detector. These parts are typically stable with capacitive loads greater than 10 nF and less than 50 pF.

The LMV431, LMV431A and LMV431B provide performance at a competitive price.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV431	SOT-23 (5)	2.90 mm x 1.60 mm
LMV431	TO-92 (3)	4.30 mm x 4.30 mm
LMV431	SOT-23 (3)	2.92 mm x 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Symbol and Functional Diagrams

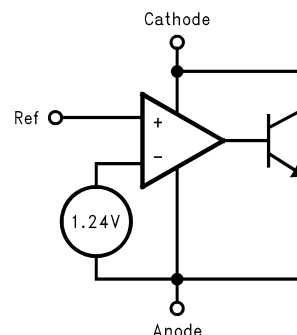
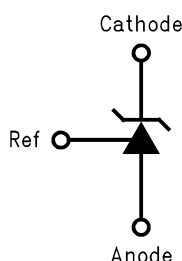


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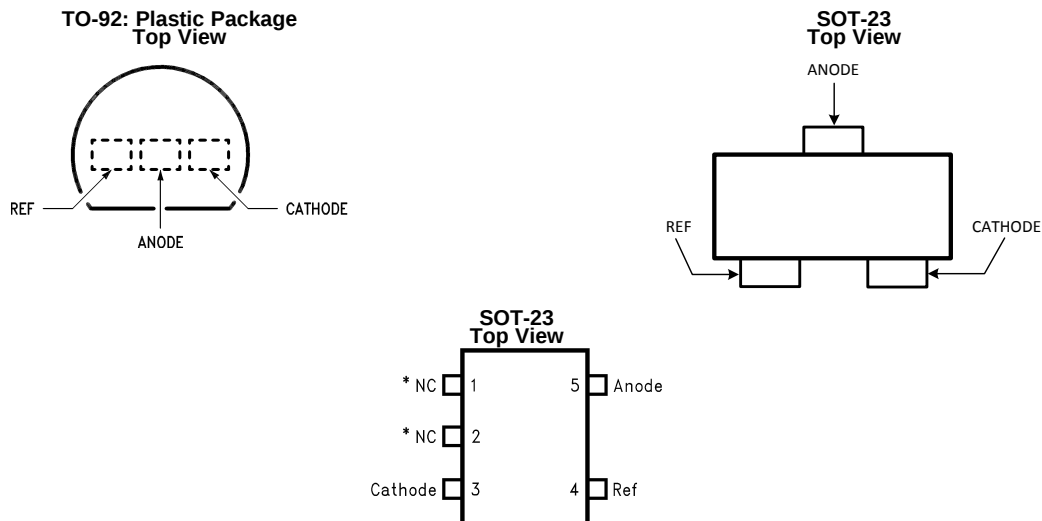
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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (May 2005) to Revision G	Page
Changed formatting to match new TI datasheet guidelines; added Device Information and Handling Ratings tables, Layout, and Device and Documentation Support sections; reformatted Detailed Description and Application and Implementation sections.	1
Added spec	4

6 Pin Configurations and Functions



*Pin 1 is not internally connected.

*Pin 2 is internally connected to Anode pin. Pin 2 should be either floating or connected to Anode pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Operating temperature	Industrial (LMV431AI, LMV431I)	–40	85	°C
	Commercial (LMV431AC, LMV431C, LMV431BC)	0	70	
Lead temperature	TO-92 Package/SOT-23 -5,-3 Package (Soldering, 10 sec.)		265	
Internal power dissipation ⁽²⁾	TO-92		0.78	W
	SOT-23-5, -3 Package		0.28	W
Cathode voltage			35	V
Continuous cathode current		–30	30	mA
Reference input current		–.05	3	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Ratings apply to ambient temperature at 25°C. Above this temperature, derate the TO-92 at 6.2 mW/°C, and the SOT-23-5 at 2.2 mW/°C. See derating curve in [Operating Condition](#) section.

7.2 Handling Ratings

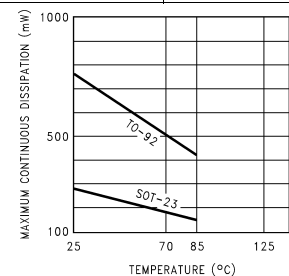
		MIN	MAX	UNIT
T _{stg}	Storage temperature range	–65	150	°C
V _(ESD)	Electrostatic discharge		2000	V
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾			

- (1) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Cathode voltage		V _{REF}		30	V
Cathode current		0.1		15	mA
Temperature	LMV431AI	–40		85	°C
Derating Curve (Slope = –1/R _{θJA})					



7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LMV431	LMV431	LMV431	UNIT
	SOT-23	SOT-23	TO-92	
	3 PINS	5 PINS	3 PINS	
R _{θJA} Junction-to-ambient thermal resistance ⁽²⁾	455	455	161	°C/W

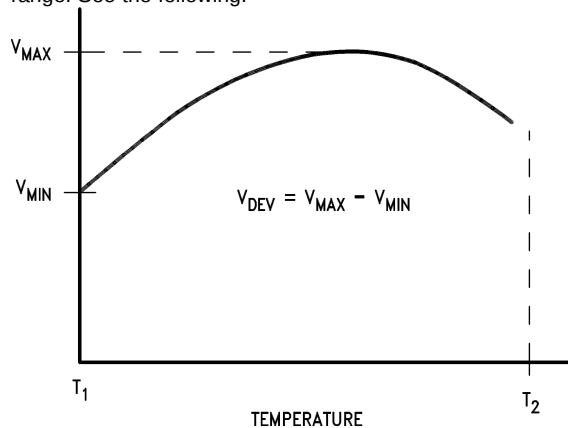
- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) T_{J Max} = 150°C, T_J = T_A + (R_{θJA} P_D), where P_D is the operating power of the device.

7.5 LMV431C Electrical Characteristics

T_A = 25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{REF}	Reference Voltage	V _Z = V _{REF} , I _Z = 10 mA (See Figure 32)	T _A = 25°C T _A = Full Range	1.222 1.24 1.258	1.21 1.27	V
V _{DEV}	Deviation of Reference Input Voltage Over Temperature ⁽¹⁾	V _Z = V _{REF} , I _Z = 10 mA, T _A = Full Range (See Figure 32)		4	12	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I _Z = 10 mA (see Figure 33) V _Z from V _{REF} to 6 V R ₁ = 10 kΩ, R ₂ = ∞ and 2.6 kΩ		-1.5	-2.7	mV/V
I _{REF}	Reference Input Current	R ₁ = 10 kΩ, R ₂ = ∞ I _I = 10 mA (see Figure 33)		0.15	0.5	μA
αI _{REF}	Deviation of Reference Input Current over Temperature	R ₁ = 10 kΩ, R ₂ = ∞, I _I = 10 mA, T _A = Full Range (see Figure 33)		0.05	0.3	μA
I _{Z(MIN)}	Minimum Cathode Current for Regulation	V _Z = V _{REF} (see Figure 32)		55	80	μA
I _{Z(OFF)}	Off-State Current	V _Z = 6 V, V _{REF} = 0 V (see Figure 34)		0.001	0.1	μA
r _Z	Dynamic Output Impedance ⁽²⁾	V _Z = V _{REF} , I _Z = 0.1 mA to 15 mA Frequency = 0 Hz (see Figure 32)		0.25	0.4	Ω

- (1) Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range. See the following:



The average temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\alpha V_{REF} \frac{\text{ppm}}{^{\circ}\text{C}} = \frac{\pm \left(\frac{V_{MAX} - V_{MIN}}{V_{REF}(\text{at } 25^{\circ}\text{C})} \right) 10^6}{T_2 - T_1} = \frac{\pm \left(\frac{V_{DEV}}{V_{REF}(\text{at } 25^{\circ}\text{C})} \right) 10^6}{T_2 - T_1}$$

Where: T₂ - T₁ = full temperature change. αV_{REF} can be positive or negative depending on whether the slope is positive or negative.

Example: V_{DEV} = 6 mV, V_{REF} = 1240 mV, T₂ - T₁ = 125°C.

$$\alpha V_{REF} = \frac{\left(\frac{6.0 \text{ mV}}{1240 \text{ mV}} \right) 10^6}{125^{\circ}\text{C}} = +39 \text{ ppm} / ^{\circ}\text{C}$$

- (2) The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R₁ and R₂, (see [Figure 33](#)), the dynamic output impedance of the overall circuit, r_Z, is defined as:

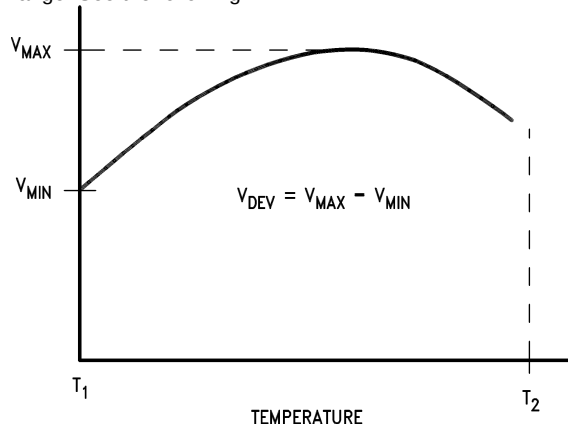
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z \left(1 + \frac{R_1}{R_2} \right) \right]$$

7.6 LMV431I Electrical Characteristics

T_A = 25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{REF}	Reference Voltage	V _Z = V _{REF} , I _Z = 10 mA (See Figure 32)	T _A = 25°C 1.222	1.24	1.258	V
		T _A = Full Range	1.202		1.278	
V _{DEV}	Deviation of Reference Input Voltage Over Temperature ⁽¹⁾	V _Z = V _{REF} , I _Z = 10 mA, T _A = Full Range (See Figure 32)		6	20	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I _Z = 10mA (see Figure 33) V _Z from V _{REF} to 6V R ₁ = 10 kΩ, R ₂ = ∞ and 2.6kΩ		-1.5	-2.7	mV/V
I _{REF}	Reference Input Current	R ₁ = 10 kΩ, R ₂ = ∞ I _I = 10 mA (see Figure 33)		0.15	0.5	μA
α _{IREF}	Deviation of Reference Input Current over Temperature	R ₁ = 10 kΩ, R ₂ = ∞, I _I = 10 mA, T _A = Full Range (see Figure 33)		0.1	0.4	μA
I _{Z(MIN)}	Minimum Cathode Current for Regulation	V _Z = V _{REF} (see Figure 32)		55	80	μA
I _{Z(OFF)}	Off-State Current	V _Z = 6 V, V _{REF} = 0V (see Figure 34)		0.001	0.1	μA
r _Z	Dynamic Output Impedance ⁽²⁾	V _Z = V _{REF} , I _Z = 0.1 mA to 15 mA Frequency = 0 Hz (see Figure 32)		0.25	0.4	Ω

- (1) Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range. See the following:



The average temperature coefficient of the reference input voltage, α_{VREF}, is defined as:

$$\alpha_{V_{REF}} \frac{\text{ppm}}{^{\circ}\text{C}} = \frac{\pm \left(\frac{V_{\text{Max}} - V_{\text{Min}}}{V_{REF}(\text{at } 25^{\circ}\text{C})} \right) 10^6}{T_2 - T_1} = \frac{\pm \left(\frac{V_{DEV}}{V_{REF}(\text{at } 25^{\circ}\text{C})} \right) 10^6}{T_2 - T_1}$$

Where: T₂ – T₁ = full temperature change. α_{VREF} can be positive or negative depending on whether the slope is positive or negative.

Example: V_{DEV} = 6 mV, V_{REF} = 1240 mV, T₂ – T₁ = 125°C.

$$\alpha_{V_{REF}} = \frac{\left(\frac{6.0 \text{ mV}}{1240 \text{ mV}} \right) 10^6}{125^{\circ}\text{C}} = +39 \text{ ppm} / ^{\circ}\text{C}$$

- (2) The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R₁ and R₂, (see [Figure 33](#)), the dynamic output impedance of the overall circuit, r_Z, is defined as:

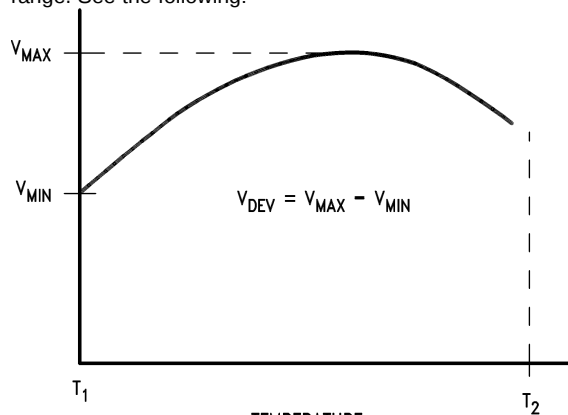
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z \left(1 + \frac{R_1}{R_2} \right) \right]$$

7.7 LMV431AC Electrical Characteristics

T_A = 25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{REF}	Reference Voltage	V _Z = V _{REF} , I _Z = 10 mA (See Figure 32)	1.228	1.24	1.252	V
		T _A = 25°C				
		T _A = Full Range	1.221		1.259	
V _{DEV}	Deviation of Reference Input Voltage Over Temperature ⁽¹⁾	V _Z = V _{REF} , I _Z = 10 mA, T _A = Full Range (See Figure 32)		4	12	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I _Z = 10 mA (see Figure 33) V _Z from V _{REF} to 6 V R ₁ = 10 kΩ, R ₂ = ∞ and 2.6 kΩ		-1.5	-2.7	mV/V
I _{REF}	Reference Input Current	R ₁ = 1 kΩ, R ₂ = ∞ I _I = 10 mA (see Figure 33)		0.15	0.50	μA
αI _{REF}	Deviation of Reference Input Current over Temperature	R ₁ = 10 kΩ, R ₂ = ∞, I _I = 10 mA, T _A = Full Range (see Figure 33)		0.05	0.3	μA
I _{Z(MIN)}	Minimum Cathode Current for Regulation	V _Z = V _{REF} (see Figure 32)		55	80	μA
I _{Z(OFF)}	Off-State Current	V _Z = 6 V, V _{REF} = 0V (see Figure 34)		0.001	0.1	μA
r _Z	Dynamic Output Impedance ⁽²⁾	V _Z = V _{REF} , I _Z = 0.1mA to 15mA Frequency = 0 Hz (see Figure 32)		0.25	0.4	Ω

- (1) Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range. See the following:



The average temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\alpha V_{REF} \frac{\text{ppm}}{^{\circ}\text{C}} = \frac{\pm \left(\frac{V_{MAX} - V_{MIN}}{V_{REF}(\text{at } 25^{\circ}\text{C})} \right) 10^6}{T_2 - T_1} = \pm \left(\frac{V_{DEV}}{V_{REF}(\text{at } 25^{\circ}\text{C})} \right) 10^6$$

Where: T₂ - T₁ = full temperature change. αV_{REF} can be positive or negative depending on whether the slope is positive or negative.

Example: V_{DEV} = 6 mV, V_{REF} = 1240 mV, T₂ - T₁ = 125°C.

$$\alpha V_{REF} = \frac{\left(\frac{6.0 \text{ mV}}{1240 \text{ mV}} \right) 10^6}{125^{\circ}\text{C}} = +39 \text{ ppm} / ^{\circ}\text{C}$$

- (2) The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R₁ and R₂, (see [Figure 33](#)), the dynamic output impedance of the overall circuit, r_Z, is defined as:

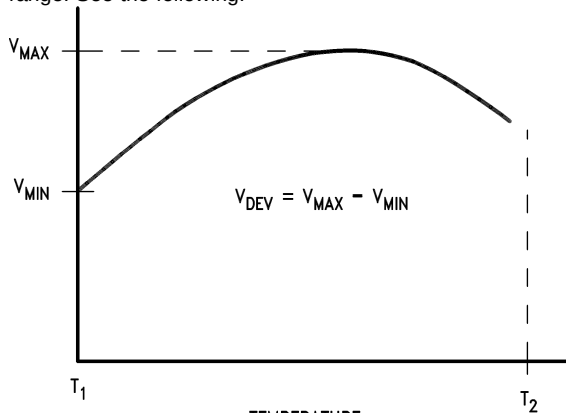
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z \left(1 + \frac{R_1}{R_2} \right) \right]$$

7.8 LMV431AI Electrical Characteristics

T_A = 25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{REF}	Reference Voltage	V _Z = V _{REF} , I _Z = 10mA (See Figure 32)	T _A = 25°C 1.228	1.24	1.252	V
		T _A = Full Range	1.215		1.265	V
V _{DEV}	Deviation of Reference Input Voltage Over Temperature ⁽¹⁾	V _Z = V _{REF} , I _Z = 10mA, T _A = Full Range (See Figure 32)		6	20	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I _Z = 10mA (see Figure 33) V _Z from V _{REF} to 6 V R ₁ = 10 kΩ, R ₂ = ∞ and 2.6 kΩ		-1.5	-2.7	mV/V
I _{REF}	Reference Input Current	R ₁ = 10 kΩ, R ₂ = ∞ I _I = 10 mA (see Figure 33)		0.15	0.5	μA
αI _{REF}	Deviation of Reference Input Current over Temperature	R ₁ = 10 kΩ, R ₂ = ∞, I _I = 10 mA, T _A = Full Range (see Figure 33)		0.1	0.4	μA
I _{Z(MIN)}	Minimum Cathode Current for Regulation	V _Z = V _{REF} (see Figure 32)		55	80	μA
I _{Z(OFF)}	Off-State Current	V _Z = 6 V, V _{REF} = 0 V (see Figure 34)		0.001	0.1	μA
r _Z	Dynamic Output Impedance ⁽²⁾	V _Z = V _{REF} , I _Z = 0.1 mA to 15 mA Frequency = 0 Hz (see Figure 32)		0.25	0.4	Ω

- (1) Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range. See the following:



The average temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\alpha V_{REF} \frac{\text{ppm}}{^{\circ}\text{C}} = \frac{\pm \left(\frac{V_{MAX} - V_{MIN}}{V_{REF}(\text{at } 25^{\circ}\text{C})} \right) 10^6}{T_2 - T_1} = \pm \left(\frac{V_{DEV}}{V_{REF}(\text{at } 25^{\circ}\text{C})} \right) 10^6$$

Where: T₂ - T₁ = full temperature change. αV_{REF} can be positive or negative depending on whether the slope is positive or negative.

Example: V_{DEV} = 6 mV, V_{REF} = 1240 mV, T₂ - T₁ = 125°C.

$$\alpha V_{REF} = \frac{\left(\frac{6.0 \text{ mV}}{1240 \text{ mV}} \right) 10^6}{125^{\circ}\text{C}} = +39 \text{ ppm} / ^{\circ}\text{C}$$

- (2) The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R₁ and R₂, (see [Figure 33](#)), the dynamic output impedance of the overall circuit, r_Z, is defined as:

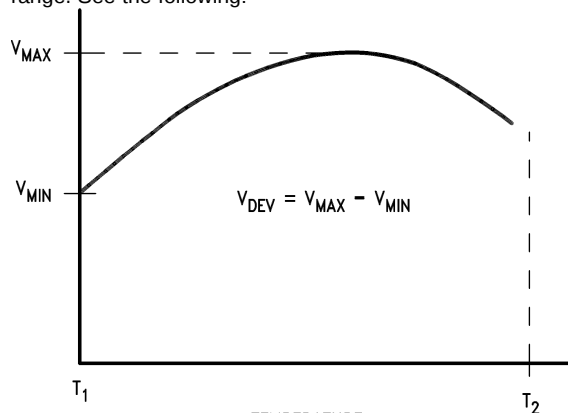
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z \left(1 + \frac{R_1}{R_2} \right) \right]$$

7.9 LMV431BC Electrical Characteristics

T_A = 25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{REF}	Reference Voltage	V _Z = V _{REF} , I _Z = 10 mA (See Figure 32)	1.234	1.24	1.246	V
		T _A = 25°C				
		T _A = Full Range	1.227		1.253	V
V _{DEV}	Deviation of Reference Input Voltage Over Temperature ⁽¹⁾	V _Z = V _{REF} , I _Z = 10 mA, T _A = Full Range (See Figure 32)		4	12	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I _Z = 10 mA (see Figure 33) V _Z from V _{REF} to 6 V R ₁ = 10 kΩ, R ₂ = ∞ and 2.6 kΩ		-1.5	-2.7	mV/V
I _{REF}	Reference Input Current	R ₁ = 10 kΩ, R ₂ = ∞ I _I = 10 mA (see Figure 33)		0.15	0.50	μA
αI _{REF}	Deviation of Reference Input Current over Temperature	R ₁ = 10 kΩ, R ₂ = ∞, I _I = 10 mA, T _A = Full Range (see Figure 33)		0.05	0.3	μA
I _{Z(MIN)}	Minimum Cathode Current for Regulation	V _Z = V _{REF} (see Figure 32)		55	80	μA
I _{Z(OFF)}	Off-State Current	V _Z = 6 V, V _{REF} = 0V (see Figure 34)		0.001	0.1	μA
r _Z	Dynamic Output Impedance ⁽²⁾	V _Z = V _{REF} , I _Z = 0.1mA to 15mA Frequency = 0 Hz (see Figure 32)		0.25	0.4	Ω

- (1) Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range. See the following:



The average temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\alpha V_{REF} \frac{\text{ppm}}{^{\circ}\text{C}} = \frac{\pm \left(\frac{V_{MAX} - V_{MIN}}{V_{REF}(\text{at } 25^{\circ}\text{C})} \right) 10^6}{T_2 - T_1} = \pm \left(\frac{V_{DEV}}{V_{REF}(\text{at } 25^{\circ}\text{C})} \right) 10^6$$

Where: T₂ - T₁ = full temperature change. αV_{REF} can be positive or negative depending on whether the slope is positive or negative.

Example: V_{DEV} = 6 mV, V_{REF} = 1240 mV, T₂ - T₁ = 125°C.

$$\alpha V_{REF} = \frac{\left(\frac{6.0 \text{ mV}}{1240 \text{ mV}} \right) 10^6}{125^{\circ}\text{C}} = +39 \text{ ppm} / ^{\circ}\text{C}$$

- (2) The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R₁ and R₂, (see [Figure 33](#)), the dynamic output impedance of the overall circuit, r_Z, is defined as:

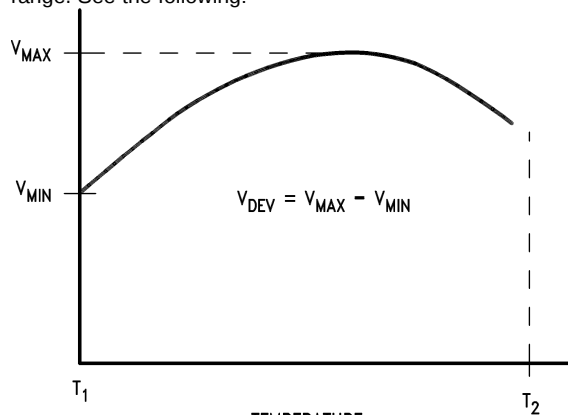
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z \left(1 + \frac{R_1}{R_2} \right) \right]$$

7.10 LMV431BI Electrical Characteristics

T_A = 25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{REF}	Reference Voltage	V _Z = V _{REF} , I _Z = 10 mA (See Figure 32)	T _A = 25°C 1.234	1.24	1.246	V
		T _A = Full Range	1.224		1.259	V
V _{DEV}	Deviation of Reference Input Voltage Over Temperature ⁽¹⁾	V _Z = V _{REF} , I _Z = 10 mA, T _A = Full Range (See Figure 32)		6	20	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I _Z = 10 mA (see Figure 33) V _Z from V _{REF} to 6V R ₁ = 10 kΩ, R ₂ = ∞ and 2.6 kΩ		-1.5	-2.7	mV/V
I _{REF}	Reference Input Current	R ₁ = 10 kΩ, R ₂ = ∞ I _I = 10 mA (see Figure 33)		0.15	0.50	μA
αI _{REF}	Deviation of Reference Input Current over Temperature	R ₁ = 10 kΩ, R ₂ = ∞, I _I = 10 mA, T _A = Full Range (see Figure 33)		0.1	0.4	μA
I _{Z(MIN)}	Minimum Cathode Current for Regulation	V _Z = V _{REF} (see Figure 32)		55	80	μA
I _{Z(OFF)}	Off-State Current	V _Z = 6 V, V _{REF} = 0 V (see Figure 34)		0.001	0.1	μA
r _Z	Dynamic Output Impedance ⁽²⁾	V _Z = V _{REF} , I _Z = 0.1 mA to 15 mA Frequency = 0 Hz (see Figure 32)		0.25	0.4	Ω

- (1) Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range. See the following:



The average temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\alpha V_{REF} \frac{\text{ppm}}{^{\circ}\text{C}} = \frac{\pm \left(\frac{V_{\text{Max}} - V_{\text{Min}}}{V_{REF}(\text{at } 25^{\circ}\text{C})} \right) 10^6}{T_2 - T_1} = \pm \left(\frac{V_{DEV}}{V_{REF}(\text{at } 25^{\circ}\text{C})} \right) 10^6$$

Where: T₂ - T₁ = full temperature change. αV_{REF} can be positive or negative depending on whether the slope is positive or negative.

Example: V_{DEV} = 6 mV, V_{REF} = 1240 mV, T₂ - T₁ = 125°C.

$$\alpha V_{REF} = \frac{\left(\frac{6.0 \text{ mV}}{1240 \text{ mV}} \right) 10^6}{125^{\circ}\text{C}} = +39 \text{ ppm} / ^{\circ}\text{C}$$

- (2) The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R₁ and R₂, (see [Figure 33](#)), the dynamic output impedance of the overall circuit, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z \left(1 + \frac{R_1}{R_2} \right) \right]$$

7.11 Typical Performance Characteristics

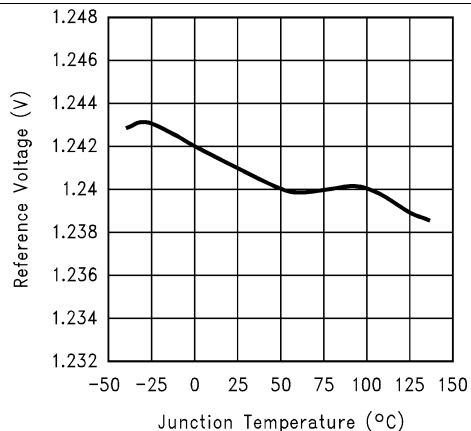


Figure 1. Reference Voltage vs. Junction Temperature

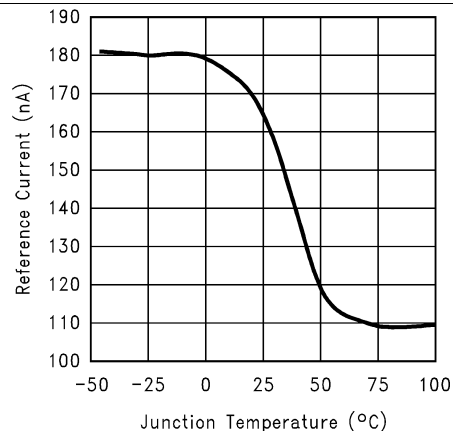


Figure 2. Reference Input Current vs. Junction Temperature

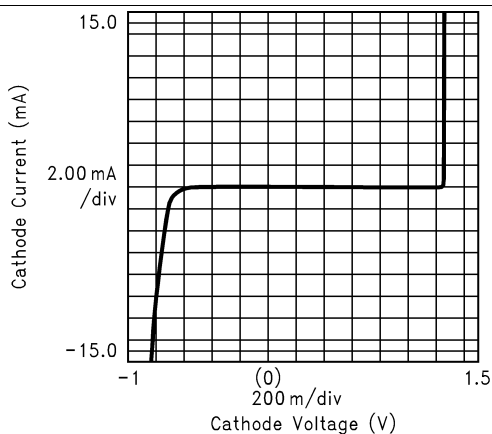


Figure 3. Cathode Current vs. Cathode Voltage 1

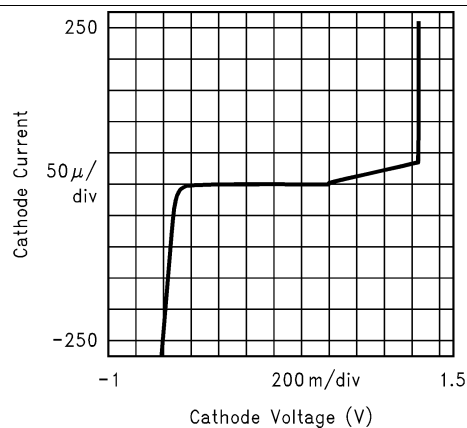


Figure 4. Cathode Current vs. Cathode Voltage 2

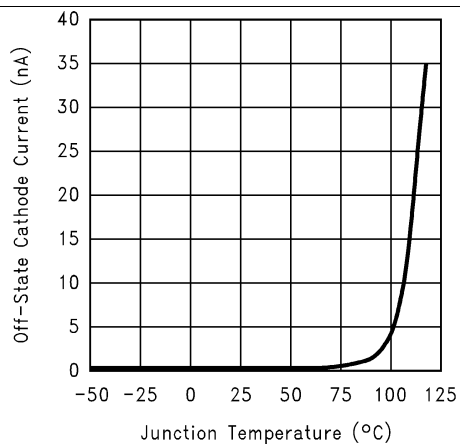


Figure 5. Off-State Cathode Current vs. Junction Temperature

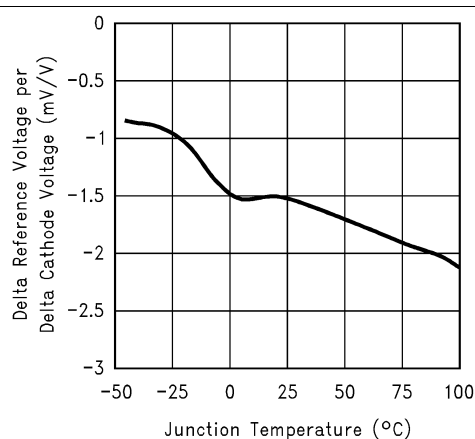
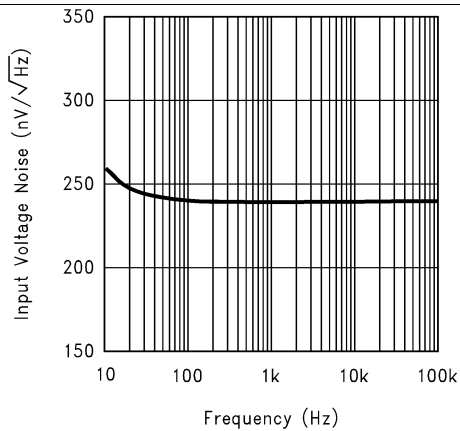
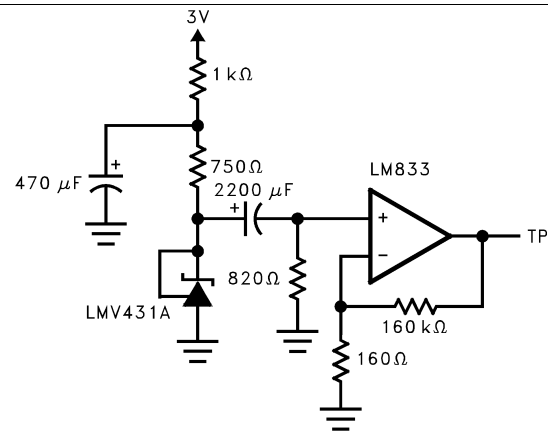
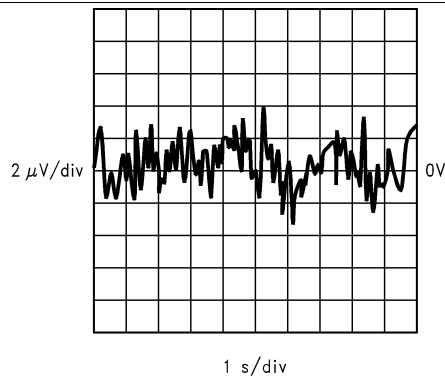
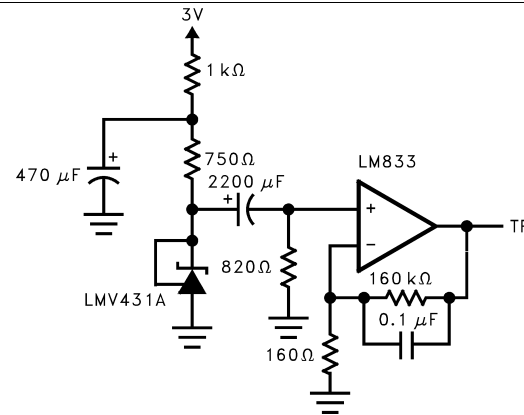
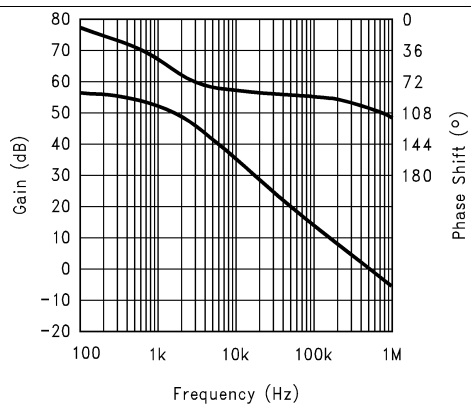
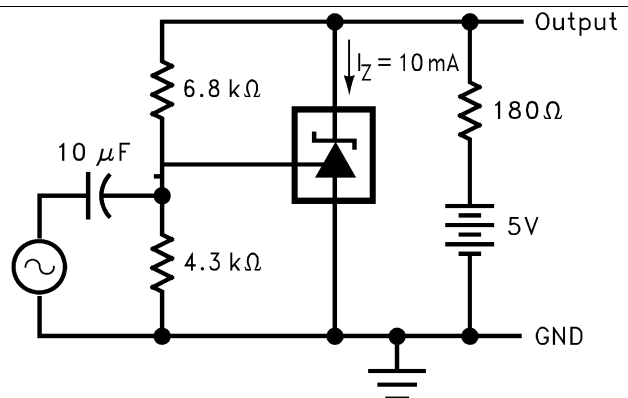


Figure 6. Delta Reference Voltage Per Delta Cathode Voltage vs. Junction Temperature

Typical Performance Characteristics (continued)


Figure 7. Input Voltage Noise vs. Frequency

Figure 8. Test Circuit For Input Voltage Noise vs. Frequency

Figure 9. Low Frequency Peak To Peak Noise


BW = 0.1 Hz To 10 Hz

Figure 10. Test Circuit For Peak To Peak Noise

Figure 11. Small Signal Voltage Gain And Phase Shift vs. Frequency

Figure 12. Test Circuit For Voltage Gain And Phase Shift vs. Frequency

Typical Performance Characteristics (continued)

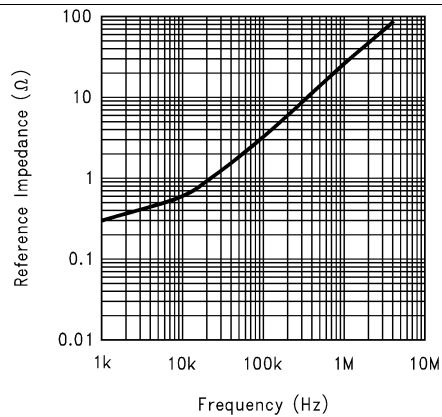


Figure 13. Reference Impedance vs. Frequency

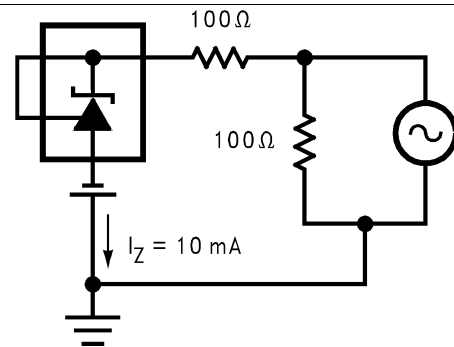


Figure 14. Test Circuit For Reference Impedance vs. Frequency

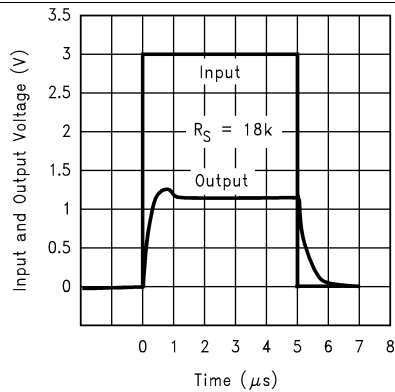


Figure 15. Pulse Response 1

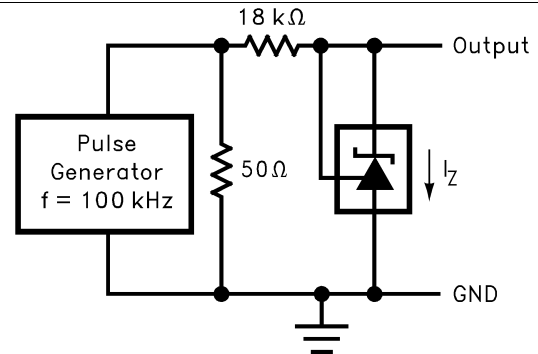


Figure 16. Test Circuit For Pulse Response 1

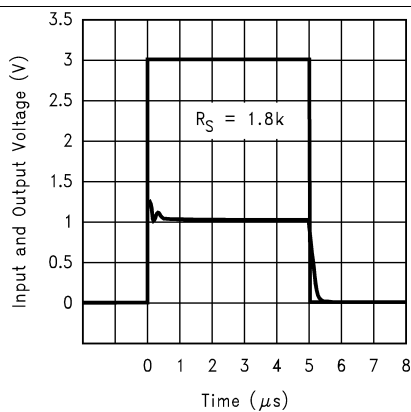


Figure 17. Pulse Response 2

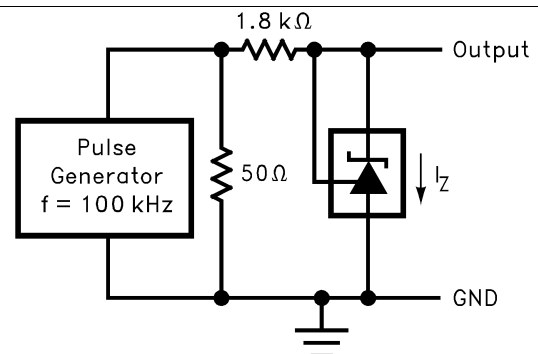
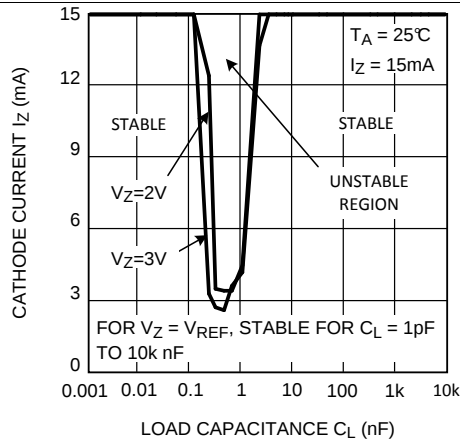
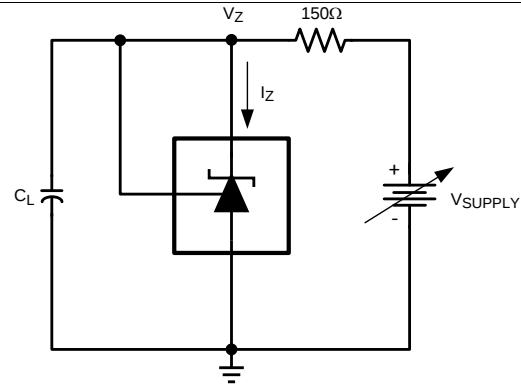
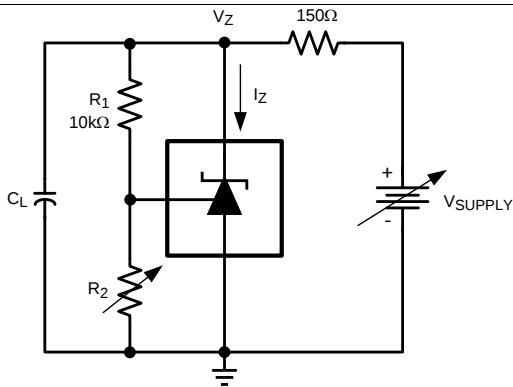
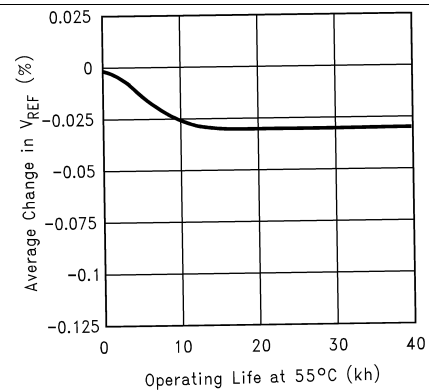


Figure 18. Test Circuit For Pulse Response 2

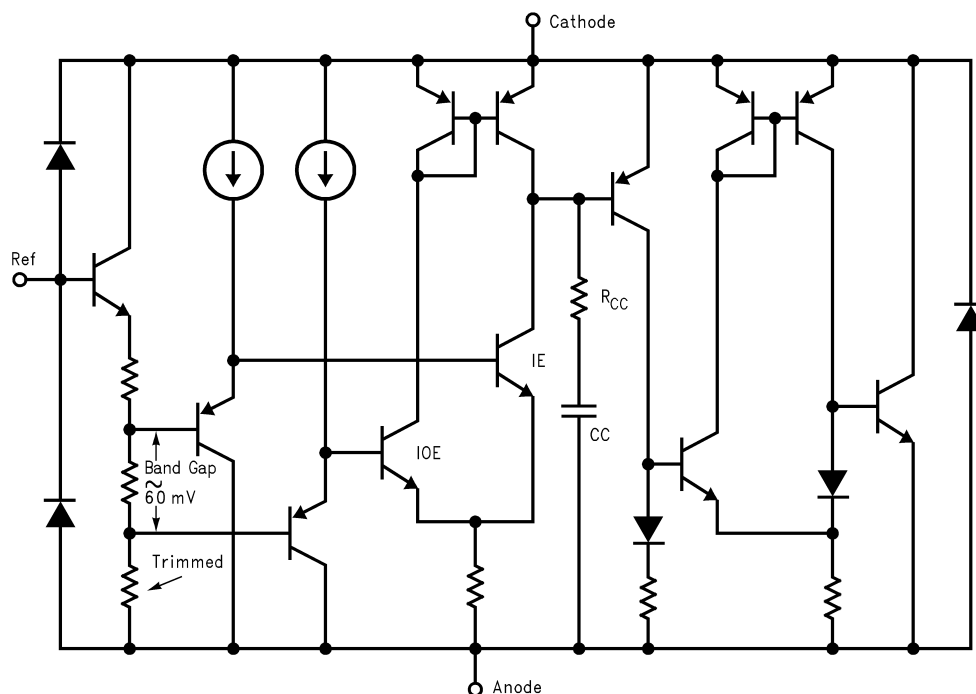
Typical Performance Characteristics (continued)

Figure 19. LMV431 Stability Boundary Condition

Figure 20. Test Circuit For $V_Z = V_{REF}$

Figure 21. Test Circuit For $V_Z = 2V, 3V$


Extrapolated from life-test data taken at 125°C; the activation energy assumed is 0.7eV.

Figure 22. Percentage Change In V_{REF} vs. Operating Life At 55°C

8 Detailed Description

8.1 Functional Block Diagram



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

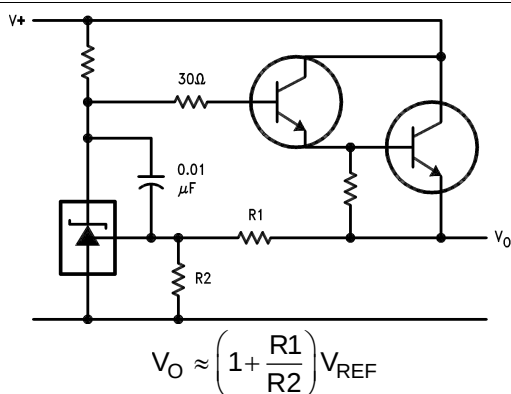


Figure 23. Series Regulator

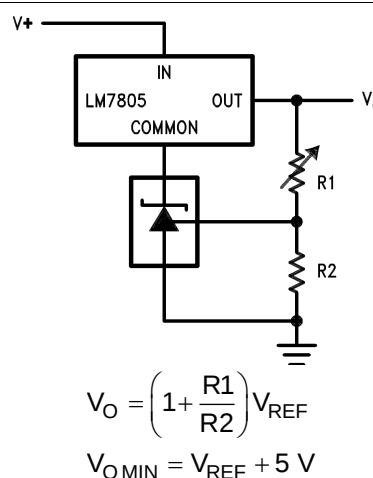


Figure 24. Output Control of a Three-Terminal Fixed Regulator

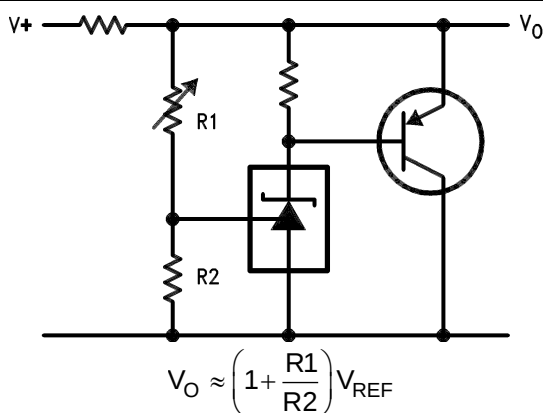


Figure 25. Higher Current Shunt Regulator

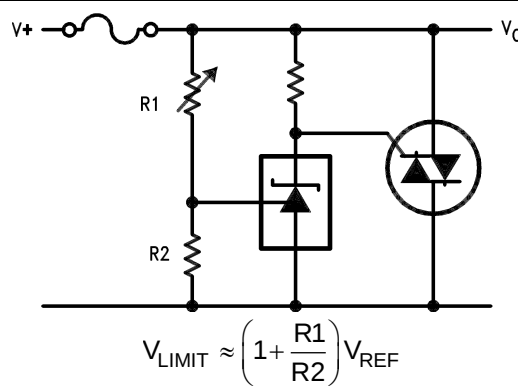


Figure 26. Crow Bar

Typical Application (continued)

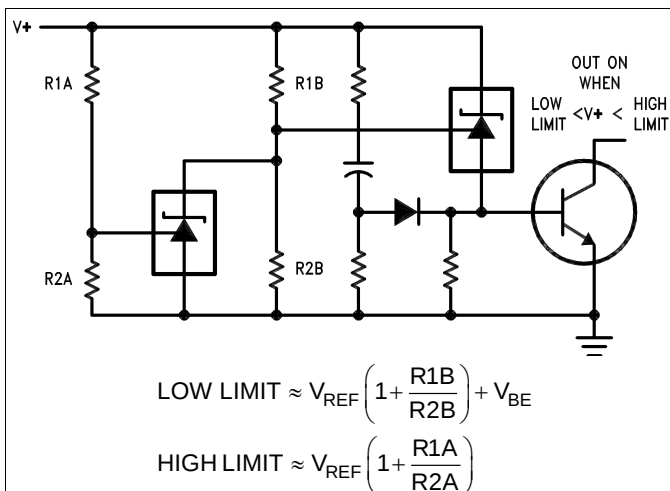


Figure 27. Overvoltage/Undervoltage Protection Circuit

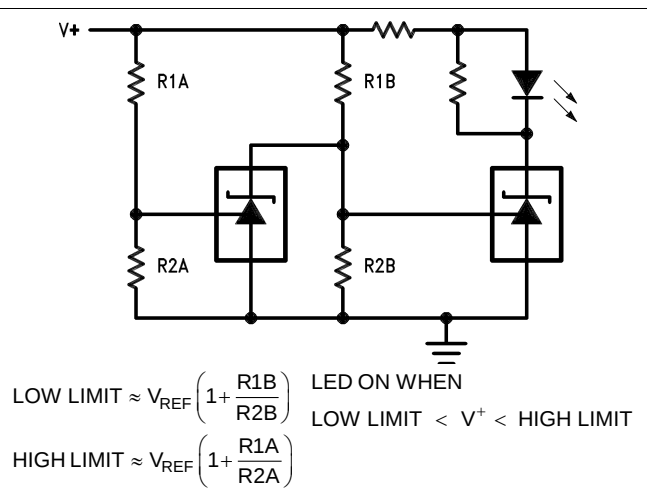


Figure 28. Voltage Monitor

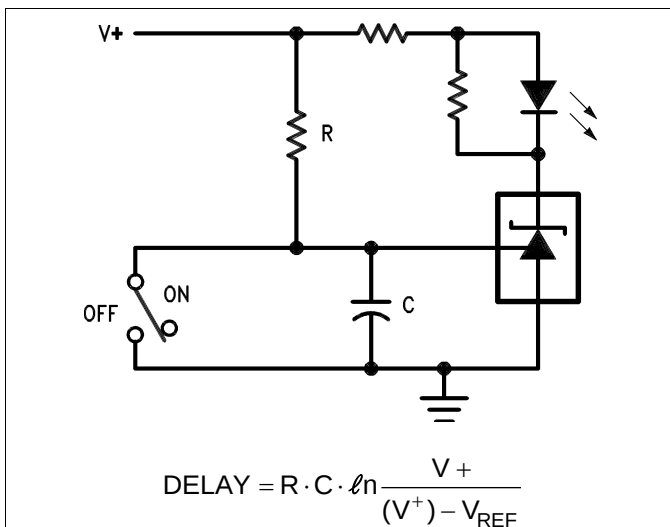


Figure 29. Delay Timer

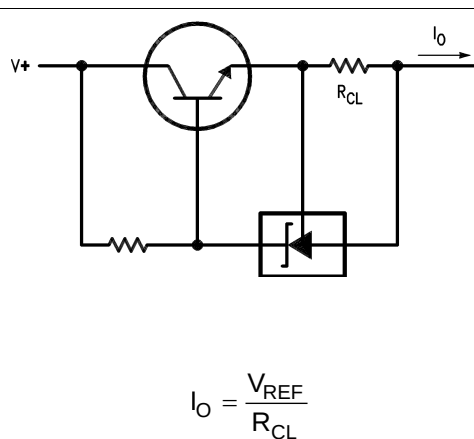


Figure 30. Current Limiter or Current Source

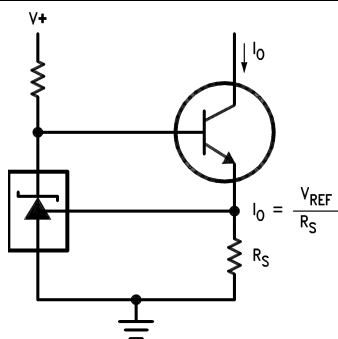


Figure 31. Constant Current Sink

9.2 DC/AC Test Circuit

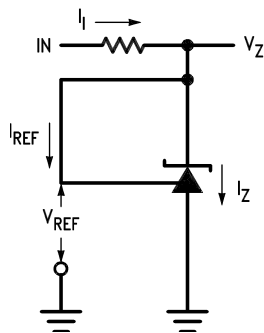


Figure 32. Test Circuit For $V_Z = V_{REF}$

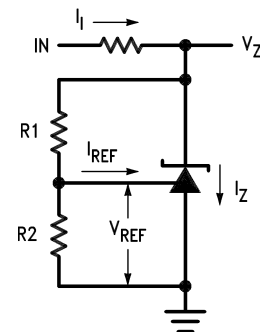


Figure 33. Test Circuit For $V_Z > V_{REF}$

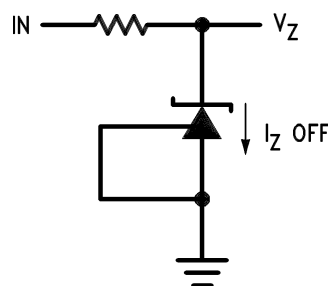


Figure 34. Test Circuit For Off-State Current

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV431	Click here	Click here	Click here	Click here	Click here
LMV431A	Click here	Click here	Click here	Click here	Click here
LMV431B	Click here	Click here	Click here	Click here	Click here

10.2 Trademarks

All trademarks are the property of their respective owners.

10.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV431ACM5/NOPB	Active	Production	SOT-23 (DBV) 5	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N09A
LMV431ACM5/NOPB.B	Active	Production	SOT-23 (DBV) 5	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N09A
LMV431ACM5X/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N09A
LMV431ACM5X/NOPB.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N09A
LMV431AIM5/NOPB	Active	Production	SOT-23 (DBV) 5	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N08A
LMV431AIM5/NOPB.B	Active	Production	SOT-23 (DBV) 5	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N08A
LMV431AIM5X/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N08A
LMV431AIM5X/NOPB.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N08A
LMV431AIMF/NOPB	Active	Production	SOT-23 (DBZ) 3	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RLA
LMV431AIMF/NOPB.B	Active	Production	SOT-23 (DBZ) 3	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RLA
LMV431AIMFX/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RLA
LMV431AIMFX/NOPB.B	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RLA
LMV431AIZ/LFT3	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	-	LMV431 AIZ
LMV431AIZ/LFT3.B	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 85	LMV431 AIZ
LMV431AIZ/NOPB	Active	Production	TO-92 (LP) 3	1800 BULK	Yes	SN	N/A for Pkg Type	-40 to 85	LMV431 AIZ
LMV431AIZ/NOPB.B	Active	Production	TO-92 (LP) 3	1800 BULK	Yes	SN	N/A for Pkg Type	-40 to 85	LMV431 AIZ
LMV431BCM5/NOPB	Active	Production	SOT-23 (DBV) 5	1000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-	N09C
LMV431BCM5/NOPB.B	Active	Production	SOT-23 (DBV) 5	1000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N09C
LMV431BCM5X/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-	N09C
LMV431BCM5X/NOPB.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N09C
LMV431BIMF/NOPB	Active	Production	SOT-23 (DBZ) 3	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RLB
LMV431BIMF/NOPB.B	Active	Production	SOT-23 (DBZ) 3	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RLB
LMV431BIMFX/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RLB
LMV431BIMFX/NOPB.B	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RLB
LMV431CM5/NOPB	Active	Production	SOT-23 (DBV) 5	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N09B
LMV431CM5/NOPB.B	Active	Production	SOT-23 (DBV) 5	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N09B

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV431CM5X/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N09B
LMV431CM5X/NOPB.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	N09B
LMV431CZ/NOPB	Active	Production	TO-92 (LP) 3	1800 BULK	Yes	SN	N/A for Pkg Type	0 to 70	LMV431 CZ
LMV431CZ/NOPB.B	Active	Production	TO-92 (LP) 3	1800 BULK	Yes	SN	N/A for Pkg Type	0 to 70	LMV431 CZ
LMV431IM5/NOPB	Active	Production	SOT-23 (DBV) 5	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N08B
LMV431IM5/NOPB.B	Active	Production	SOT-23 (DBV) 5	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N08B
LMV431IM5X/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N08B
LMV431IM5X/NOPB.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	N08B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV431ACM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431ACM5/NOPB	SOT-23	DBV	5	1000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431ACM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431AIM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431AIM5X/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431AIM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431AIMF/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LMV431AIMFX/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LMV431BCM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431BCM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431BIMF/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LMV431BIMFX/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LMV431CM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431CM5/NOPB	SOT-23	DBV	5	1000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431CM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431IM5/NOPB	SOT-23	DBV	5	1000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV431IM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431IM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV431ACM5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV431ACM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV431ACM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV431AIM5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV431AIM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV431AIM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV431AIMF/NOPB	SOT-23	DBZ	3	1000	208.0	191.0	35.0
LMV431AIMFX/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LMV431BCM5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV431BCM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV431BIMF/NOPB	SOT-23	DBZ	3	1000	208.0	191.0	35.0
LMV431BIMFX/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LMV431CM5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV431CM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV431CM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV431IM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV431IM5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV431IM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

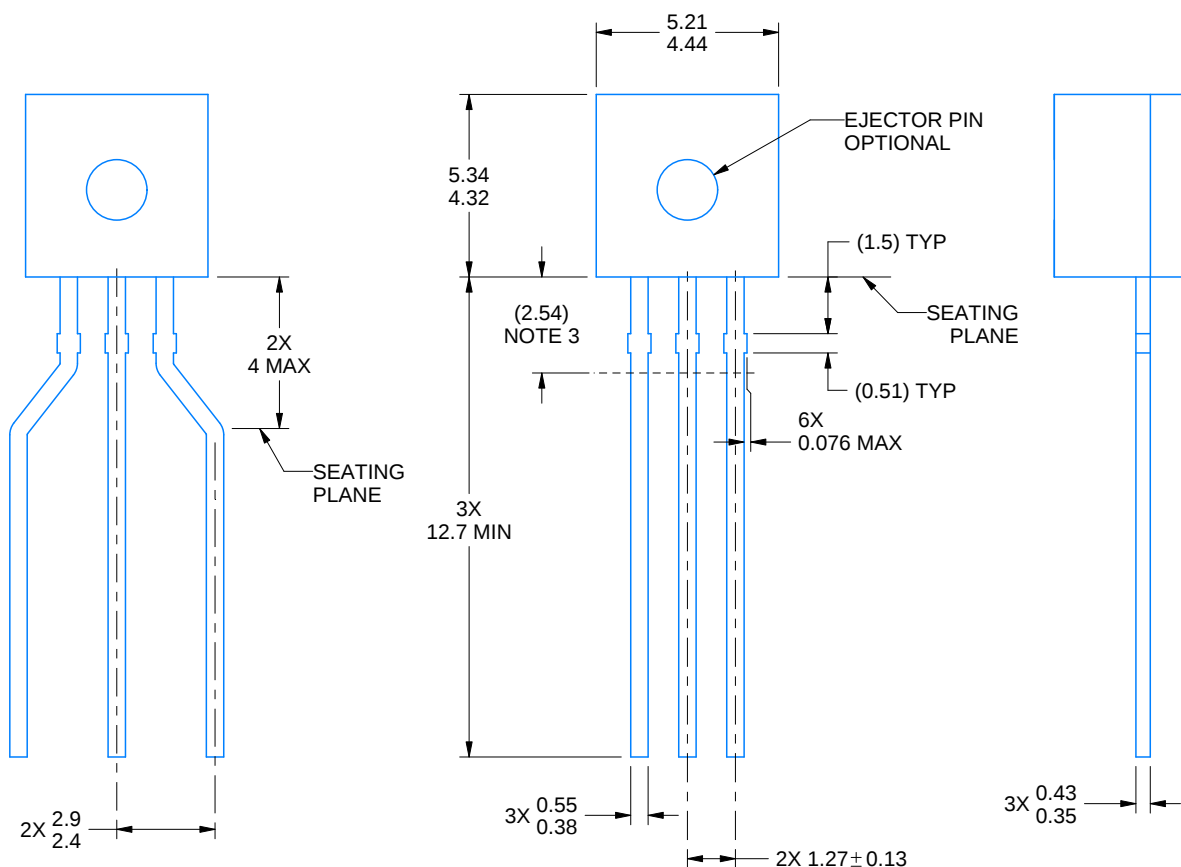
LP0003A



PACKAGE OUTLINE

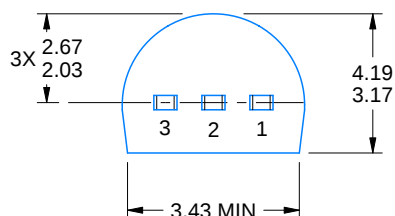
TO-92 - 5.34 mm max height

TO-92



FORMED LEAD OPTION
OTHER DIMENSIONS IDENTICAL
TO STRAIGHT LEAD OPTION

STRAIGHT LEAD OPTION



4215214/C 04/2025

NOTES:

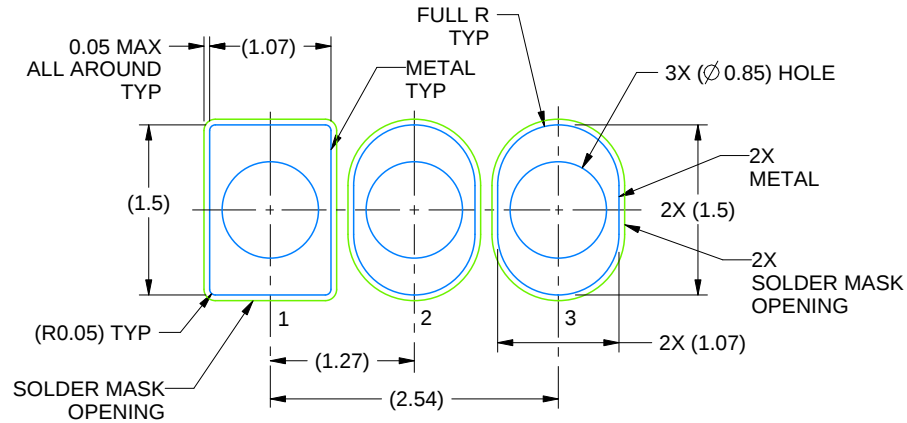
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
 - a. Straight lead option available in bulk pack only.
 - b. Formed lead option available in tape and reel or ammo pack.
 - c. Specific products can be offered in limited combinations of shipping medium and lead options.
 - d. Consult product folder for more information on available options.

EXAMPLE BOARD LAYOUT

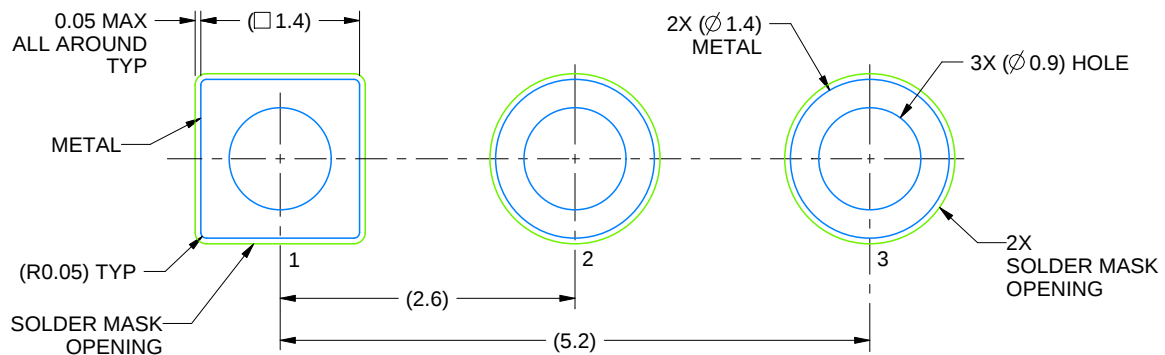
LP0003A

TO-92 - 5.34 mm max height

TO-92



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

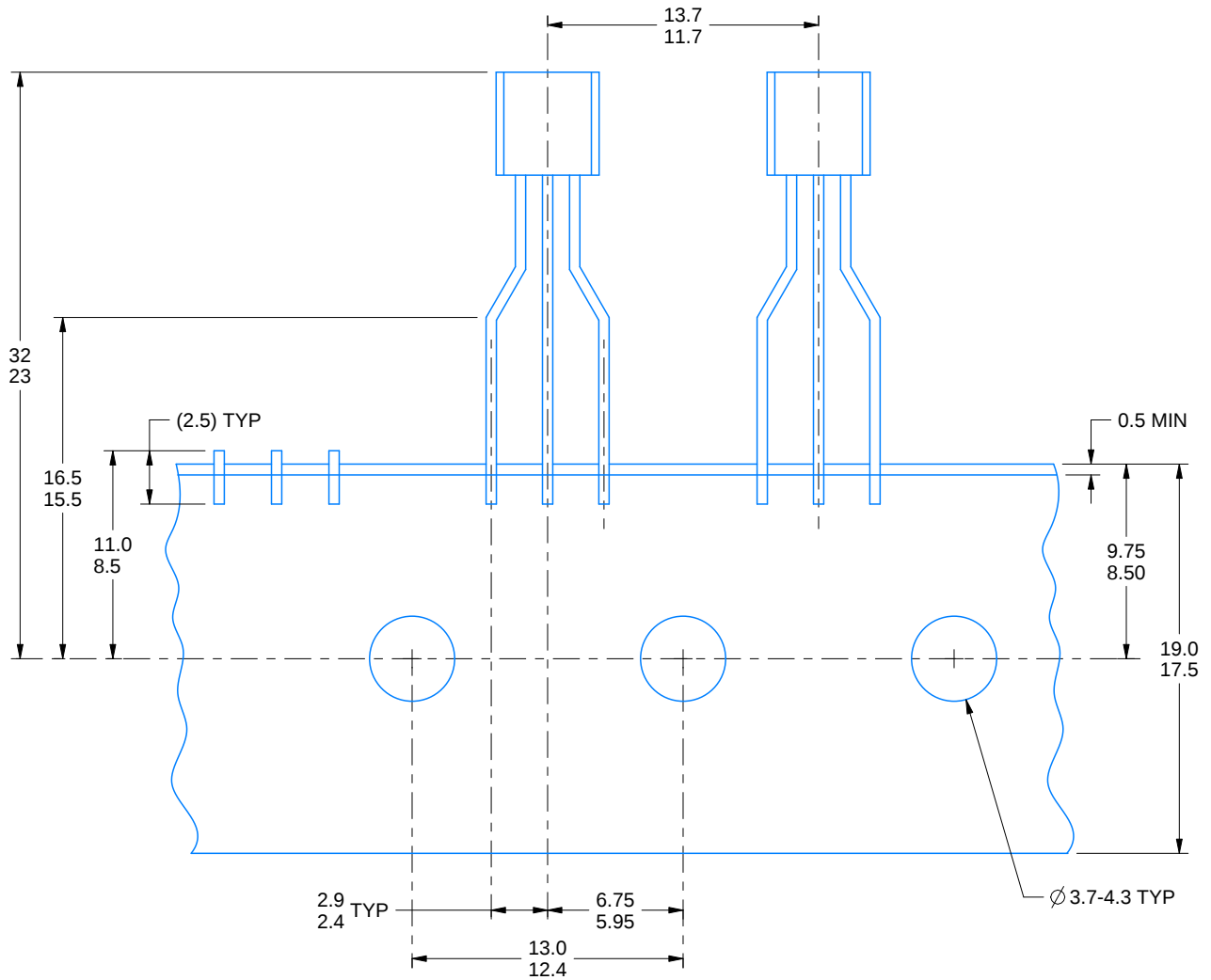
4215214/C 04/2025

TAPE SPECIFICATIONS

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/C 04/2025



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

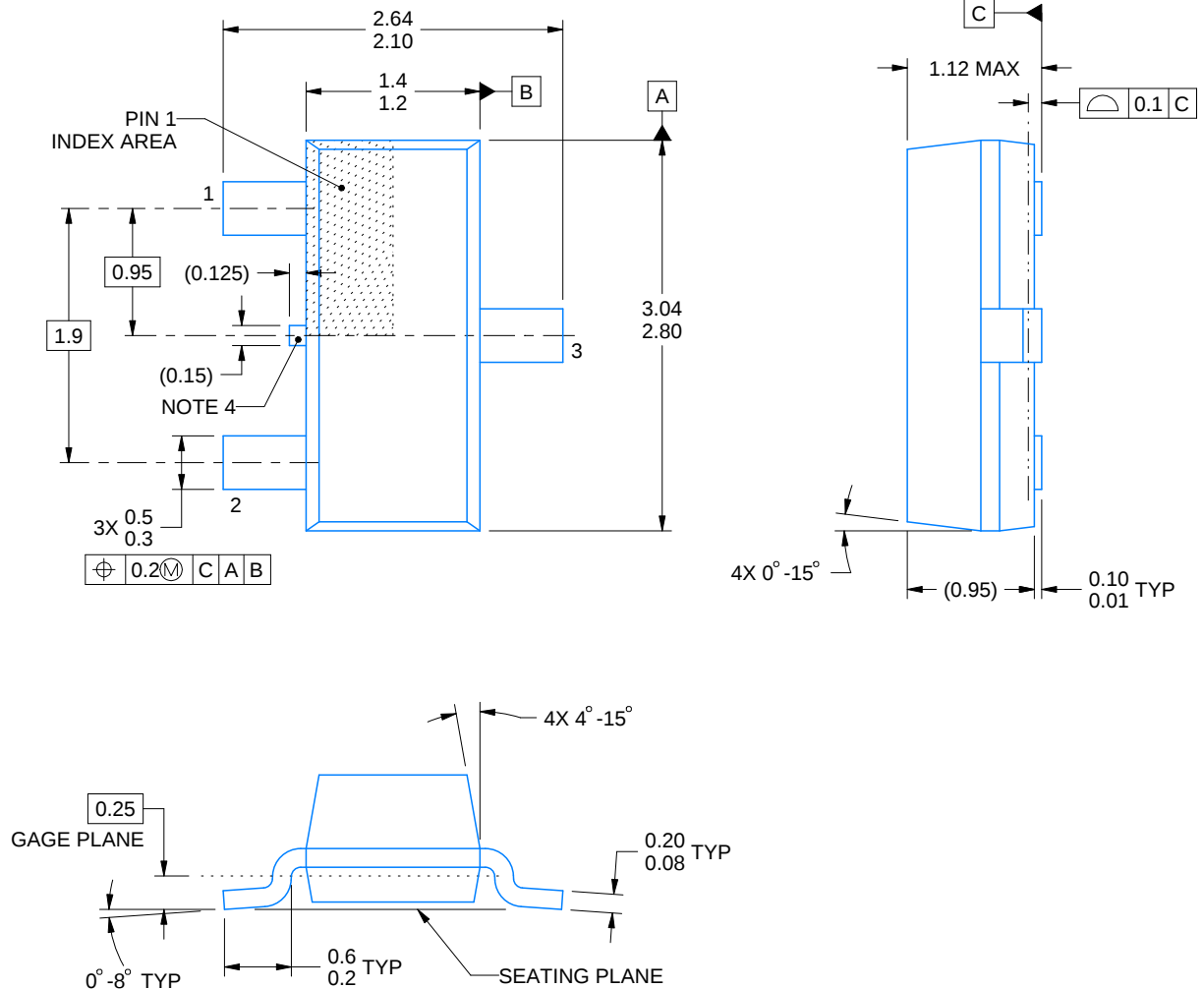
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBZ0003A**PACKAGE OUTLINE****SOT-23 - 1.12 mm max height**

SMALL OUTLINE TRANSISTOR



4214838/F 08/2024

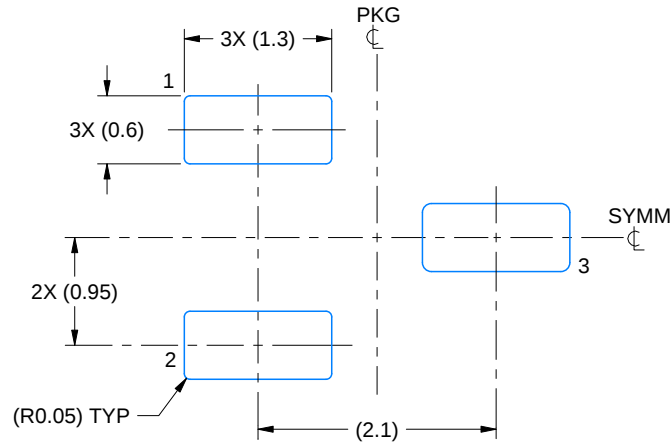
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

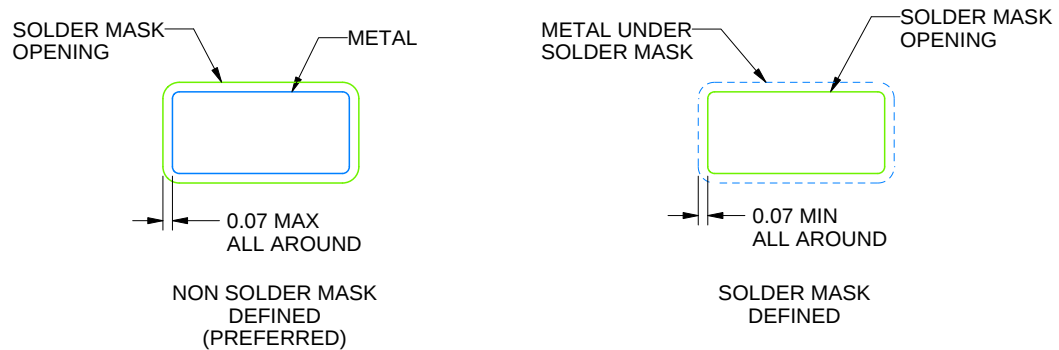
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

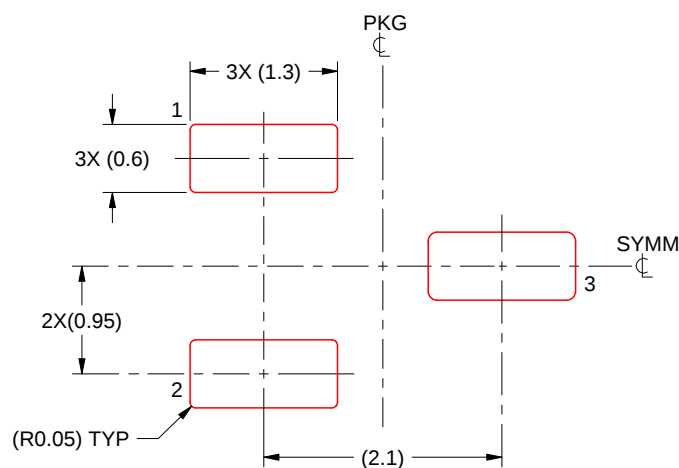
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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